Magneto-electric Transistor Devices and Circuits with Steering Logic

Andrew Marshall
Dept of Electrical Engineering,
University of Texas at Dallas,
Richardson TX 75080, U.S.A.
andrew.marshall@utdallas.edu

Peter A. Dowben
Dept of Physics and Astronomy,
University of Nebraska,
Lincoln, NE 68588, U.S.A.
pdowben@unl.edu

***Abstract*— Magneto-electric transistor (MEFET) schemes are voltage-controlled spintronic devices. Introduced here is a one-source two-drain magneto-electric MEFET, such that each gate has two outputs. This allows logic to be configured with a steering function, switching the electron flux to one of two outputs termed "steering logic". The result is a highly efficient and simple scheme for logic implementation. A majority gate can be constructed with four components (four single input devices) but with only one leakage path and requiring only a single clock cycle to complete the function.**

Keywords*— *Magnetoelectric, Beyond CMOS, logic, steering logic, benchmarking

I. Introduction

The magneto-electric transistor (MEFET) concept has been given increasing consideration as a versatile option for beyond CMOS circuitry [1-6], as this opens the door to spintronics without ferromagnetic domain reversal, and thus the long delay associated with switching ferromagnetic elements. Benchmarking efforts of a variety (MEFET) concepts are progressing [3-7], where there has been an effort to compare the MEFET with CMOS [3].

The MEFET schemes are based on polarization of the semiconductor channel, by the boundary polarization of the magneto-electric gate [1-4] and thus are inherently nonvolatile spintronics devices. The advantage to the magneto-electric field effect transistor is that such schemes avoid the complexity and detrimental switching energetics associated with magneto-electric exchange-coupled ferromagnetic devices. In addition, the canting of the interface magnetization and low barriers to domain switching can be assets to device utilization and may no longer be an issue to device implementation.

Spintronic MEFET devices based solely on the switching of a magneto-electric, are expected to have a switching speed limited only by the switching dynamics of the magneto-electric material, and above all are voltage controlled spintronic devices. The basic device is shown in Figure 1(a). Such magneto-electric spintronic devices are considered a versatile option for beyond CMOS circuitry. This device is an enhancement to the spin transistor proposed by Datta and Das [8].

In the original spin transistor, the applied gate voltage controls the channel spin precession, through electric field generated due to the spin orbit dependent Rashba effect. This results in a change in the source-drain (IDS) current, which represents the state variable of the device.

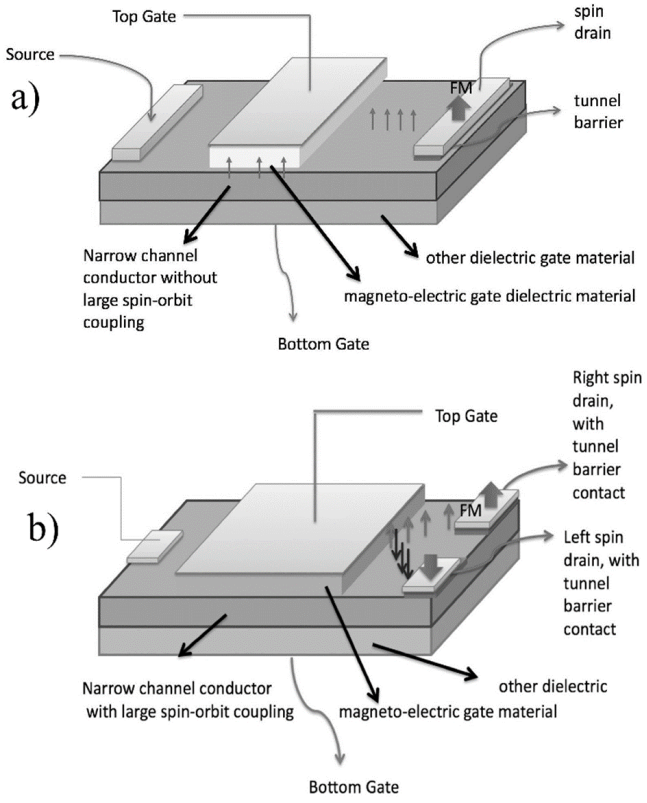

Figure 1: (a) Simple MEFET gate, used in earlier logic schemes. Here the channel is polarized depending on the chromia spin vector orientation. The basic top gated magneto-electric spin-FET with a ferromagnetic (FM) source and drain. (b) View and detail of operation for steering MEFET, showing the dual drain configuration and single source.

Evaluation of beyond CMOS devices is required in order to determine if any of the new concepts may compete favorably with CMOS. To this end, it is important to benchmark equivalent functions that may be available in CMOS and in the process being evaluated. While benchmarking is a vital part of the process, it is also important to evaluate the beyond CMOS

devices in a manner that optimizes their strengths. Here we evaluate the MEFET steering devices in a stacked "steering logic", using the simulation methods described in [7], and find the technique gives improved performance over conventional implementations of logic in MEFET.

This device is ultimately expected to operate down to gate voltages of around 100 mV or less, possesses inherent memory due to the non-volatile AFM order of the magneto-electric and has a sharp turn-on voltage [9-10]. A particular advantage is that the device also has a potential on-off ratio of ~ 106 [11], which is comparable to CMOS and advantageous for implementing logic functions. It also features an extremely low switching delay of around 6 ps (or less), if the antiferromagnetic domain reversal mechanism is coherent rotation [12]. Variants of the device have been proposed as building blocks for conventional-style logic such as inverters, NAND and NOR, recognizable from CMOS logic [1-3]. In addition, the basic MEFET can be used to form very area efficient designs for what in CMOS are compound gates, such as XOR, AND and OR gates [3,7]. While efficient, the problem with the prior evolution of devices, based on the MEFET, is they have aimed to optimize the logic operations at the device level [2-4].

Introduced here is a single-source double-drain magneto-electric MEFET, such that each gate has two outputs that allows logic to be configured with a steering function, directing the electron flux to one of the two outputs. Recent work suggests this one source, two drain device appears to be very close to realization [13-20], and it is only a matter of time before such a device is constructed with an antiferromagnetic magneto-electric as the gate dielectric. Indeed, there are already detailed theoretical efforts to understand how such a device might work [21-22]. The circuit architecture obtained from this type of component is termed "steering logic, and it results is a highly efficient and simple scheme for logic implementation, at the circuit level. The new approach optimizes gate level logic, resulting in greater area efficiency, performance and leakage over conventional designs.

II. MEFET STEERING GATES

A. Logic Functions

Steering logic in the MEFET case steers the electron flux to one or the other of two outputs, based on the local field introduced by the magneto-electric gate on the semiconductor channel, which should have spin-orbit coupling, to make the device operational [21-23]. Thus, in this steering logic MEFET, any gate should have two output ports (Out+ and Out-) to which the electrons are steered. These correspond to the logic "1" and "0" voltage or current levels in the usual transistor logic. It is important to note that when carriers enter either drain only the charge current matter at the outputs. Using a directional spin-orbit state at the source voltage, voltage applied to the gate, steers current to the left or right drain (Figure 1b). This can be used for transparent logic schemes.

Combining steering MEFETs allows all input combinations to impact all outputs. With two tiers of gates, logic gates AND, XOR, or OR logic gates, and their inverses are possible (figure 2). A third input row gives up to eight outputs. This has been noted previously in the context of binary-decision logic [24-26].

B. Majority Gate

We can also generate functions such as the Majority/Minority gate (Figure 3). The majority function typically requires at least four conventional logic gates, but here is constructed with the same 3-tier steering stack from which other three input functions are made. It is clear that the basic majority gate of Figure 3 has several unused steering devices. We can form a gate-optimized version of this majority gate by reviewing the stack for unused gates as well as removing any of the superfluous gates. Further simplifications can be made by combining outputs that have the same function.

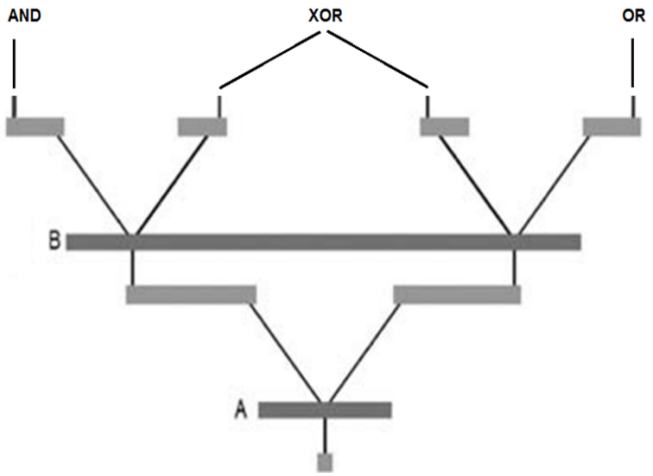

Figure 2: The structure of fig 1(b) can be used to form an AND, XOR or a NOR gate function, as well as the inverse, NAND, OR, and XNOR.

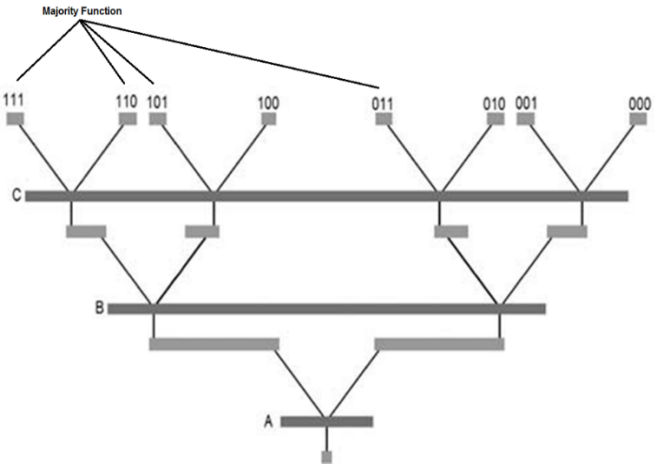

Figure 3: Schematic of a steering logic gate with 3 input gates (A, B, C).This configuration allows any output from any input. Here the majority output combination is shown. It can be stacked for any number of inputs, just by adding extra rows of devices.

Here, the two steering gates connected to the "C" input are doing the same logical function, so the outputs can be merged to form the resultant, much simplified, circuit of Figure 4. Comparing this new MEFET steering gate majority gate to the prior MEFET designs [3] shows that the steering design has lower leakage, and only requires a single clock cycle to complete the function. It also results in improved area efficient.

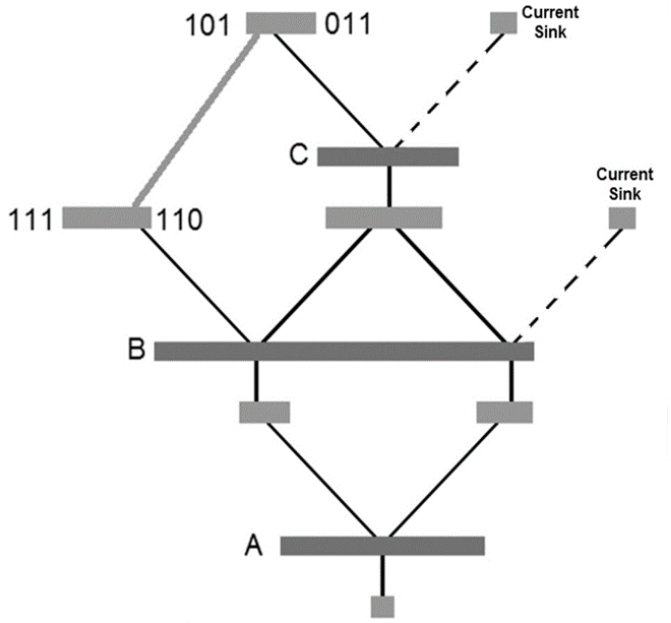

Figure 4: The schematic of the condensed Majority logic function based on the steering, one source, two drain ME-FET devices, of Figure 1a.

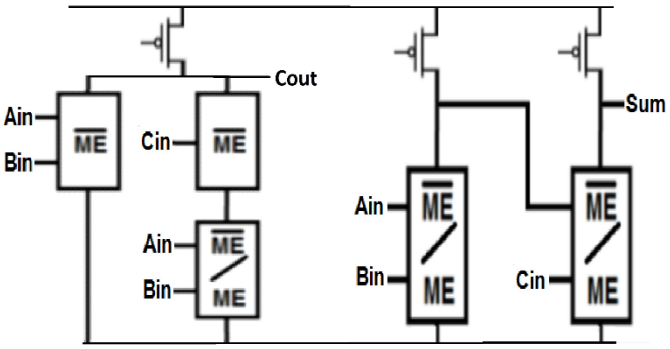

Figure 5: Full adder using conventional MEFET logic design. This has nine input gates, five MEFET devices has three leakage paths to ground, and takes two clock cycles to complete the function.

C. *Full Adder*

The full adder is the most important digital benchmarking circuit. A comparison of CMOS and ME-FET designs has been made previously [3]. This is shown in figure 5. The steering logic version however (figure 6), requires just seven components (seven single input), seven gates, one leakage path, but only a single clock cycle. This has just one leakage path, and only needs a single clock cycle to complete the full add sum and carry functionality The area of prior and steering ME-FET full adders are similar, but the delay for the entire cell is now 50% of the non-steering ME-FET version described in [3]. The delay-to-carry using steering logic is reduced by around 20%, as a result of capacitance reduction, and there is a lowering of leakage power by approximately 25% compared to prior ME-FET logic described in [3].

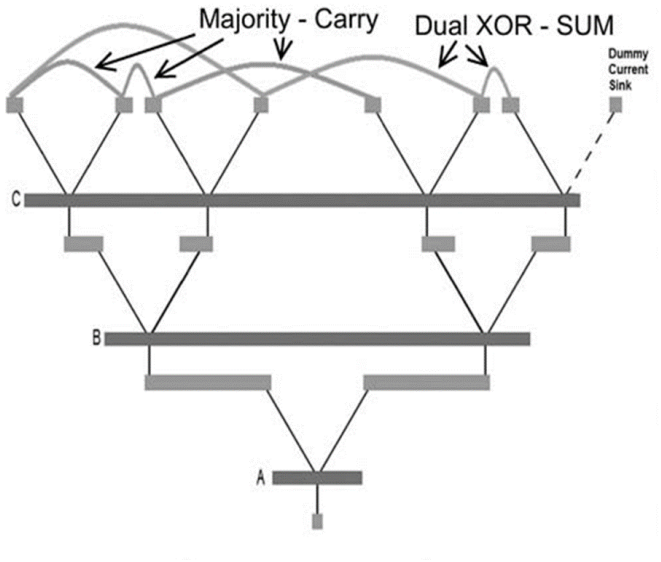

Figure 6: Full adder using combined functions from the steering logic. This same functionality can be obtained from simply combining the circuits in Figures 3 and 4, however such a combination is much less efficient in terms of area, speed and both active and passive power.

A performance comparison of the full adder in CMOS, MEFET (using conventional logic configurations), and MEFET (using a steering logic configuration) assuming a 15 nm equivalent process node, as used in prior benchmarking exercises with beyond CMOS technologies [10], are shown in table 1 and figure 7. These show that the MEFET with steering logic implementation is expected to exhibit similar performance (delay) but for that same delay, have considerably lower power than CMOS.

I. CONCLUSIONS

We have presented a new magneto-electric transistor concept that lends itself to efficient logic architecture, based on MEFET anomalous Hall effect steering logic, where all possible outputs, from a set of static inputs, are available. These outputs can be monitored to generate a variety of logical output functions.

We have determined that in the instance of the industry standard full adder benchmarking circuit, we achieve a reduction in delay time from between 20 to 50%, while at the same time reducing leakage power by 75%. These improvements are achieved in a similar die area. This use of the MEFET

anomalous Hall effect steering logic also permits multiple logical functions to be generated from the same circuitry, by tapping off the different outputs.

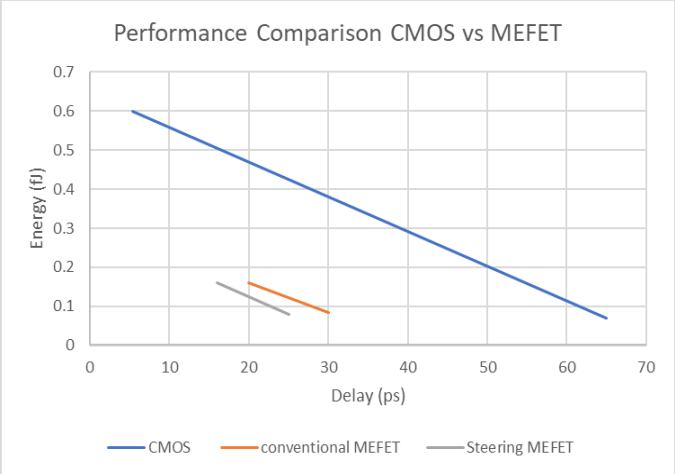

Figure 7: Performance comparison of the full-adder test circuit of CMOS [10], conventional MEFET [3] and steering MEFET (this work). Most desirable performance corner is minimum delay coupled with minimum energy, or performance more toward the lower left corner. As can be seen both MEFET technologies give better performance and lower energy than CMOS, and steering is improved over the regular MEFET configurations.

ACKNOWLEDGMENT

This work was supported by nCORE, a wholly owned subsidiary of the Semiconductor Research Corporation (SRC), through the Center on Antiferromagnetic Magneto-electric Memory and Logic task ID 2760.001, 2760.002 and 2760.003 and by the National Science Foundation (NSF), through Grant No. NSF-ECCS 1740136. The authors are grateful to Dmitri Nikonov for some seminal contributions to this work and Ian Young for pointing out pertinent background to this work.

TABLE I. THE PERFORMANCE COMPARISON OF THE FULL ADDER IN CMOS [10], THE MORE CONVENTIONAL PRIOR MEFET LOGIC [3] AND STEERING MEFET (THIS WORK).

	energy(fJ)	Delay(ps)
HP CMOS	0.6	5.4
LP CMOS	0.07	65
HP MEFET	0.16	20
LP MEFET	0.085	30
HP Steering MEFET	0.16	16
LP Steerig MEFET	0.08	25

REFERENCES

[1] P. A. Dowben, C. Binek, and D. E. Nikonov, in Nanoscale Silicon Devices; edited by Shuni Oda and David Ferry; Taylor and Francis (London) 2016, Chapter 11, pp 255-278.

[2] P. A. Dowben, C. Binek, K. Zhang, L. Wang, W.-N. Mei, J. P. Bird, U. Singisetti, X. Hong, K. L. Wang, D. Nikonov, IEEE J. Exploratory Solid-State Computational Devices and Circuits 4, 1-9 (2018)

[3] N. Sharma, J. P. Bird, Ch. Binek, P. A. Dowben, D. Nikonov, and A. Marshall, "Evolving Magneto-electric Device Technologies", Semiconductor Science and Technology 33 (2020), in the press

[4] C. Pan, A. Naeemi, IEEE J. Explor. Solid-State Computat. 4, 69-75 (2018)

[5] N. Sharma, C. Binek, A. Marshall, J. P. Bird, P. A. Dowben and D. Nikonov, 2018 31st IEEE International System-on-Chip Conference (SOCC), Arlington, VA, USA, IEEE Explore 146-151 (2018)

[6] N. Sharma, A. Marshall, J. Bird, P. A. Dowben, 2017 Fifth Berkeley Symposium on Symposium & Steep Transistors Workshop (E3S) IEEE Xplore, INSPEC Accession Number: 17453928 (2018)

[7] N. Sharma, C. Binek, A. Marshall, J. P. Bird, P. A. Dowben, D. Nikonov, "Compact Modeling and Design of Magneto-electric Transistor Devices and Circuits", IEEE International System-on-Chip Conference (SOCC), 2018, p146-151

[8] S. Datta and B. Das, "Electronic analog of the electro‐optic modulator," Appl. Phys. Lett., vol. 56, no. 7, pp. 665‐667, Feb. 1990.

[9] W. Echtenkamp and C. Binek, "Electric Control of Exchange Bias Training," Phys. Rev. Lett., vol. 111, no. 18, p. 187204, Oct. 2013.

[10] A. Iyama and T. Kimura, "Magnetoelectric hysteresis loops in Cr2O3 at room temperature," Phys. Rev. B, vol. 87, p. 180408, May 2013.

[11] H.-J. Chuang, B. Chamlagain, M. Koehler, M. Madusanka Perera, J. Yan, D. Mandrus, D. Tománek, and Z. Zhou, NanoLetters 2016; doi: 10.1021/acs.nanolett.5b05066

[12] A. Parthasarathy, S. Rakheja, "Dynamics of magnetoelectric reversal of an antiferromagnetic domain", Physics Review Applied 11, 034051 (2019)

[13] A. Avsar, J. Y. Tan, T. Taychatanapat, J. Balakrishnan, G. K. W. Koon, Y. Yeo, J. Lahiri, A. Carvalho, A. S. Rodin, E. C. T. O'Farrell, G. Eda, A. H. Castro Neto, B. Özyilmaz, Nature Comm. 5, 4875 (2014); doi: 10.1038/ncomms5875

[14] Z. Wang, D.–K. Ki, H. Chen, H. Berger, A. H. MacDonald, A. F. Morpurgo, Nature Comm. 6, 8339 (2015); doi: 10.1038/ncomms9339

[15] X. Cui, G.-H. Lee, Y. D. Kim, G. Arefe, P. Y. Huang, C.-H. Lee, D. A. Chenet, X. Zhang, L. Wang, F. Ye, F. Pizzocchero, B. S. Jessen, K. Watanabe, T. Taniguchi, D. A. Muller, T. Low, P. Kim, J. Hone, Nature Nano. 10, 534 (2015)

[16] Z. Wang, C. Tang, R. Sachs, Y. Barlas, and J. Shi, Phys. Rev. Lett. 114, 016603 (2015)

[17] J. Balakrishnan, G. K. W. Koon, A. Avsar, Y. Ho, J. H. Lee, M. Jaiswal, S.-J. Baeck, J.-H. Ahn, A. Ferreira, M. A. Cazalilla, A. H. Castro Neto, B. Özyilmaz, Nat. Comm 5 (2014) 4748

[18] A. M. Afzal, K. H. Min, B. M. Ko and J. Eom, RSC Adv. 9 (2019) 31797

[19] J. Park, H. Duk Yun, M.-J. Jin, J. Jo, I. Oh, V. Modepalli, S.-Y. Kwon, and J.-W. Yoo, Phys. Rev. B 95, 245414 (2017)

[20] Z. Wang, C. Tang, R. Sachs, Y. Barlas, and J. Shi, Phys. Rev. Lett. 114, 016603 (2015)

[21] Z. Qiao, W. Ren, H. Chen, L. Bellaiche, Z. Zhang, A. H. MacDonald, and Qi. Niu, Phys. Rev. Lett. 112, 116404 (2014)

[22] H. Takenaka, S. Sandhoefner, A. A. Kovalev, E. Y. Tsymbal, Phys. Rev. B 100, 125156 (2019)

[23] L.-H. Wu and X. Hu, Phys. Rev. Lett. 114, 223901 (2015)

[24] N. Asahi, M. Akazawa, and Y. Amemiya, IEEE Transactions on Electron Devices 44, 1109 (1997)

[25] S. Kasai and H. Hasegawa, IEEE Electron Device Letters. 23, 446 (2002)

[26] N. Asahi, M. Akazawa, and Y. Amemiya, IEEE Transactions on Electron Devices 42, 1999 (1995)