A THIN-FILM PIEZO-SILICON ACOUSTOELECTRIC ISOLATOR WITH MORE THAN 30 DB NON-RECIPROCAL TRANSMISSION

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ABSTRACT

Bulk acoustic wave (BAW) thin-film lithium niobate (LN)-silicon (Si) delay lines are presented that offer more than 30 dB of non-reciprocal transmission ratio enabled by the acoustoelectric (AE) effect. In this scheme, the interaction of drifting electrons and acoustic phonons turns the microacoustic waveguide into a strong isolator. By tailoring a heterostructure stack of LN and Si, up to ~22 dB of AE gain (160 μW) is measured at only ~4 mW of DC bias power, yielding an unprecedented high power-added efficiency of 4%. This is realized within a 4.3% fractional bandwidth and a spurious-free span of 400 MHz centered around 700 MHz. Furthermore, thermal analysis and measurement results support device operation under large and continuous bias, mostly due to the high thermal conductivity of Si. The increasing demand for non-reciprocal RF components such as isolators and circulators in rapidly growing areas, namely, 5G communications and quantum computing could render this platform a potentially suitable candidate for further investigations.

KEYWORDS

Acoustoelectric Effect; Circulator; Delay Line; Isolator; Lithium Niobate; Non-Reciprocal

INTRODUCTION

While overcoming reciprocity is becoming more important as emerging RF communication protocols are gaining complexity and more stringent requirements, conventionally used ferrite-based solutions are facing limited applicability. This is due to the fact that such components are bulky, expensive, and incompatible with monolithic integration. Conversely, non-reciprocal components are projected to be integrated in virtually all transceivers for self-interference cancellation and enabling simultaneous transmission and receive. Additionally, development of quantum processors is partly tied to such components in the form of isolators and circulators as they are an essential part of the readout architecture of individual qubits and the greater the number of qubits, the more the number of required non-reciprocal components.

Considering such great impacts, which are simplistically represented in Fig. 1 (a), different magnet-less approaches have been taken to overcome reciprocity. These efforts can be mainly categorized into using nonlinearity [1], [2], space-time modulation [3] – [5], and external bias. The first approach often involves frequency conversion and attains narrow bandwidths with weak non-reciprocity. Modulation based approaches, on the other hand, overcome such issues but a synchronized clock is an essential component for their application [6]. Among the last category a promising solution is based on utilization of the acoustoelectric (AE) effect which takes advantage of direction-dependent energy coupling between drifting electrons and acoustic phonons to amplify or attenuate piezoelectrically generated acoustic waves (AW) in a micro-scale waveguide. A major advantage of this scheme is the very slow velocity of AW compared to electromagnetic waves. This allows for extreme miniaturization and longer retention of information, both of which are desired for the targeted applications.

Non-reciprocity due to the AE effect has been demonstrated in various platforms employing surface acoustic waves (SAW) [7] - [13] and more recently bulk acoustic waves (BAW) [14], [15], however, the reported power-added efficiencies ($PAE = (P_{RF\_out}–P_{RF\_in})/P_{DC\_bias}$) have been so far limited to below 2%; the very high DC power consumption or very low AE gain and non-reciprocity are mainly attributed to the limited coupling between the drifting electrons and the piezoelectric field. Nevertheless, BAW waveguides are advantageous in terms of frequency scaling, reduced propagation loss, and higher electromechanical coupling (K^2) – with the latter being especially important as it warrants a larger AE efficiency and operational bandwidth. Consequently, in this work we present a BAW delay line implemented on a heterostructure made from lithium niobate (LN) bonded onto silicon (Si) with a passband frequency at ~700 MHz. By proper selection of the thickness of the two films, such waveguides demonstrate above 20 dB of AE gain and 30 dB of non-reciprocal transmission ratio (NTR = S_{21}/S_{12}).

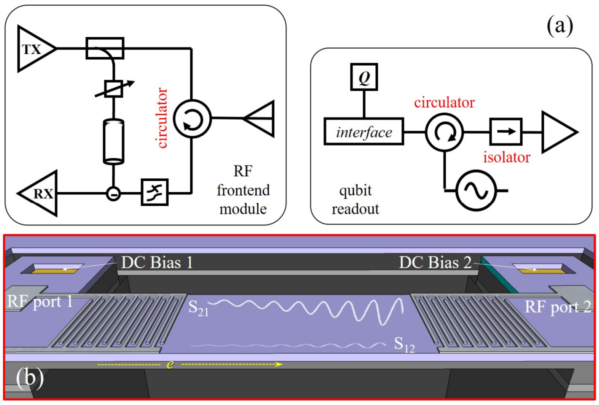

Figure 1: (a) A simplistic architecture for RF frontends (left) and qubit readout circuit (right) where non-reciprocal components in the form of circulators and isolators are essential. (b) Conceptual schematic of an AE BAW delay line showing AE gain/loss due to electron drift in Si (direction shown by the yellow arrow).

DESIGN AND SIMULATIONS

The delay line is formed on a suspended LN-Si heterostructure with two pairs of interdigital transducers (IDT) positioned along its two ends. AW are launched and

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detected by such IDTs while supersonic electrons drifting along (or the opposite of) the AW propagation axis will result in amplification (or attenuation) of the wave. This is done by pumping electrons in the Si layer through the DC bias points at the two ends of the waveguide; as conceptually shown in Fig. 1 (b). The resulting momentum exchange is highly dependent on the K^2 as well as the electrical properties of the Si film. Among such electrical properties, a high electron mobility and relaxation time are desired. For the case of Si, at relatively low n-type doping concentrations (resistivity ~6 Ω-cm), the mobility could be as high as ~1400 cm^2/(V·s); on the other hand, a thinner Si film would increase the relaxation time, however, too thin of a film would eventually decreases the mobility due to the increased scattering.

To achieve a very high K^2, fundamental symmetric lamb waves (S_0) propagating along Y+30° of X-cut LN are targeted. The thickness of the LN and Si are respectively chosen to be 1 µm and 0.8 µm; from the dispersion characteristic of the device stack using a 3D COMSOL model, K^2 is estimated and plotted in Fig. 2. A finger pitch (*FP*) of 5 µm is chosen for the IDTs in this work, resulting in a K^2 of ~16% and a passband center frequency of ~700 MHz. A much larger K^2 and subsequently, AE gain is postulated for a thinner Si film.

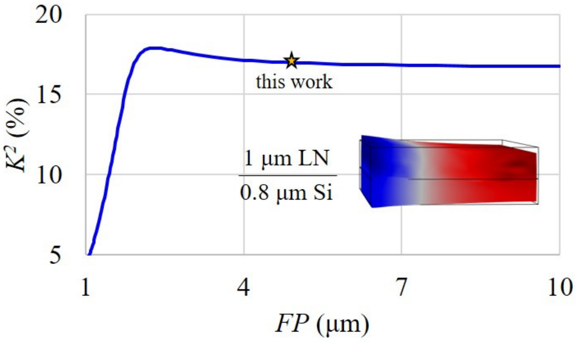

Figure 2: The stress profile and electromechanical coupling (K^2) of S_0 mode derived from the dispersion characteristic of the device stack showing a K^2 of ~16% at FP =5 µm.

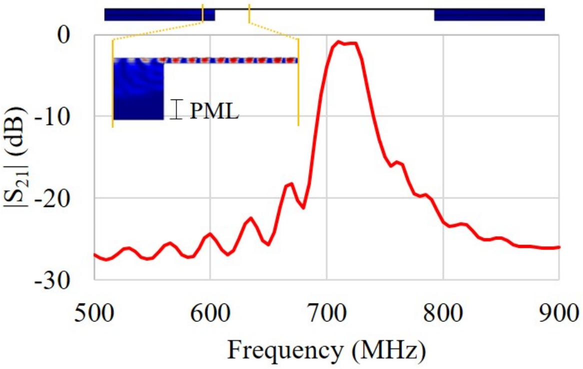

Figure 3: The transmission response of the delay line structure (shown on top) simulated by COMSOL 2D analysis; the structure is terminated in PML from the bottom.

Next, in order to study the frequency response of the delay line, a 2D COMSOL model is used and the device is mechanically terminated with a perfectly matched layer (PML) from the bottom side to mimic the irreversible energy leakage into the substrate. Fig. 3. shows the simulated frequency response of a 200 µm long device (L200) which is defined as the separation between the two port IDTs. The simulated structure has 20 pairs of IDTs with a *FP* of 5 µm for excitation/detection.

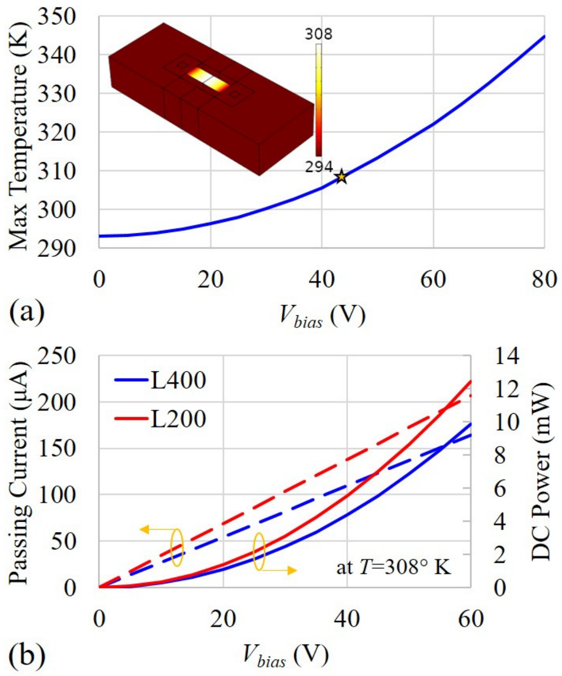

Figure 4: (a) The effect of Joule heating on temperature of the delay line simulated by COMSOL; moderate heating enables operation under a large continuous DC bias. (b) DC power pumped into the device and current passing through it as a function of V_{bias} simulated for two device lengths.

A major drawback of many of the AE devices is the excessive heating under the continuous bias operation, requiring a pulsed operation. In this case, as a result of the low thermal conductivity of the structure, Joule heating can permanently damage the device. Si, on the other hand, with its considerably larger thermal conductivity enables continuous bias operation. This is validated using a COMSOL model to study the thermal behavior of the device under a constant bias. Joule heating due to current passing through the Si layer and convective air cooling are added to the model and the steady state maximum device temperature (T) as a function of the applied bias (V_{bias}) is plotted in Fig. 4 (a). As an example, at V_{bias} = 45 V the temperature rises by only 14° K.

The former model is also used to determine the DC power consumption of the delay line as a result of applying the bias. This is to separate the unwanted resistive loss from the actual power pumped into the device. The former is due to the poor contact to the Si during the experiment which yields at least four times larger than expected resistance to be measured across the bias terminals. As a result, the value of passing currents from the simulation and measurement are compared and used to estimate the actual DC power/voltage pumped into the device. Fig 4. (b) shows the value of current passing through the delay line as well as the dissipated bias power as a function of the applied voltage for two device lengths. Temperature drift of such values is taken into consideration and for simplification the plots assume $T = 308°$ K which occurs at $V_{bias} = 45$ V.

FABRICATION

The fabrication process flow for the BAW delay lines starts with a bonded stack of thin films of LN and Si on insulator. The deposition and patterning of IDTs (0.1 µm Mo in this work) is performed next followed by etching the LN film to expose Si layer for DC bias contacts and overlaying the probing points to reduce Ohmic loss with Au. Next step is etching the device stack down to the insulator layer and the final step is suspending the devices by removing the handle layer. The scanning electron micrograph (SEM) of a fabricated device is shown Fig. 5 with the inset showing the close-up of the suspended device stack. The delay line has a footprint of ~0.8 mm^2.

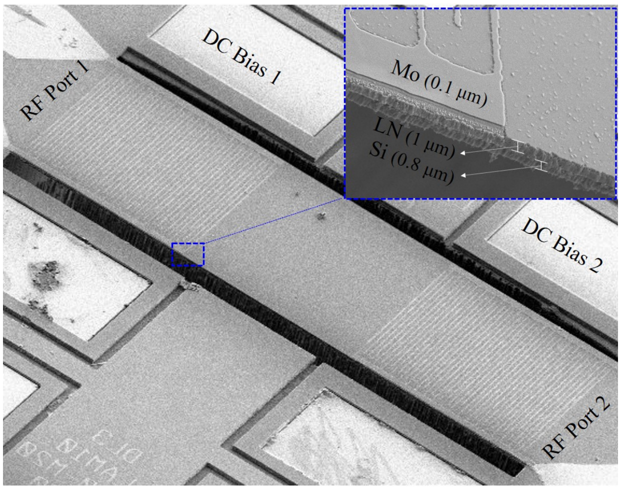

Figure 5: The scanning electron micrograph (SEM) of the BAW delay line (L200) with its connections labeled; the inset shows the device stack close-up.

MEASUREMENT RESULTS

The delay lines are first characterized using a calibrated vector network analyzer (VNA) at room temperature and atmospheric pressure. A pair of RF microprobes for the 2 ports and a pair of DC microprobes for the DC bias terminals are used. The input power of the VNA is set at 0 dBm. The transmission (S_{21}) and reverse isolation (S_{12}) of a 400 µm long device (L400) is plotted in Fig. 6 with solid and dashed black lines, respectively; without the DC pump, reciprocity is evident. Once the DC bias is applied, AWs travelling along the electrons are amplified and an AE gain of up to ~22 dB (160 µW) is measured; this is plotted by red in Fig. 6 leading to a minimum insertion loss (IL) of 7.9 dB. Conversely, AWs travelling opposite to the electrons are attenuated by more than 9 dB leading to a NTR of more than 31 dB; this is shown by the blue curve in Fig. 6 with an IL of above 40 dB. The device under test (DUT) demonstrates a spurious-free response in the span of 400 MHz with a minimum suppression of 20 dB. The 3dB fractional bandwidth (FBW) of the DUT is measured to be 4.3%. The current passing through the device in this case is measured to be 85 µA which from Fig. 4 (b) corresponds to ~4 mW of input DC pumped power; this results in a high *PAE* of 4%. The port reflections are shown in Fig. 6 as well with the DUT being matched to 50Ω ports.

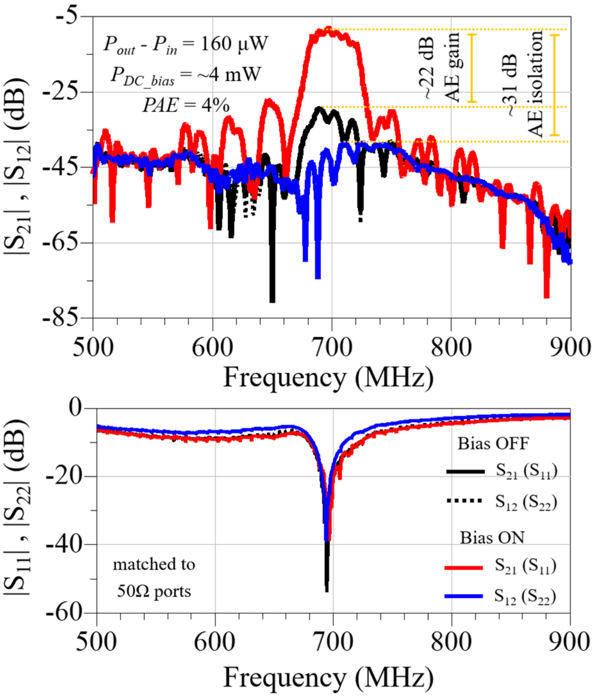

Figure 6: Measured transmission and reverse isolation of a L400 delay line once the bias is ON/OFF (top) and same for port reflections (bottom). AE gain of ~22 dB with ~31 dB isolation is achieved for a DC bias power of only ~4 mW (corresponding to V_{bias} <45 V).

In order to determine the efficiency of the AE effect as a function of the input RF power level, a single tone test is performed. For this task a 700 MHz tone at power levels of 0 to 18 dBm is generated by means of a signal generator and fed to the DUT while the output of the DUT is fed to a spectrum analyzer. The signal level before and after applying the bias is measured and from the difference of the two, the AE gain is calculated. This is shown in Fig. 7 for two 200 µm long delay lines (L200) with apertures of 150 µm (A150) and 200 µm (A200). In each of the cases, the bias pump power is respectively fixed at 13.5 mW (11.3 dBm) and 6.3 mW (8 dBm), determined in the same manner as explained in the previous section. A higher *PAE* is evident for the A200 device. Additionally, comparing the results from the L400 and L200 delay lines shows that the longer device is much more efficient; with ~22 dB of gain at only ~4 mW for former (*PAE* = 4%) compared to ~15 dB of gain at more than 6 mW for latter (*PAE* < 1%). It is worth mentioning that the IL of all the delay lines studied are in the range of 30 dB without any bias application. This is believed to be mainly due to the roughness of device boundary from etching steps as well as the Ohmic loss of the Mo IDTs.

Finally, to investigate the application of the AE delay lines as a building block of an AE circulator, the circuit shown in Fig. 8 is simulated by Keysight ADS; for this task, the measured data from a biased L400 device is used while the delay lines (assumed identical) are coupled together by power dividers.

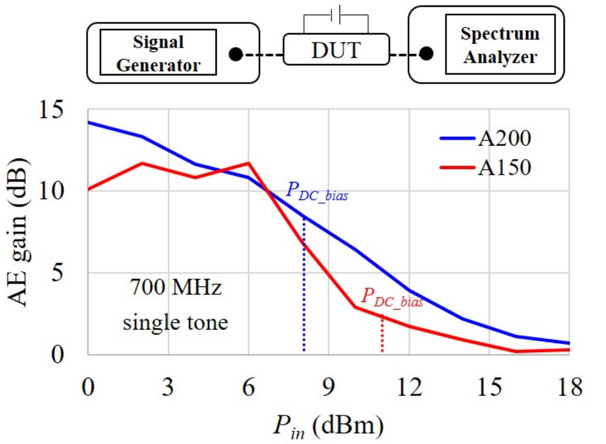

Figure 7: Measured AE gain of L200 delay lines as a function of the input RF power level. A single tone 700 MHz signal as shown in the measurement setup is used while a higher PAE is observed for A200 device.

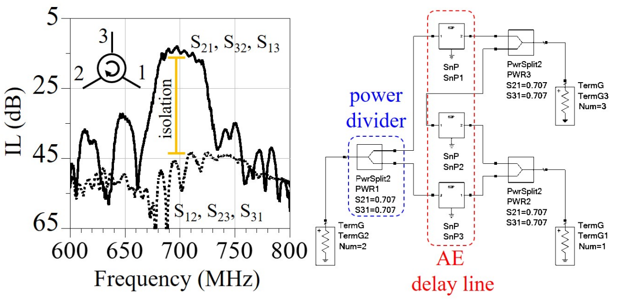

Figure 8: Simulated response of a circulator made from 3 AE delay lines connected together with power dividers using the measured response of a L400 device.

CONCLUSION

Taking advantage of the acoustoelectric (AE) effect, microacoustic isolators in lithium niobate-silicon heterostructures were demonstrated. Upon application of a bias voltage and injecting drifting electrons in the Si layer the acoustic delay lines become strongly non-reciprocal and proper selection of the thicknesses of the thin films results in a very high AE gain and non-reciprocity at a relatively low DC bias power.

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