W-Band MMIC Chip Assembly Using Laser-Enhanced Direct Print Additive Manufacturing

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***Abstract*— In this article, the first *W*-band laser-enhanced direct print additive manufacturing (LE-DPAM) monolithic microwave integrated circuit (MMIC) chip-carrier assembly is demonstrated. Acrylonitrile butadiene styrene (ABS) is 3-D printed using fused deposition modeling to form substrate layers, and DuPont CB028 conductive paste is microdispensed to form transmission lines and on-chip interconnects. These processes are combined with picosecond-pulsed laser micromachining using two wavelengths in the infrared (IR) (1064 nm) and ultraviolet (UV) (355 nm) regions to create features as small as 5 μm for printed layers with a high 6:1 aspect ratio and to improve the effective conductivity of the printed traces. The laser machining process is also adopted to fabricate vertical interconnections (vias) over multilayer substrates while also suppressing higher order modes. Four different dc-to-110-GHz transmission-line configurations have been investigated, including a coplanar waveguide (CPW), a grounded CPW (GCPW), a novel multilayer CPW-microstrip transition, and a GCPW-microstrip transition with attenuation <0.3 dB/mm and return loss >10 dB. This process is extended to embed a *W*-band MMIC low-noise amplifier (LNA) die inside a laser-machined cavity with a carrier-chip gap less than 5 μm. Also, RF/dc interconnects were microdispensed to connect the transmission lines on the substrate and MMIC die. Chip-to-board transition loss as low as 0.03 dB per interconnect with return loss >7.5 dB was achieved with performance that is comparable to that of the probed MMIC die. The MMIC chip-carrier assembly provides a low-cost, versatile yet simple on-demand laser-enhanced additive manufacturing process to package a wideband MMIC die using a single automated LE-DPAM platform.**

***Index Terms*— Broadband transmission lines, fused deposition modeling (FDM), integrated circuit interconnects, laser machining, microdispensing, millimeter wave (mm-wave), multichip module (MCM), RF packaging, 3-D printing, wire or ribbon bonding.**

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I. Introduction

THE push for fifth-generation (5G) wireless and millimeter-wave (mm-wave) applications requires cost-effective yet high-performance fabrication and packaging techniques [1]. Additive manufacturing (AM) technologies, such as aerosol jet printing (AJP), inkjet printing, microdispensing, and fused deposition modeling (FDM), have been used to manufacture mm-wave transmission lines [2]–[18]. These techniques are viable for the fabrication of multichip modules that include monolithic microwave integrated circuit (MMIC) chip assembly packages with multilayer interconnects for low manufacturing cost while facilitating rapid prototyping and design customization [6], [13], [19]–[28]. With continuous improvements, the overall performance of additive manufactured interconnects is now comparable to that of the best multilayer printed circuit boards (PCBs) and thin-film circuits on ceramic substrates. This work further advances the state of the art to enable *W*-band operation, by leveraging our prior works such as a 2.45-GHz phased array antenna fabricated by direct print additive manufacturing (DPAM) [19] and packaging of a 20-GHz MMIC chip by laser-enhanced DPAM (LE-DPAM) [20].

Undoubtedly, there have been significant advances in mm-wave packaging that have brought greater levels of integration, reduced size, and weight, as well as performance improvements. Historically, mm-wave package assemblies were based on split-block, milled metal housings [1], [29]. The evolving need to reduce weight and cost drove the demand for system-in-a-package (SiP) concepts that led to multiple promising techniques for integrated circuit (IC) chip integration, such as chip-on-board (COB) or direct chip attach (DCA) [30]–[32], multichip module laminate/deposited/ceramic (MCM-L/C/D) packages [33]–[35], and land-grid array (LGA) with integrated antennas [1], [36], [37]. These packaging technologies typically involve nonplanar, multilayered, complex processes that require multiple tools and expensive processing techniques and development. These challenges present opportunities for AM-based packaging solutions that can offer high-performance integration capability that is both cost-effective and compact for mm-wave frequency SiP applications.

A particular aspect of mm-wave packaging where LE-DPAM can be advantageous is the chip-to-board

integration. Typically, chip-to-board interconnects between the MMIC dies and the packaging substrate utilize thermosonic ribbon bonds that require precise alignment and special bonding layers [38]–[42]. For ribbon-bond interconnects over a certain loop length, sizable parasitic inductance can be introduced, which leads to reflection and radiation losses [43], [44]. Thus, to operate efficiently at W-band frequencies, ribbon-bond lengths need to be kept as short as possible. The parasitic inductance of ribbon bonds can be compensated in a PCB/MMIC assembly by adding capacitance, however, this reduces operational bandwidth and could further complicate the design and fabrication [30], [44]–[46]. Ribbon bonds may also be vulnerable to failure under high vibration environments [26], [38], [47]–[49]. Another approach used for the chip interconnect is flip-chip technology, which generally requires underfill layers that require detuning, very flat surfaces, and substrates that can withstand high-temperature and high-pressure processing [42], [48], [50]–[53]. While the flip-chip approach provides short chip-to-board connections, it has poor thermal dissipation that makes it not well suited for high-power applications [52]. LE-DPAM can address the tight chip-to-board integration requirement while keeping the backside ground of the MMIC on a stable heatsink, by embedding the MMIC in a laser-machined cavity.

The processes used with the proposed LE-DPAM approach are carried out on a single automated platform and include FDM of a thermoplastic, such as acrylonitrile butadiene styrene (ABS), microdispensing of silver paste (e.g., DuPont CB028), and picosecond-pulsed laser machining at wavelengths of 355 or 1064 nm. Because of the ability to print in three dimensions using a computer-aided design (CAD) model, AM can simplify the fabrication of an otherwise complicated structural and/or electronic device. LE-DPAM also enables low production costs and design customization with a fast turnaround time. Important advantages of LE-DPAM that set it apart from traditional manufacturing techniques include layer-by-layer 3-D printing of multimaterial structures and sloped or curved surfaces, and the ability to generate high-aspect-ratio cavities and vias as small as 100 μm wide, all of which are demonstrated in this article. The picosecond-pulsed laser machining achieves high accuracy for features as small as 5 μm while improving the performance of the transmission lines. These approaches help to overcome some of the main challenges for AM such as low metal layer conductivity and low resolution in the printed features while maintaining tight tolerances for the circuit dimensions.

The work presented in this article was initiated with an analysis on 5G and W-band packaging technology [1], followed by demonstrations of LE-DPAM to fabricate coplanar waveguide (CPW) transmission lines operating from dc to 110 GHz [2]. In Section III, new dc-to-110-GHz LE-DPAM transmission-line configurations with attenuation as low as 0.3 dB/mm at 110 GHz are presented. A CPW fabrication process with reduced complexity compared to that used in [2] is employed to demonstrate a novel CPW-to-microstrip transition based on a via-less configuration. In addition, a grounded CPW (GCPW) transmission line and a GCPW-microstrip transition are demonstrated. These designs are less susceptible

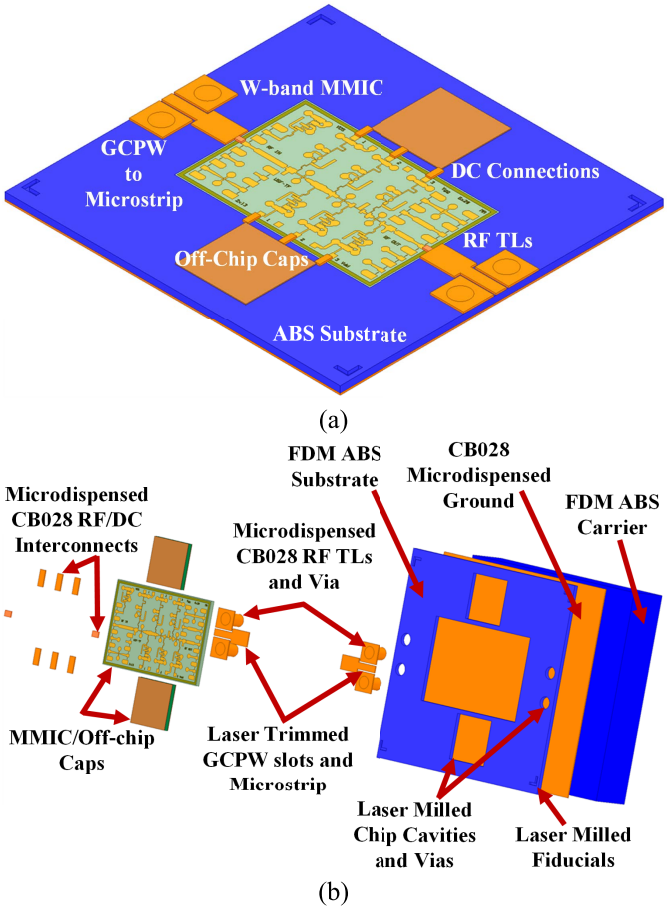

Fig. 1. (a) Isometric and (b) exploded illustrations of the LE-DPAM W-band LNA chip-carrier assembly.

to undesired mode excitations and exemplify the ability to simplify an otherwise complex structure using LE-DPAM. In Section IV, the LE-DPAM techniques are further investigated to demonstrate a multilayered chip-carrier assembly of a W-band low-noise amplifier (LNA) MMIC chip, as shown in Fig. 1. The MMIC chip is embedded in a laser-machined cavity so that the top of the chip is at the same level as the surrounding substrate. The lateral dimensions of the cavity can be laser-machined to match the dimensions of the die to within a 5-μm margin. This technique enables a virtually zero-length chip-to-board interconnect to be directly printed from the substrate to connect with the probe pads of the MMIC die, thus enabling broadband operation up to 110 GHz.

II. LE-DPAM Fabrication Process

The LE-DPAM process used in this work is carried out with an nScrypt 3Dn tabletop system. The automated platform is equipped with a Lumera SUPER RAPID-HE picosecond-pulsed laser with 355-nm ultraviolet (UV) and 1064-nm infrared (IR) wavelengths while holding an alignment accuracy of 0.5 μm. This digital manufacturing platform integrates FDM, microdispensing, and laser machining. ABS, a thermoplastic with $\varepsilon_r = 2.35$ and $\tan_\delta = 0.0065$ measured at 30 GHz [54], is used to print the dielectric substrate with a minimum single-layer thickness of 20 μm, where the ABS filament is extruded from a 200-μm inner diameter and

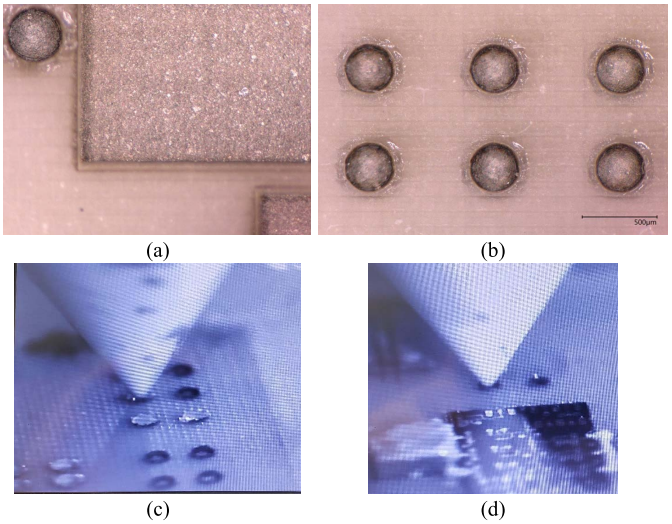

Fig. 2. Images of (a) exposed bottom CB028 silver paste ground plane after laser milling the via and chip cavities using the 355-nm laser. (b) 300-μm-wide via laser milled before microdispensing showing exposed bottom CB028 ground. (c) 300-μm-wide via being filled with CB028 using a 75-μm-diameter ceramic nozzle. (d) Microdispensing CB028 for the transmission lines, interconnects, and via for the assembled MMIC die.

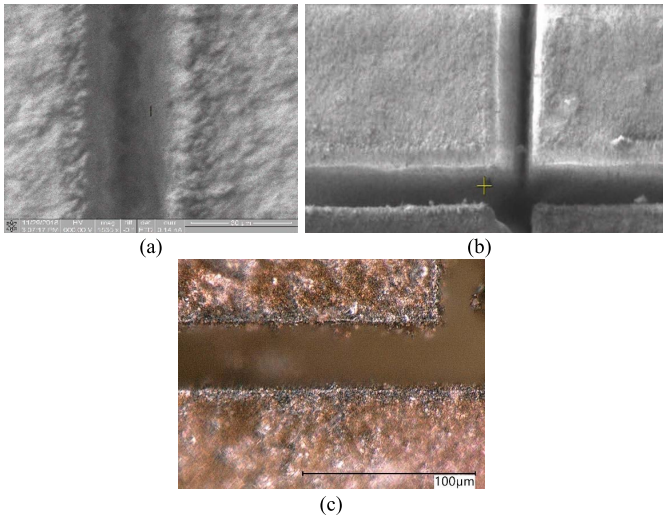

Fig. 3. Laser milled slots using (a) 1064- and (b) and (c) 355-nm picosecond laser pulses. (a) and (b) 15-μm slot width with 30-μm-thick silver paste with (b) 355-nm laser machined slot with smooth wall surfaces. (c) 2000× zoomed-in image of a 35-μm slot showing a 2-μm region of sintered paste on the slot edges.

240 °C heated FDM nozzle onto a 110 °C heated bed. The conductor layers for the transmission lines and chip-to-board interconnects are formed by microdispensing a conductive silver paste (Dupont CB028) using a 50- or 75-μm-diameter microdispensing nozzle. The printing height (the distance from the tip to the substrate during printing), air pressure, and printing speed are 15–80 μm, 3 psi, and 2.5 mm/s, respectively. The CB028 silver paste is dried *in situ* on the printer bed heated at 110 °C to achieve a dc bulk conductivity of 2 MS/m [19]. The CB028 layer is printed conformally on flat or sloped ABS surfaces with a well-controlled thickness. The cavities and vertical interconnections (vias) between the layers are achieved by laser machining to cut through the ABS substrate to expose the bottom CB028 ground layer, as shown in Fig. 2(a) and (b), and then, the vias are filled by microdispensing CB028, as shown in Fig. 2(c) and (d). Laser-machined vias with high-aspect-ratio sidewalls were demonstrated with diameters as small as 100 μm, with a desired height-to-diameter aspect ratio of 1:1 to ensure that CB028 would fill the via without trapped air voids. However, for increased performance and repeatability, a 300-μm-wide via design with an aspect ratio of 1:3 was selected for the transmission-line development.

The postdeposition laser trimming step in the LE-DPAM process has several advantageous use cases, such as patterning features as small as 5 μm and achieving up to 100× enhancement of the printed trace conductivity due to the sintering of the silver particles in the silver paste [Fig. 3(a)–(c)] [2], [3]. It is observed that the laser beam at an IR wavelength of 1064 nm exhibits a stronger interaction with the silver paste than with the ABS, while the UV wavelength of 355 nm couples better with the ABS. With these attributes, the laser can be used to selectively remove certain layers with the bottom layer acting as an etch stop; this is exemplified in Fig. 2(a) and (b) with the via and cavity patterning that exposes

TABLE I

SUMMARY OF LASER PROCESSING PARAMETERS (RECIPE)

Structure	*Wavelength (nm)*	*Repetition Rate*	*Average Power (mW)*	*Stage Speed (mm/s)*
CPW	355	100 KHz	65	30
CPW	1064	100 KHz	2000	30
GCPW (thin substrate)	355	1 MHz	90	100
Cavity	355	100 KHz	10	20
Via	355	100 KHz	10	1

the bottom CB028 ground plane of the GCPW and microstrip. Since the laser spot size diameter is directly proportional to the wavelength, the 355-nm wavelength can also be used instead of 1064 nm to achieve significantly finer resolution due to its threefold reduction in laser spot size. This system produces a 5-μm spot size for the 355-nm wavelength compared to the 12–15-μm laser spot size of the 1064-nm wavelength. The smaller laser spot size results in smoother sidewalls and an improved aspect ratio of 6:1 over the 2:1 ratio achieved at 1064 nm, as shown in Fig. 3(a)–(c). It was also observed that the removal of some ABS during the laser cutting of the (G)CPW lines creates an overablated recess underneath the slots, which decreases the effective permittivity and loss tangent [2]. By varying the pulsed laser process parameters, the depth of the recess can be adjusted and this in turn modifies the effective permittivity [2]. The power, stage speed, and repetition rate during the laser processing were optimized for producing the best laser cuts to create the designed features with parameters summarized in Table I.

III. BROADBAND TRANSMISSION LINES AND (G)CPW-TO-MICROSTRIP TRANSITIONS

Following the fabrication process introduced in Section II, four ultrawideband transmission-line configurations have been investigated and characterized from dc to 110 GHz.

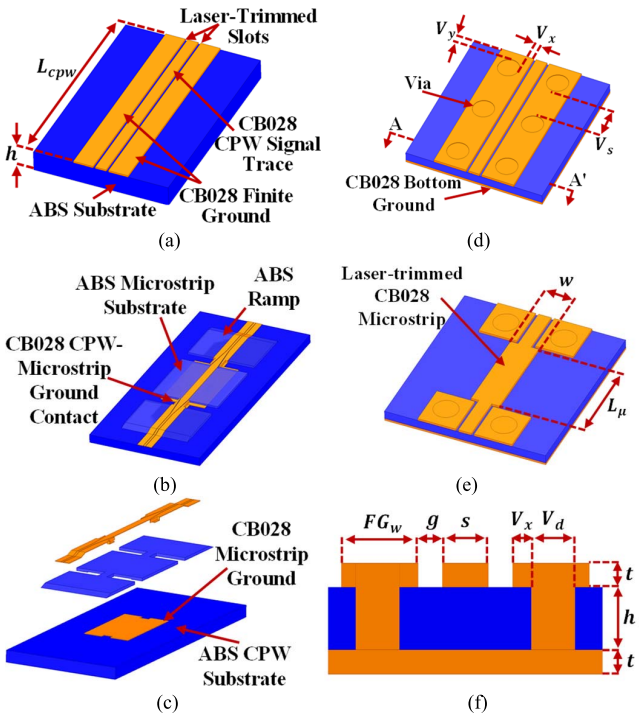

Fig. 4. Illustrations of four LE-DPAM transmission-line configurations. (a) CPW. (b) CPW-Microstrip-CPW. (c) Exploded view of CPWMicrostrip-CPW. (d) GCPW. (e) GCPW-Microstrip-GCPW. (f) A-A′ Cross-sectional view of GCPW.

Fig. 4 shows the LE-DPAM-fabricated CPW, GCPW, via-less CPW-to-microstrip transition, and GCPW-to-microstrip transition.

A. Transmission-Line Design Guidelines for Mm-Wave Operation

Transmission lines designed for W-band operation impose design restrictions for the key dimensions that often require tight fabrication tolerances to achieve optimal performance. Compared to the conventional CPW, the finite ground CPW (FG-CPW) exhibits a reduction in the width of the grounds to lower susceptibility to the excitation of higher order modes at mm-wave frequencies. This performance is achieved by keeping the ground plane width, FG_w, less than $\lambda_g/4$, where λ_g is the guided wavelength ($\lambda_o/\sqrt{\varepsilon_r}$) at the highest operating frequency [2], [55], thus avoiding resonances due to the finite width of the substrate and any in-package conductor walls that the transmission lines may be enclosed by. When FG_w is larger than twice the center conductor width, s, both the line attenuation (α) and the effective permittivity of the CPW become largely independent of the width of the grounds [2], [55]. To mitigate radiation losses and reduce dispersion, the upper limit of the ground width is designed to be less than $\lambda_g/8$. The sum of the two gap widths, g, and the center conductor width, s, is considered as the total linewidth of the CPW line, which should be kept smaller than $\lambda_g/4$ to suppress coupling to parasitic modes. The top FG-CPW conductors are printed by microdispensing of CB028 with a thickness, t, which can be precisely controlled by the distance between the microdispenser nozzle and the substrate to control the characteristic impedance of the CPW lines.

The GCPW and microstrip configurations add several new design constraints that increase the complexity of the design and fabrication. The substrate thickness, h, between the top and bottom conductors should not be larger than 100–150 μm to avoid exciting higher order modes and to reduce radiation losses [56]–[58]. Tighter control of h is also required due to the sensitivity of the characteristic impedance of GCPW and microstrip to the thickness. The GCPW via diameter, V_d, needs to be small to achieve compact designs while ensuring no trapped air voids in the silver paste inside the vias that can degrade high-frequency performance. To ensure operation up to 110 GHz, vias should be placed along the GCPW top grounds and spaced with a distance, V_s, no greater than $\lambda_g/4$ to avoid generating higher order modes due to leaked energy from the side ground [59]. In addition, to ensure proper RF grounding, the vias should be positioned as close as possible to the center conductor; the sum of h and the distance between the via and GCPW ground edges, V_x, should be less than $\lambda_g/4$ to prevent the grounds from acting as patch antennas and exciting higher order modes [59]. These design constraints result in dimensions much smaller than what can be readily achieved by microdispensing of the silver paste using the AM processes alone. Thus, the 355-nm picosecond-pulsed laser trimming is employed to achieve fine features as small as 5 μm with the desired dimensional accuracy.

B. Design and Fabrication of the Transmission Lines

A set of six different FG-CPW transmission lines with varying characteristic impedances based on the configuration shown in Fig. 4(a) have been designed and fabricated following the aforementioned guidelines [2]. Per the fabrication procedure discussed in Section II, a 0.5-mm-thick ABS substrate was first 3-D printed by FDM to provide structural support for subsequent layers as well as provide sufficient isolation from the metal probe chuck during high-frequency characterizations due to its dimension being much greater than the linewidths. The top FG-CPW conductors are printed by microdispensing CB028 with a thickness, t, varied between 15 and 80 μm, to achieve different characteristic impedances. By using the CPW laser processes in Table I, several transmission lines were fabricated by laser trimming to define the CPW slots, as shown in Fig. 5(a).

In addition, a novel via-less ultrawideband CPW-microstrip-CPW transition was designed and fabricated using a similar LE-DPAM process shown in Fig. 5(b). The design is shown in Fig. 4(b) and (c). The structure includes a CPW transmission line printed over a sloped ramp to transition to the targeted microstrip substrate thickness while maintaining a 50-Ω characteristic impedance. The CPW grounds are dropped to the bottom layer to connect to the microstrip ground, and the CPW signal line continues to transition into the microstrip. The structure then transitions back to CPW to complete the back-to-back transition. This results in a smooth structural and electromagnetic (EM) transition that minimizes radiation losses due to discontinuities and enables it to operate from dc to 110 GHz. This design can be used to embed an MMIC die within the microstrip substrate, where a laser machined

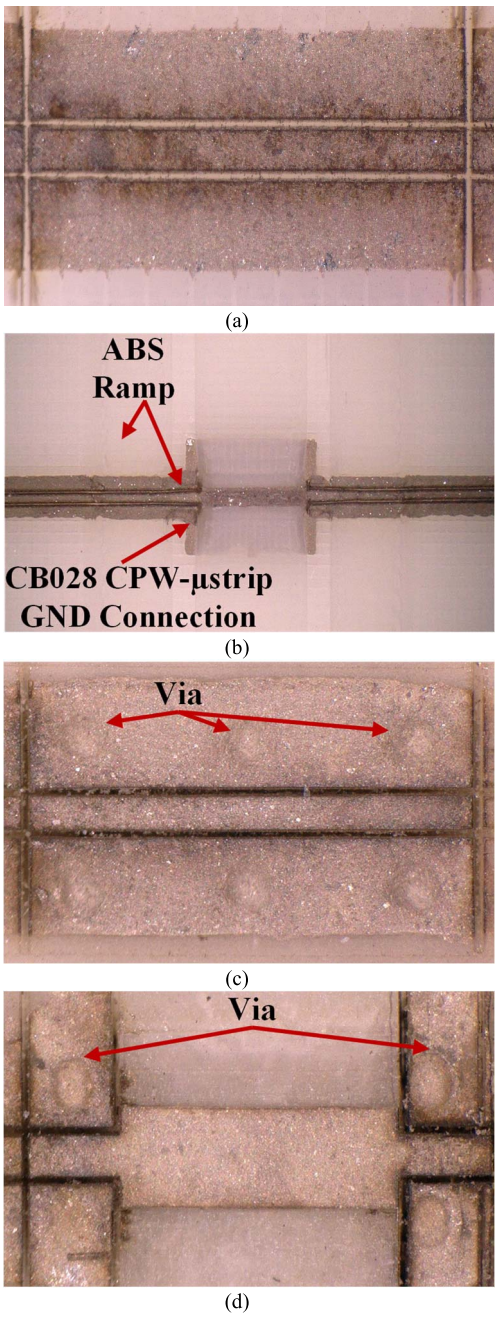

Fig. 5. Images of fabricated LE-DPAM transmission lines with key features specified. (a) 2-mm-long CPW. (b) 16-mm-long CPW-Microstrip-CPW. (c) 2.18-mm-long GCPW. (d) 2.18-mm-long GCPW-Microstrip-GCPW.

cavity is used to mount the MMIC to form a chip carrier. Also, it can be used to transition between different substrate thicknesses. The fabrication starts by printing a 0.5-mm-thick ABS substrate, followed by the printing of the 3 mm × 2 mm microstrip ground plane using a 15-μm-thick layer of CB028. Three different ABS sections are then printed, which include the sloped ramps and the 100-μm-thick microstrip substrate. A 30-μm-thick layer of CB028 is then microdispensed over the ABS sections to form the CPW and microstrip top conductors while simultaneously printing over the exposed bottom microstrip ground plane. This enables the CPW grounds to connect with the microstrip ground, as shown in the exploded view in Fig. 4(c). The top CB028 layer is separated into ground and signal traces to form the CPW transmission lines using laser milling, as shown in Fig. 5(b).

Finally, a dc-to-110 GHz GCPW transmission line and a GCPW-to-microstrip transition were designed and fabricated based on the configurations shown in Fig. 4(d)–(f). The fabrication starts by printing a 0.5-mm-thick carrier to serve as a structural support. A 15-μm-thick, large CB028 ground plane was then microdispensed and dried *in situ*. A swab with ABS dissolved in acetone (also known as ABS juice) is lightly applied to the dried ground conductor to improve its adhesion to subsequent layers. This step can be automated by using a spray print nozzle integrated into the nScrypt printer. A 100-μm-thick ABS layer was then printed as the substrate for the GCPW and microstrip transmission lines. Alignment fiducials and 300-μm-diameter vias were fabricated using the via process described in Section II and shown in Fig. 2(b) and (c). The filling of the vias and printing of the top 15-μm-thick conductor layer was then completed by microdispensing of CB028 during the same process step. Finally, the 355-nm wavelength laser was used to define the GCPW slots and adjust the microstrip widths, as shown in Fig. 5(c) and (d). The laser process was optimized by increasing the repetition rate to 1 MHz along with increasing the stage travel speed to 100 mm/s to circumvent excessive etching of the 100-μm-thick FDM printed ABS substrate underneath the top CB028 layer of the microstrip.

C. Transmission-Line Characterization

The transmission lines were characterized using a Keysight PNA-N5227A network analyzer and GGB 150-μm-pitch picoprobes at 0–67 GHz. Subsequently, measurements at 65–110 GHz were performed using 3742A-EW Anritsu *W*-band extenders and GGB 150-μm pitch picoprobes. The broadband frequency responses have a 2-GHz overlap between 65 and 67 GHz and were combined to ensure data consistency. A multiline thru-reflect-line (mTRL) probe tip calibration using a GGB CS-5 calibration substrate [60] was performed for both measurement sets. A 1-mm-thick glass slide was placed underneath the non-GCPW lines and the calibration substrate to avoid exciting microstrip modes at higher mm-wave frequencies by coupling to the metal chuck of the probe station. The effect of the 1-mm-thick glass plate on the non-GCPW was studied and no noticeable difference in measured frequency response was observed with and without the glass plate as a spacer. Fig. 6 shows the attenuation and return loss of the CPW, CPW-microstrip-CPW, GCPW, and GCPW-microstrip-GCPW configurations from dc up to 110 GHz. The transmission lines exhibit a return loss greater than 10 dB and a 0.30–0.77-dB/mm attenuation at 110 GHz that is on par with that of copper-clad microwave laminates and thin-film circuits made of low loss ceramic substrates such as alumina.

Equivalent circuit model parameters for these transmission lines (series resistance, R_{series}, inductance, L_{series}, shunt capacitance, C_{shunt}, and conductance, G_{shunt}) are shown in Table II. Even though the CPW lines have the larger R_{series}, GCPW and microstrip still exhibit higher losses especially at higher frequencies as the EM fields are more concentrated within

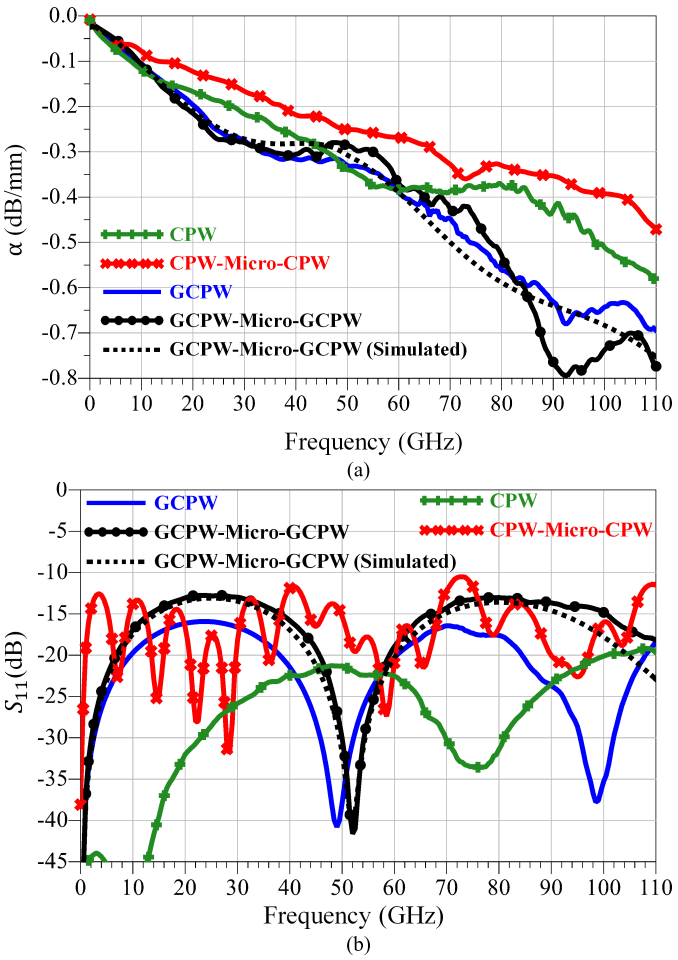

Fig. 6. Measured and simulated frequency responses of the LE-DPAM transmission lines. (a) Attenuation. (b) Return loss (S_{11}).

TABLE II
TRANSMISSION-LINE EQUIVALENT CIRCUIT PARAMETERS (110 GHz)

TL	R_{series} (kΩ/m)	L_{series} (nH/m)	G_{shunt} (S/m)	C_{shunt} (pF/m)
CPW	3.7	181	0.26	83
GCPW	2.3	225	1.2	81
Microstrip	1.2	243	1.57	88

the lossy ABS substrate material instead of the air due to the bottom ground conductor of the GCPW and microstrip as opposed to the CPW configuration. Therefore, the dielectric loss within the printed ABS substrate, G_{shunt}, has a higher impact on the total transmission-line attenuation than the effect of R_{series}, which is indicated by the significantly higher G_{shunt} for the GCPW and microstrip than that of the CPW.

The fabricated transmission lines were also used to extract the material properties using two 3-D EM models that were developed to simulate the broadband performance of the (G)CPW and microstrip transmission lines. The first model incorporates the physical characteristics and topographies of these transmission lines. This model ascribes different conductivities to the sintered slot edges and the rest of the conductor trace composed of dried silver paste while also accounting for the recess underneath the slots that are created by the

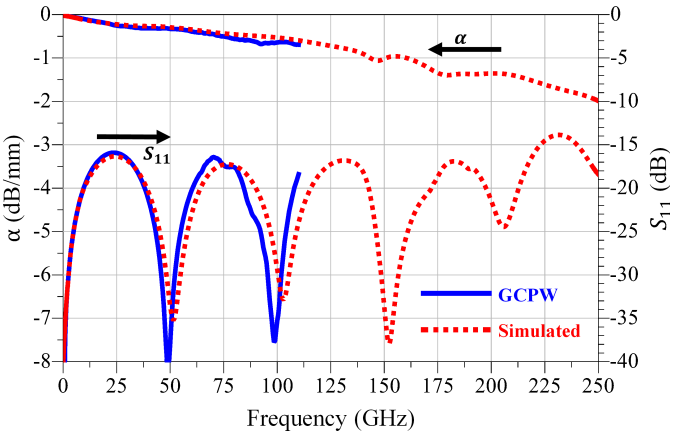

Fig. 7. Simulated and measured attenuation and return loss (S_{11}) for GCPW.

overablation of ABS during the laser cutting of the (G)CPW slots; details of the model are reported in [2]. A simplified EM model that is compatible with RF circuit schematic simulations was also developed. This model approximates the effective material properties of the LE-DPAM dielectric and conductors yet provides an accurate representation of the transmission-line performance. The extracted value for the effective conductivity of the transmission line's top metallization layers that includes both sintered and nonsintered regions was 5 MS/m. The conductivity of the bottom metallization layer and via remained at 2 MS/m, which is the same value used for the nonsintered regions in the initial model [2]. Meanwhile, the effective permittivity was determined to be 2 for the CPW and 2.35 for the GCPW and microstrip. In addition, the dielectric loss was modeled using the multipole Debye model for wideband operation. The effective loss tangent for the CPW is determined to be 0.006 and 0.01 at 10 and 80 GHz, respectively, while the GCPW and microstrip are determined to be 0.006 and 0.0275 at 10 and 80 GHz, respectively. The dielectric properties are dependent on the laser processes summarized in Table I. For example, the overablated recess of the CPW line is larger than those of the GCPW and microstrip transmission lines, thus resulting in smaller permittivity and loss tangent values since more EM fields are propagating in air as opposed to the lossy ABS substrate [2]. The results of Ansys HFSS simulations of this model performed for the GCPW-micro-GCPW transition are presented in Fig. 6. A close agreement between measured and simulated frequency responses is achieved for all transmission lines and transitions. Although the transmission lines were measured up to 110 GHz, simulations indicate that they can sustain mode-free operation up to at least 250 GHz as shown by simulated broadband characteristics of the GCPW in Fig. 7.

The transmission-line dimensions are summarized in Table III and compared to transmission lines reported by other prior works, for which the attenuation of the transmission lines is reported at 110 GHz or the highest measured frequency. To the best of our knowledge, the measured attenuation at 110 GHz in this work represents the best performance for additively manufactured planar transmission lines. In addition, the 110 °C sintering temperature is lower than most previously reported process temperatures for other AM technologies,

TABLE III
SUMMARY OF TRANSMISSION-LINE CHARACTERISTICS (ALL DIMENSIONS ARE IN MICROMETERS UNLESS OTHERWISE NOTED)

Work	Type	Zo (Ω)	s	g	FG_w	V_x	V_y	V_s	L_{CPW} (mm)	w	L_μ (mm)	h	t	Sinter Temp (°C)	Frequency (GHz)	Attenuation (dB/mm)	Process
This work	CPW	60	135	30	260	NA	NA	NA	2	NA	NA	500	25	110	110	0.30	Fully LE-DPAM using 355nm
	CPW	50	160	20	260	NA	NA	NA	2	NA	NA	500	25	110	110	0.59	Fully LE-DPAM using 355nm
	CPW-Micro	50	70	20	260	NA	NA	NA	6.5×2	245	3	100	30	110	110	0.47	Fully LE-DPAM using 1064nm
	GCPW	50	160	35	470	275	360	515	2.18	NA	NA	100	15	110	110	0.70	Fully LE-DPAM using 355nm
	GCPW-Micro	50	160	35	470	275	360	NA	0.52×2	265	1.14	100	15	110	110	0.77	Fully LE-DPAM using 355nm
[58]	CPW	50	50	25	230	NA	NA	NA	6.6	NA	NA	500	~2	NA	110	0.46	Gold on alumina PCB lithography
[35]	Thin-film Micro	55	NA	NA	NA	NA	NA	NA	NA	60	10	60	5	850	110	0.2	Advanced photoimageable thick-film and ceramic-based
[3]	CPW	50	300	20	1500	NA	NA	NA	1.5	NA	NA	380	25	90	40	0.38	LE-DPAM on Rogers RT5870 using 1064nm
[4]	CPW	70	102	30	360	NA	NA	NA	-	NA	NA	50	~2	140	110	0.37	AJP on LCP(3850HT)
[5]	CPW	50	~35	40	~120	NA	NA	NA	1	NA	NA	-	-	150	110	0.40	Inkjet on LCP(3850HT)
[6]	Micro	50	NA	NA	NA	NA	NA	NA	NA	51	2-6.6	20	2-3	172	110	0.50	Rapid micro-product development (RMPD)
[7]	GPCW-Micro	50	60	30	725	NA	NA	NA	0.5×2	70	1	~20	~2.6	120	100	0.65	Fully AJP

which allows the LE-DPAM technology to be utilized for low-temperature chip-carrier assembly or other device packaging applications.

IV. LE-DPAM LNA MMIC CHIP-CARRIER ASSEMBLY

A. Design and Fabrication

This section demonstrates an embedded *W*-band LNA using LE-DPAM to achieve a highly integrated, compact MMIC chip-carrier assembly that can be a viable replacement for current multilayer PCB technology to be utilized for multichip modules, as shown in Fig. 1. The LE-DPAM approach to packaging mm-wave MMIC dies is twofold: 1) conversion of the inductive chip-to-board interconnects to 50-Ω transmission lines and 2) achieving interconnect lengths shorter than 5 μm by laser milling a cavity in the substrate that is within 5-μm margin of the actual dimensions of the MMIC chip, as shown in the cross section of Fig. 8(i). To guarantee this tight tolerance, the lateral dimensions of MMIC chips are individually measured to account for manufacturing tolerances and used to define the geometry of the chip-carrier cavity on demand. This approach facilitates a chip-to-board interconnect length with minimal parasitic inductance and a tighter fit compared to traditional wire bonding techniques. The LE-DPAM fabrication process is inherently flexible and changes can be applied with minimal modification to other layers. For example, transmission lines can be printed before the MMIC assembly in order to support direct probing of both the transmission lines and the MMIC for testing purposes. Alternatively, the transmission lines and interconnects can be directly printed postassembly for a continuous, uninterrupted RF connection and to eliminate an additional process step. In addition, the GCPW/microstrip substrate layer can be fabricated to be the same thickness as the MMIC chip, thus avoiding additional via connections while providing a good heatsink for high-power applications.

Following the design and fabrication techniques of the GCPW-microstrip-GCPW transition as discussed in Section III, a 100-μm-thick, 3 mm × 2 mm commercial-off-the-shelf (COTS) *W*-band GaAs LNA chip from OMMIC (CGY2190UH/C2) [61] and a 450-μm-thick, 100 μm × 100 μm integrated wire-bondable 0.1-μF and 100 pF off-chip bypass capacitors are AM packaged [62]. The initial fabrication steps are similar to the GCPW-microstrip process, as shown in Fig. 8(a) and (b). During the via-hole laser-milling step, cavities of the same dimensions as the MMIC die and off-chip capacitors are laser-milled into the printed ABS substrate to expose the CB028 bottom ground plane, as shown in Figs. 2(a) and (b) and 8(c) and (d). The substrate thickness is selected to be 100 μm to match the thickness of the MMIC chip. EPO-TEK H20E conductive epoxy is used to attach the chip and off-chip capacitors to the exposed CB028 ground plane, as shown in Fig. 8(d). EPO-TEK 353ND dielectric epoxy is applied manually to seal the MMIC die to refill the surrounding air gaps to mitigate any potential short-circuit issues, as shown in Fig. 8(e) and (f); however, advanced 3-D printer models can automate this process due to greatly improved alignment accuracy down to 10 nm. The thermal-set epoxy is in liquid form when it is applied and is dried and solidified on the heated printer bed. Because of the low viscosity of the epoxy, it can conform within the gap between the IC die and the gap surrounding it with little chance of overflow between the IC die and cavity gap forming a flat surface when it is fully cured. The CB028 via fill, dc, and RF transmission lines are microdispensed using a 75-μm nozzle, while the interconnects between the MMIC and off-chip capacitors to the microstrip transmission line are deposited using a 50-μm diameter nozzle, as shown in Fig. 8(g). Finally, the GCPW slots and microstrip are

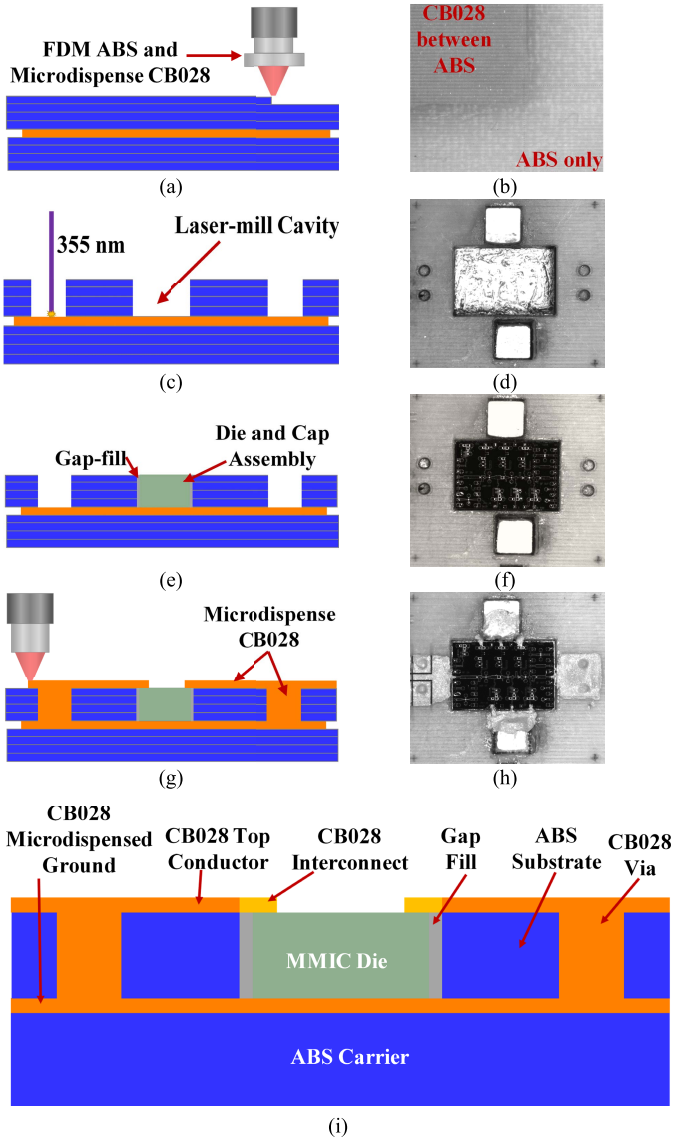

Fig. 8. LE-DPAM process used to package a W-band LNA. Left: cross-sectional illustration at different LE-DPAM stages. Right: top views of the packaged LNA. (a) FDM ABS carrier, microdispense ground, and FDM ABS 100-μm-thick substrate. (b) CB028 ground situated between ABS carrier and 100-μm-thick substrate. (c) Laser-milling cavity/via. (d) Laser-milled via and cavity, chip cavities prepared with epoxy, and assembled bypass capacitors. (e) and (f) Die assembled and gaps are filled. (g) Microdispensing TL/interconnects and via with CB028. (h) Laser-trimming GCPW slots and microstrip. (i) Final cross-sectional view of the assembled W-band LNA.

laser milled to ensure width accuracy. The RF chip-to-board interconnect microstrip width is 70 μm in order to maintain a 50-Ω characteristic impedance up to the probe pad on the GaAs MMIC die. Fig. 9 shows the 5.2 mm $\times$ 4.6 mm LE-DPAM fabricated W-band LNA MMIC chip-carrier assembly.

B. Measurement Results

The W-band chip-carrier assembly was characterized using a similar measurement setup as described in Section III with the exception of increasing the internal attenuator at the input to 40 dB to avoid gain compression of the active device since the 65–110 GHz extenders have an output power of

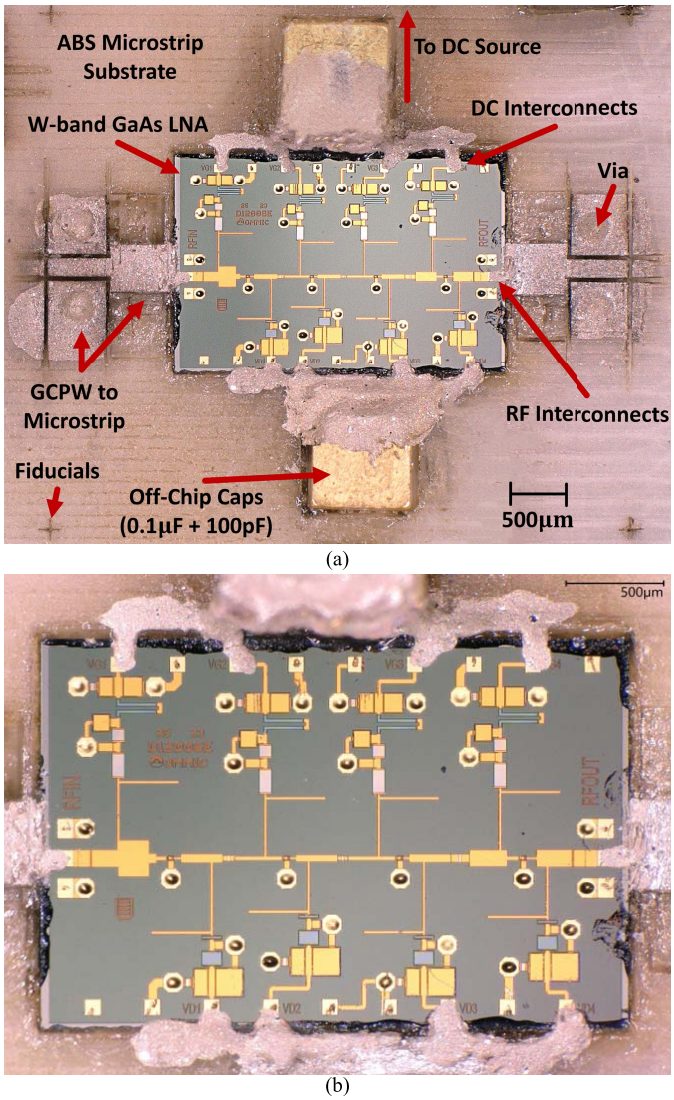

Fig. 9. (a) Fabricated 5.2 mm $\times$ 4.6 mm W-band LE-DPAM packaged LNA. (b) Zoomed-in image showing the LE-DPAM RF and dc interconnects.

10 dBm. After full mTRL calibration, the reference plane of the measurement is positioned after the attenuator and at the tip of the W-band probes. To characterize the performance of the chip-carrier assembly, the bare LNA die was RF-probed prior to packaging as a baseline measurement and showed similar frequency responses to the manufacturer's datasheet [61]. Finally, the full LE-DPAM chip carrier is RF-probed to measure the frequency responses up to 110 GHz. For both measurements, the die was biased at a drain voltage, gate voltage, and drain current of 1 V, 0.2 V, and 33 mA, respectively. All the measured results are shown in Fig. 10.

The measured frequency response of the AM embedded LNA shows an improved return loss over the bare die, where S_{11} and S_{22} are better than -7.25 and -9 dB, respectively, for the full 65–110-GHz frequency range, which is comparably better than -4.75 and -3.35 dB, respectively, for the bare MMIC chip. The gain of the chip-carrier packaged MMIC LNA follows the same pattern as the gain of the bare die and exhibits a maximum gain of 24.3 dB. The difference in the measured gains of the bare die and embedded die is plotted

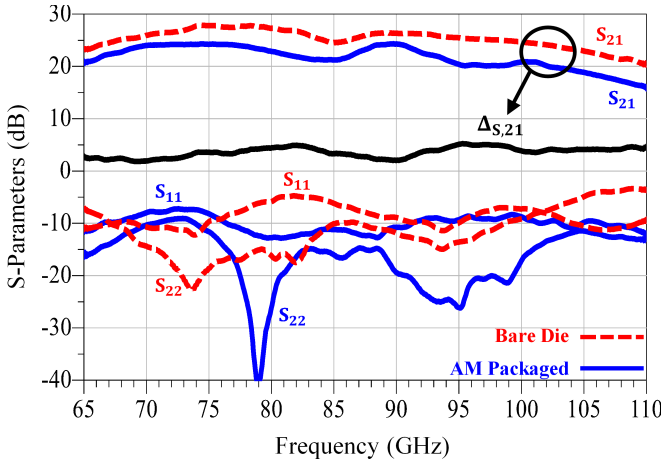

Fig. 10. S-parameter response for the chip-assembled *W*-band LNA compared with the S-parameters of the RF probed bare *W*-band LNA die. $\Delta_{S,21}$ is the measured gain difference between the AM assembly chip and bare die.

as $\Delta_{S,21}$ in Fig. 10, which is between 1.74 and 5.2 dB for the full frequency range. The reverse isolation, $S_{12,}$ for both measurements is greater than 40 dB.

To facilitate understanding the effect of the chip-to-board transitions, identical GCPW-microstrip-GCPW transmission lines have been fabricated and characterized without a cavity-embedded IC die as discussed in Section III, in Figs. 4(e) and (f) and 5(d). Also, the measured and simulated responses are presented in Fig. 6 to estimate the contribution of the chip-to-board interconnection. The insertion loss of the identical design of GCPW-microstrip-GCPW transmission lines without a cavity embedded IC chip ranges between 0.87 and 1.74 dB across the 65–110-GHz range. As shown in Fig. 10, the loss $\Delta_{S,21}$ of 1.76 dB at 90 GHz includes contributions by the transmission-line and chip-to-board interconnects. According to Fig. 6, the total loss of the GCPW-microstrip-GCPW transition at 90 GHz is 1.70 dB. This indicates that the total loss contributed by just the chip-to-board interconnects at both input and output ports of the LNA chip is only 0.06 dB, which suggests only 0.03-dB loss per chip-to-board interconnect transition. The variation in insertion loss and return loss of the interconnects can be attributed to the parasitic capacitance and inductance introduced by the nonoptimized GSG-launch to microstrip transition as well as the abrupt geometrical change (i.e., width) of the 50-Ω microstrip line over the printed chip carrier and the chip-to-board interconnects. The chip-to-board interconnects were also off-centered due to the utilization of the same chip carrier to test different MMIC dies that also contribute to the variation. The discrepancies observed are also attributed to geometric imperfection due to the fabrication tolerances. Future work can reduce the parasitic capacitance and inductance by optimizing the GSG launches and printing a centered microstrip interconnect with gradual changes in the width to form tapered microstrip to interconnect the transmission line on the board to the pads on the chip. In addition, for a more robust connection, we can utilize GCPW instead of microstrip configuration for the chip-to-board interconnects.

TABLE IV
COMPARISON WITH OTHER CHIP-TO-BOARD INTERCONNECTS

Work	Die	Process	Total Package Loss	Chip-to-board Interconnect Loss	Frequency
This work	GaAs LNA	Fully LE-DPAM using 355nm	1.76 dB	0.54 dB/mm	90 GHz
[20]	GaAs LNA	Fully LE-DPAM using 1064nm	2.4 dB	0.2 dB/mm	20 GHz
[21]	GaAs PA	Fully AJP	1 dB	0.33 dB/mm	15 GHz
[22]	GaAs 0-dB	Fully AJP	1 dB	0.49 dB/mm	60 GHz
[23]	GaAs TL	AJP with LTCC	2 dB	0.8 dB/mm	140 GHz
[24]	GaAs LNA	Fully Inkjet	1.9 dB	1.3 dB/mm	40 GHz
[39]	InP LNA	V-shaped Wirebond LCP	3.8 dB	0.63 dB/mm	110 GHz
[51]	CMOS Chip	Flip-chip	0.95 dB	10 dB/mm*	94 GHz

**Flip-chip bumps are typically ~100 um-long, yielding ~1 dB loss per transition.*

In recent years, there have been several promising AM chip packaging techniques that exhibit excellent performance. Many of these AM IC chip assembly packages operate under 67 GHz using technologies, such as AJP [21], [22], [26], inkjet printing [24], [25], and LE-DPAM/DPAM printing [19], [20]. Meanwhile, AM processes have been used as a supplement to conventional packaging [27], [28]. AM IC chip assembly packaging has also been used for frequencies higher than 67 GHz, including all-in-polymer MCM process at *D*-band [6], *W*-band chip assembly with on-chip antenna using inkjet printing [63], the 225-GHz AJP chip interconnects with a low-temperature co-fired ceramic (LTCC) substrate [23], and AM used as a supplemental process technique [13]. Table IV compares this work's LE-DPAM's chip-carrier assembly technique with other cost-effective multilayer MCM chip-to-board technologies. The chip-carrier package improves the return loss of the LNA and exhibits a minimum of 0.03-dB loss per interconnect transition. The gap width between the chip-carrier host substrate and the MMIC chip embedded within the cavity is less than 5 μm due to the customized and laser-machined cavity dimensions. To the best of our knowledge, this is the first ever fully AM MMIC chip carrier that operates up to 110 GHz. These results lay a solid foundation for multichip modules.

Depending on design requirements and the inherent design/fabrication flexibility enabled by AM technologies, this fabrication process can be altered by applying slight design modifications such as using a GCPW chip-to-board interconnect configuration instead of microstrip to connect with the ground probe pads on the die or printing the 100-μm-thick GCPW/microstrip substrate directly over a heatsink carrier instead of the 0.5-mm-thick ABS carrier substrate. Also, the off-chip bypass capacitors [62] can be replaced by LE-DPAM fabricated on-package capacitors. Even though a fully additively manufactured chip-carrier assembly of the *W*-band

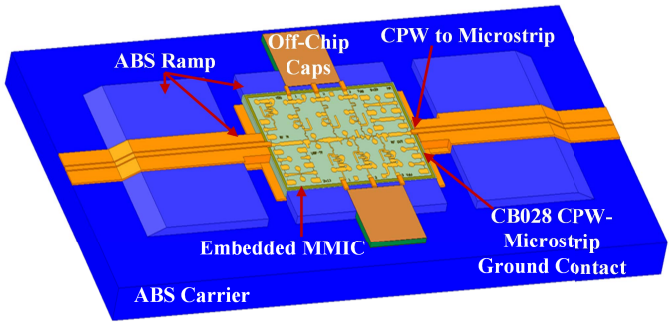

Fig. 11. Illustration for an alternative LE-DPAM chip-embedding scheme using CPW-micro-CPW transition design.

MMIC as shown in Fig. 9 has adopted the GCPW-microstrip-GCPW configuration [Fig. 5(d)] that levels the MMIC die with the substrate, the chip assembly could also be implemented using an alternative CPW-microstrip-CPW configuration as shown in Fig. 5(b), where the transmission line is instead brought to the same level as the die, as shown in Fig. 11.

V. Discussion

In addition to providing a high-performance and simplified packaging technology of MMIC chips that can operate up to 110 GHz, we envision that the fabrication and testing can all be encompassed under one hood over a fully automated platform without removing the MMIC chip from the stage. This is one of the key advantages over traditional multistep fabrication methodologies, which often rely on photomasking, deposition, lithography, and etching and require several tools and wet/dry etching processes. LE-DPAM also enables direct 3-D printing and test-on-demand capabilities to realize a range of customized parts that can be mass-produced economically, therefore reducing the development time of a concept to final products from weeks to just hours. The LE-DPAM fabrication approach presented already includes the whole fabrication process by using a single automated platform, where the printing of the dielectric, conductors, curing/drying, sintering, and laser milling are performed without removing the sample off the LE-DPAM tool stage. A future implementation can automate the pick-and-place process as well as incorporate RF testing probes, where the stage can move to the testing region for RF probing of the chip and final package, which would be valuable for rapid prototyping or quality assurance during mass production.

VI. Conclusion

The first ever fully AM MMIC chip carrier that operates up to 110 GHz has been successfully demonstrated by using the LE-DPAM technology. Simulations indicate that the MMIC chip-carrier package can sustain mode-free operation up to at least 250 GHz. The design and packaging methodology provides a low-cost, versatile yet simple on-demand approach to package wideband MMICs using a fully automated platform. The print-on-demand capability demonstrates the flexibility of the technology to fabricate multimaterial conformal layers while embedding MMIC chips to replace ribbon bonding with lower parasitic effects, thus offering performance better than ribbon-bonding and allowing a tight fit for the MMIC chips in a highly integrated package. By removing the ribbon bonds or bond wires, this LE-DPAM packaging approach for the cavity-embedded MMICs also leads to better mechanical robustness. LE-DPAM is highly scalable and can be utilized for medium-to-high volume manufacturing. The technique can also accommodate the usage of high permittivity, high glass transition temperature materials of superb chemical inertness to be adapted for harsh environments. The technology presented here can be extended for a full front-end module, including on-package antennas for 5G and high mm-wave applications.

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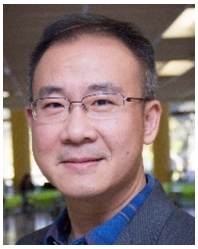

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