A Closed-Loop Current Source Gate Driver with Active Voltage Balancing Control for Series-Connected GaN HEMTs

Zhengda Zhang, Chunhui Liu, Yunpeng Si, Yifu Liu, Mengzhi Wang and Qin Lei
School of Electrical, Computer and Energy Engineering
Arizona State University
Tempe, Arizona, USA
zzhan235@asu.edu

2021 IEEE Energy Conversion Congress and Exposition (ECCE) | 978-1-7281-5135-9/21/$31.00 ©2021 IEEE | DOI: 10.1109/ECCE47101.2021.9595419

***Abstract*—The voltage rating of the commercial Gallium Nitride (GaN) power devices are limited to 600/650 V due to the lateral structure. Stacking the low-voltage rating devices is a straightforward approach to block higher dc-link voltage. However, the unbalanced voltage sharing can occur due to the discrepancies in the gate driving loops, the device parameter tolerance and the device-to-ground displacement currents for the series-connected devices in the stack. In this paper, a novel closed-loop current source gate driver is proposed, which addresses the voltage imbalance issue of series-connected GaN HEMTs for both hard switching and soft switching scenarios. The proposed current source gate driver controls the device switching timing and the dv/dt with fine accuracy by directly regulating the device gate current. Without the employment of the lossy snubber circuit or the external Miller capacitor, the switching energy and the switching speed are almost not compromised for each individual device. Meanwhile, the closed-loop strategy improves the adaptivity to different operating conditions. A series-connected GaN-based multiple pulse tester is built to validate the proposed current source gate driver and the voltage balancing strategies in different switching scenarios.**

***Index Terms*—Gallium nitride, HEMTs, stacking, closed-loop, current control, driver circuits, parasitic capacitance, switching loss.**

I. Introduction

Gallium Nitride (GaN) power devices offer low specific on-state resistance, fast switching-speed and high operating temperature capabilities compared with Silicon (Si) counterpart. All of these are beneficial for the efficiency, power density, specific power, as well as the reliability of power electronics converters [1]. Though Silicon Carbide (SiC) excels in high-temperature applications, the material characteristics of GaN are superior in high-efficiency, high-frequency converters [2]. Meanwhile, cost reduction of GaN devices will progress faster than for SiC devices due to significant lower substrate costs and Si-CMOS manufacturing line compatibility [3]. The highest voltage rating of the commercial GaN HEMTs is typically at 600/650 V level, due to their lateral structure. The vertical GaN devices are considered to have higher voltage rating, but they have not yet been produced on a commercial level. The insufficient voltage rating of GaN HEMTs hinders their appliance in higher dc-link systems, such as 800 V battery electric vehicles (EV) and medium voltage (MV) applications.

Stacking converters and stacking switches are the two most common approaches to block higher dc link voltage. The cascaded H-bridges and multilevel converters can be categorized as the stacking converter solution. The advantages of this solution include lower dv/dt, lower EMI and lower output harmonics. However, the complexity of hardware structure as well as the control scheme are greatly increased for this solution. Stacking switches is much simpler in terms of the hardware structure and control scheme. The biggest challenge is to prevent the over-voltage breakdown for each individual low-voltage switch in the stack. Some researchers have been working on the topic of series-connected fast-switching devices (GaN and SiC). In [4], a 1.2 kV super-cascode GaN transistor is demonstrated, which is based on two series-connected depletion-mode GaN. The structure has the same drawbacks as the typical cascode GaN, such has the undesired voltage sharing between the low-voltage Si MOSFET and the depletion-mode GaN during the switching transient and large parasitic inductance in the package due to the multiple dies. In [3], a 1.2 kV GaN transistor is made up by the series connection of a enhancement-mode GaN transistor and a depletion-mode GaN transistor. However, the device parameter mismatch can be severe for the two different type of GaN devices and no discussion is made on the dynamic voltage sharing of the two devices. An integrated gate driver circuit is proposed in [5] to solve the issue of voltage imbalance for series-connected enhancement-mode GaN devices and a detailed mathematical model is developed as well. However, the circuit parameters need to be carefully tuned to achieve the desired switching timing for the series-connected devices, which makes this method very sensitive to the variance in the operating conditions, such as load current, dc link voltage and temperature. In [6], a current mirror is in series with a large extra Miller capacitor to serve as a controllable extra Miller capacitor. The drain-to-source dv/dt of each device can be regulated to achieve well-balanced voltage sharing. However, this strategy is only suitable for the devices with large input capacitance, such as high current rating power modules and Si devices, in which the turn-off dv/dt is determined by the charging speed of the Miller capacitance. For the discrete wide-

band-gap (WBG) devices, the input capacitance is significantly smaller. During the turn-off transient, the input capacitance can be discharged below the threshold before the drain-to-source voltage starts to rise. In other words, during the dv/dt transient, the device channel can be already cut off and the device can be regarded as a junction capacitor. The value of the extra Miller capacitor needs to be dominant in the output capacitance (C_{oss} = C_{gd} + C_{ds}) in order to regulate the dv/dt. The large extra Miller capacitor will significantly slow down the dv/dt of the switch and more switching energy will be produced during the switching transient. Meanwhile, the extra Miller capacitor will make the gate driving loop more sensitive to the dv/dt and ringings in the power loop. To sum, a practical strategy for solving the voltage imbalance issues in series-connected GaN devices is lacked in the existing literatures.

The current source gate driver is employed in [7], [8] to address the voltage imbalance issues for series-connected fast-switching devices. Since the device gate current is directly controlled, the device switching timing and dv/dt can be regulated with fine accuracy. However, no closed-loop implementation is included in these studies, so the adaptivity to different operating conditions is not validated yet for the current source gate driver. In this paper, a novel closed-loop current source gate driver is presented. With the direct and precise regulation of the device gate current, the drain-to-source voltages of the switches in the stack can always be roughly equalized for both soft switching and hard switching scenarios. Sufficient experimental tests have been conducted to verify the performance of the proposed current source gate driver in a variety of operating conditions. The rest of the paper is organized as follows. Section II reviews the root causes of the unbalanced voltage sharing in different switching scenarios. Section III presents the operating principles of the proposed closed-loop current source gate driver and the novel adaptive voltage balancing schemes. Section IV demonstrates the experimental verification. Finally, Section V concludes this paper.

II. Review of the Root Causes for the Unbalanced Voltage Sharing

As mentioned in the introduction, the unbalanced voltage sharing can be caused by: 1) the discrepancies in the gate driving loops; 2) the device parameter tolerance; 3) the device-to-ground displacement currents for the series-connected devices in the stack. For the discrepancies in the gate driving loops, it can be alleviated by using symmetrical connections and circuit layouts for the series-connected switches in the stack. For the device parameter tolerance, it can be overcome by adding small external gate-to-source/drain-to-source capacitors. For the device-to-ground displacement current, however, it is hard to be passively compensated, because the device-to-ground parasitic capacitance is typically unknown. Therefore, the active compensation mechanism should be employed. Basically, the major task in this study is to actively compensate the voltage imbalance caused by the device-to-ground displacement currents.

The effect of the device-to-ground parasitic capacitance on the dynamic voltage sharing for the series-connected devices have already been discussed in the previous studies [6], [9], [10]. It is still necessary to make a summary of the effect in different switching scenarios, because it is the precondition of the proposed voltage balancing schemes.

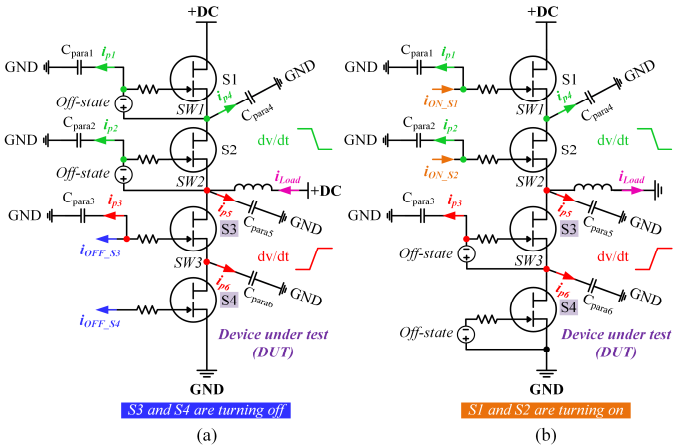

Fig. 1. (a) Device-to-ground displacement currents during the lower arm switches (DUT) 'soft' turn-off transient. (b) Device-to-ground displacement currents during the lower arm switches (DUT) 'hard' turn-off transient.

A. 'Soft' Turn-Off Scenario

As is shown in Fig. 1(a), two GaN switches are connected in series for both upper arm and lower arm in a phase-leg. The upper arm switches (S_1 and S_2) are in the gate-off state, and the lower arm switches (S_3 and S_4) are actively turning off. The lower arm switches are regarded as the device under test (DUT). Since the load current will assist the charging/discharging of the device junction capacitances during this transient, the lower arm switches (S_3 and S_4) are experiencing 'soft' turn-off process. For the 'soft' turn-off scenario, the device drain-to-source dv/dt can be restricted by either the device gate current (i_{gate}) or the device drain current (i_{drain}) [8], as illustrated in the following equation:

$$\begin{aligned} i_{gate} &\geq C_{gd}\frac{dV_{ds}}{dt} \\ i_{drain} &\geq (C_{gd}+C_{ds})\frac{dV_{ds}}{dt} \end{aligned} \tag{1}$$

where C_{gd} is the device gate-to-drain capacitance (Miller capacitance) and C_{ds} is the device drain-to-source capacitance.

For the devices with large input capacitance, such as the conventional Si devices and SiC power modules, the device drain-to-source dv/dt is typically restricted by the gate current during the 'soft' turn-off transient. Most of the gate driver supplied current is utilized to charge the Miller capacitance during the rising dv/dt transient. However, for the devices with small input capacitance, such as discrete WBG devices (SiC and GaN) or even Si super-junction MOSFETs, the device drain-to-source dv/dt is typically determined by the drain/load current during the 'soft' turn-off transient. With

the excessive gate driver supplied current, the device gate-to-source capacitance (C_{gs}) will be quickly discharged below its threshold. Therefore, the device channel is already cut off before its drain-to-source voltage starts to rise. Then the device becomes an equivalent junction capacitor, and the charging speed of the junction capacitor is determined by the drain/load current amplitude [8]. This fast turn-off property is beneficial for reducing the device turn-off energy, because the overlapping between the device drain-to-source voltage and current is minimized. The extremely fast turn-off process of the discrete WBG devices is also referred as the nearly 'lossless' turn-off in [11].

However, as mentioned earlier, due to the existence of the device-to-ground parasitic capacitances, the actual gate current and drain current of the series-connected switches are different even with well-matched gate driving and device parameters. The device gate-to-ground parasitic capacitances are labeled as C_{para1}, C_{para2} and C_{para3} in Fig. 1. In the real system, the gate-to-ground parasitic capacitances consist of the isolation capacitance of the isolated DC/DC power supplies, the isolation capacitance for the isolated gate drivers and the device gate to heat sink parasitic capacitance (if the heat sink is grounded). The device drain/source-to-ground parasitic capacitances are labeled as C_{para4}, C_{para5} and C_{para6} in Fig. 1. In the real system, the major drain-to-ground parasitic capacitance comes from the PCB interlayer capacitance for the discrete devices. For the fast-switching GaN-based power converters, the flux-cancellation PCB layout techniques are usually employed to reduce the power loop parasitic inductance. To achieve the flux-cancellation between the switching nodes and the power ground, they are normally placed in the two adjacent layers of a PCB and overlapped pretty well. If the overlapping area between the switching node and the power ground is assumed to be only 10 mm$\times$10 mm, the interlayer stray capacitance will be around 30 pF, which is already significant compared with the junction capacitance of the discrete GaN devices.

Based on Fig. 1(a), the gate currents of S_3 and S_4 can be written as:

$$\begin{aligned} i_{\text{gate(S3)}} &= i_{\text{OFF(S3)}} + i_{\text{p3}} \\ i_{\text{gate(S4)}} &= i_{\text{OFF(S4)}} \end{aligned} \tag{2}$$

where $i_{\text{OFF(S3)}}$ and $i_{\text{OFF(S4)}}$ are the gate driver supplied turn-off currents for S_3 and S_4, respectively; i_{p3} is the gate-to-ground displacement current for S_3.

Meanwhile, due to the existence of the drain/source-to-ground displacement currents, the relation between the drain currents of S_3 and S_4 can be expressed as:

$$i_{\text{drain(S3)}} = i_{\text{drain(S4)}} + i_{\text{p6}} \tag{3}$$

where i_{p6} is the drain-to-ground displacement current for S_4.

It is clear that S_3 has both higher gate current and higher drain current than S_4 does. As discussed earlier, the drain-to-source dv/dt is typically determined by the drain/load current for the discrete GaN devices. If no compensation mechanism is implemented, the top-sitting switch S_3 will have higher dv/dt than the bottom-sitting switch S_4 does due to the bigger drain current, which can eventually cause the over-voltage breakdown. The proposed current source gate driver can properly regulate the gate driver supplied turn-off currents [$i_{\text{OFF(S3)}}$ and $i_{\text{OFF(S4)}}$] to precisely adjust the drain-to-source rising voltage starting timing to compensate the difference in the slew rate. In this way, the well-balanced voltage sharing among the series-connected switches can be obtained. The detailed voltage balancing scheme in the 'soft' turn-off scenario will be presented in Section III.

B. 'Hard' Turn-Off Scenario

As is shown in Fig. 1(b), the upper arm switches (S_1 and S_2) are actively turning on, and the lower arm switches (S_3 and S_4) are in the gate-off state. Since the load current will not assist the discharging of the junction capacitances of the upper arm switches, the upper arm switches (S_1 and S_2) are experiencing 'hard' turn-on. Meanwhile, the drain-to-source voltage of the lower arm switches (S_3 and S_4) will be forcedly pulled up. Therefore, the lower arm switches (S_3 and S_4) can be regarded as experiencing 'hard' turn-off.

Since the lower arm switches are already in the gate-off state during this transient, the dv/dt will be determined by the drain current from the dc-link. Based on (3), the top-sitting switch (S_3) has higher drain current than the bottom-sitting switch (S_4) does due to the existence of the drain-to-ground displacement current. Therefore, the top-sitting switch (S_3) will have higher dv/dt than the bottom-sitting switch (S_4) does, which can eventually cause the over-voltage breakdown. This phenomenon is also referred as the voltage imbalance of series-connected body-diodes in [9]. Actually, this issue is very hard to solve from the gate side with the conventional voltage source gate driver, because the gates are already in the off state for the switches with the rising drain-to-source voltage. The proposed current source gate driver can trigger the gate of the switch that has higher dv/dt for a very short period of time during the complementary switches 'hard' turn-on transient by precisely regulating its gate current. Since the other switches in the stack are still in the gate-off state, the dc-link shoot-through will not happen. In this way, the impedance of that triggered switch is decreased, so its average dv/dt is reduced and the well-balanced voltage sharing can be obtained. The detailed voltage balancing scheme in the 'hard' turn-off scenario will be presented in Section III as well.

It should be mentioned that the device-to-ground displacement currents also affect the slew rate of the falling drain-to-source voltages for the turn-on switches. As long as the turn-on timing is very synchronized for all the switches in the stack, the over-voltage breakdown is unlikely to occur during the turn-on transient. However, if there is several nanosecond turn-on timing difference among the series-connected switches, the over-voltage can still occur [12]. The drain-to-source voltage of the delayed turn-on switch will start to rise at first until its gate-to-source voltage reaches the turn-on threshold. Therefore, it is still very critical to guarantee the consistency of the gate driving circuits for different switches in the stack [8].

III. Operating Principles of the Proposed Closed-Loop Current Source Gate Driver

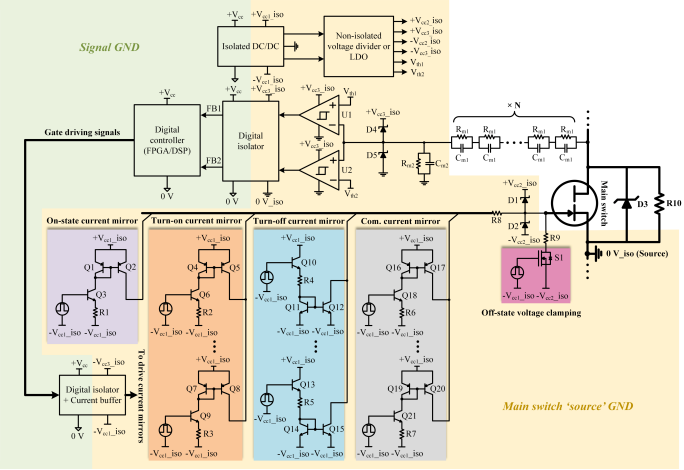

Fig. 2. Schematic of the proposed closed-loop current source gate driver.

A. Hardware Architecture

The schematic of the proposed closed-loop current source gate driver is shown in Fig. 2. The detailed operating principles of each part are introduced as follows.

1) Current mirror circuits: The current mirror circuits are utilized as the fast-responded, discontinuous current sources. Four sets of current mirror circuits are included in the proposed current source gate driver: the turn-on current mirror circuit; the turn-off current mirror circuit; the compensation current mirror circuit and the on-state current mirror circuit, which is only required for GaN gate injection transistor (GIT).

The turn-on gate current (i_{ON}) from each current mirror circuit can be calculated as (taking the Q_4-Q_5-Q_6 current mirror as an example):

$$i_{\mathrm{ON}} = \frac{V_{\mathrm{drive(on)}} - V_{\mathrm{BE}}}{R_2} \tag{4}$$

where $V_{\mathrm{drive(on)}}$ is the driving voltage across Q_6 and R_2; V_{BE} is the base-to-emitter voltage drop for the BJTs (around 0.7 V).

Similarly, the turn-off gate current (i_{OFF}) from each current mirror circuit can be calculated as (taking the Q_{10}-Q_{11}-Q_{12} current mirror as an example):

$$i_{\mathrm{OFF}} = \frac{V_{\mathrm{drive(off)}} - 2V_{\mathrm{BE}}}{R_4} \tag{5}$$

where $V_{\mathrm{drive(off)}}$ is the driving voltage across Q_{10}, R_4 and Q_{11}.

The compensation current amplitude and on-state current amplitude can be calculated by (4) as well. The compensation gate current is used to counteract the voltage imbalance caused by the device-to-ground displacement current. The detailed compensation mechanism will be discussed later in this paper. It should be mentioned that different level current mirrors can be paralleled to provide the multilevel turn-on, turn-off and compensation gate currents.

2) Voltage clamping circuits: One of the concerns for the current source gate driver is the effective gate voltage clamping during the steady off-state or on-state due to the lack of the voltage source. The breakdown voltage of the Zener diode can be used to sustain the desired off-state or on-state gate-to-source voltage. However, it is found that the Zener diode clamping can not guarantee the stable off-state or on-state gate-to-source voltage in [8]. For the proposed current source gate driver, the isolated power supply is still needed for powering the secondary side current mirror circuits, so the power supply can be directly used for clamping the gate voltage. As is shown in Fig. 2, during the off-state, the low-voltage MOSFET S_1 will be turned on to clamp the gate-to-source voltage to the desired off-state voltage ($-V_{\mathrm{cc2\_iso}}$). The resistor R_9 is used to limit the pulse current amplitude flowing through S_1. It should be mentioned that the active on-state voltage clamping is not needed for GaN GIT, because its on-state gate-to-source voltage is determined by the on-state gate current amplitude. As long as the on-state current mirror has the stable output, the on-state gate-to-source voltage of the GaN GIT will be steady. However, the active on-state gate voltage clamping should be employed for the voltage-driven p-gate GaN to achieve the stable on-state voltage. Meanwhile, the off-state/on-state active voltage clamping is only kicked in during the steady off-state/on-state. The device gate current during the switching transients is still supplied by the current mirror circuits, so the gate driver is still based on the controllable current sources. Moreover, the Schottky diodes D_1 and D_2 are utilized to suppress the gate-to-source voltage overshoot and undershoot during the switching transients.

3) Sensing circuit and the window comparator: The voltage divider circuit is employed to sense the device drain-to-source voltage during the steady off-state. The pure resistive voltage divider is found to have slow transient response, so the capacitive voltage divider is also employed [6], [13]. As is shown in Fig. 2, the sensed drain-to-source voltage is the input for the window comparator. The window comparator has two thresholds (V_{th1} and V_{th2}), which indicate the desired off-state drain-to-source voltage range. The upper threshold V_{th1} represents the upper limit of the desired voltage range, while the lower threshold V_{th2} reflects the lower limit of the desired voltage range. If the desired voltage sharing is $\pm 10\%$ of the average voltage, the two thresholds can be expressed as:

$$\begin{aligned} V_{\mathrm{th1}} &= \frac{R_{\mathrm{m2}}}{N \cdot R_{\mathrm{m1}} + R_{\mathrm{m2}}} \cdot \frac{V_{\mathrm{dc}}}{M} \cdot 110\% \\ V_{\mathrm{th2}} &= \frac{R_{\mathrm{m2}}}{N \cdot R_{\mathrm{m1}} + R_{\mathrm{m2}}} \cdot \frac{V_{\mathrm{dc}}}{M} \cdot 90\% \end{aligned} \tag{6}$$

where V_{dc} is the dc-link voltage; N is the number of the paralleled R_{m1} and C_{m1} branches and M is the number of the series-connected main switches.

The output states of the window comparator is summarized in Table I. The digital isolator is employed to transfer the outputs of the window comparator to the digital controller on the primary side. Based on the states of the two feedback

TABLE I
OUTPUT STATES OF THE WINDOW COMPARATOR

Input	U_1 output	U_2 output	Voltage sharing
$V_{sense} < V_{th2}$	'1'	'0'	Under-voltage
$V_{th2} < V_{sense} < V_{th1}$	'1'	'1'	Desired voltage range
$V_{sense} > V_{th1}$	'0'	'1'	Over-voltage

signals (FB1 and FB2), the controller will implement the appropriate tuning algorithm for the compensation current mirrors in the next control cycle.

4) Power supplies: As is shown in Fig. 2, the isolated DC/DC power supply is needed for powering the current mirror circuits, digital isolators, current buffers and comparators on the secondary side. A single isolated power supply with the non-isolated voltage dividers or LDOs can satisfy all the desired driving and signal conditioning voltage levels for the proposed current source gate driver. First, the isolated DC/DC power supplies should have bidirectional outputs ($+V_{cc1\_iso}$ and $-V_{cc1\_iso}$), because the negative turn-off gate voltage is usually desired for the GaN devices to prevent the mis-triggering during the switching transients [14], [15]. The main switch source should be set as the ground for the secondary side of the isolated DC/DC power supply. Meanwhile, the current mirror power supply voltage should be wider than the GaN device gate-to-source voltage range to guarantee the BJTs operate in the forward active region [8]. The desired gate-to-source voltage range for the main switch is from $-V_{cc2\_iso}$ to $+V_{cc2\_iso}$. Second, the driving voltage of the current mirrors should be referred to their negative supplied voltage (the current mirror ground), so it can be negative ($-V_{cc3\_iso}$) referred to the main switch source ground. Last but not least, since the window comparator is referred to the main switch source ground, another positive supply voltage ($+V_{cc3\_iso}$) should be generated for powering the comparator and the following digital isolator.

5) Static voltage sharing resistors and transient voltage suppressor (TVS) diodes: The static voltage sharing resistor (R_{10}) is utilized for equalizing the steady state voltage sharing. Its value should be in the range of hundreds of kΩ, so the additional loss generated in the resistor is negligible. Since its value is so large, it will not help the device dynamic voltage balancing at all. The transient voltage suppressor (TVS) diode (D_3) should be employed to prevent the over-voltage breakdown of the main switch for the initial few switching cycles, because the closed-loop control is one-control-cycle delayed. Since the TVS diode only dissipates the energy of voltage spike for very few switching cycles, the size of the TVS diodes can be very compact. Meanwhile, for the state-of-the-art 500 ~600 V TVS diode, the junction capacitance is only around 10 pF, which has very little impact on the main switch switching speed.

B. Proposed Digital Adaptive Voltage Balancing Scheme in 'Soft' Turn-Off Scenario

As mentioned earlier in this article, for the discrete GaN devices, the dv/dt is usually determined by the drain/load current amplitude during the 'soft' turn-off transient. Although the slew rate of the device rising drain-to-source voltage can not be directly regulated by adjusting the gate current amplitude, the dv/dt starting timing can be precisely controlled. The device with higher dv/dt can be turned off a little bit later, so the well-balanced voltage sharing can be obtained. Actually, this compensation mechanism is referred as the active gate delay control in [10], [12]. However, for the conventional voltage source gate driver, there is only one control freedom, which is the device turn-off gate signal timing. Since the gate can be turned off very quickly for WBG devices (tens of nanoseconds), the controller needs to have extremely high resolution to precisely tune the device turn-off timing. In [10], the selected controller needs to have 0.625 ns unit time step. Since the required adjustment resolution is too high, the device voltage sharing performance is easy to be degraded by the signal jitters [12]. For the proposed current source gate driver, another control freedom is introduced, which is the turn-off gate current amplitude. If the turn-off gate current amplitude is set to be small enough near the threshold voltage level, the device turn-off timing can be precisely adjusted even with larger unit time step in the controller.

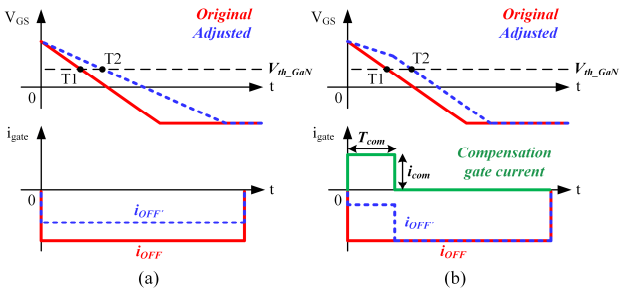

Fig. 3. Different solutions of tuning device turn-off timing during the 'soft' turn-off transient. (a) Solution 1. (b) Solution 2.

Two solutions can be utilized to adjust the device turn-off timing for the current source gate driver, which are shown in Fig. 3. For solution 1 [Fig. 3(a)], the turn-off gate current is directly decreased, so the device turn-off timing will be adjusted from T_1 to T_2. However, the driving voltage for the current mirror needs to be regulated continuously for this solution. Either the digital-to-analog converter (DAC) or the analog controller is required, which will make the gate driver structure more complicated. For solution 2 [Fig. 3(b)], the compensation current is injected to the device gate and the compensation current direction is different from the turn-off gate current. By controlling the amplitude (i_{com}) and pulse-width (T_{com}) of the compensation gate current, the device turn-off timing can be effectively adjusted as well. The latter solution (solution 2) is more suitable for the digital control. The pulse-width of the compensation current can be adaptively adjusted. The

tuning resolution is determined by the unit time step in the controller (ΔT). The amplitude of the compensation current can be adjusted by enabling different level current mirrors in the paralleled branch. Since the digital control will simplify the structure of the gate driver, solution 2 is employed in this study.

For solution 2, two control freedoms are available, which are the pulse-width ($T_{\rm com}$) and the amplitude ($i_{\rm com}$) of the compensation gate current. The product of the compensation current pulse-width and the amplitude is actually the compensation current gate charge ($Q_{\rm com}$). The regulation range and resolution of $i_{\rm com}$ are restricted by the number of paralleled current mirrors. However, for $T_{\rm com}$, it can be regulated in a large range with the controller minimum time step size. Therefore, $T_{\rm com}$ is selected as the major control variable to adjust the device turn-off timing.

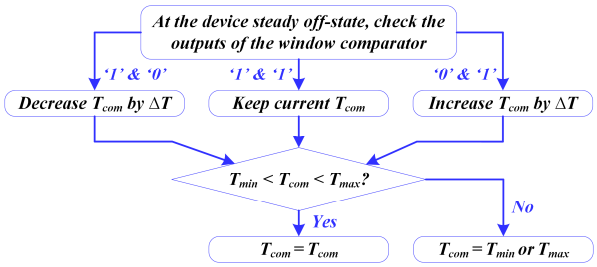

Fig. 4. The flowchart of the adaptive tuning of the compensation current pulse-width.

The flowchart for the adaptive tuning of the compensation current pulse-width is shown in Fig. 4. First, the output states of the window comparator are checked to determine the voltage sharing state of the device (under-voltage, desired voltage or over-voltage) based on Table I. Next, in the following control cycle, the pulse-width of the compensation current is adjusted by a unit time step (ΔT) or kept constant according to the voltage sharing state in the previous control cycle. Eventually, the pulse-width of the compensation current should be limited within certain range. The minimum compensation current pulse-width ($T_{\rm min}$) should be larger than zero, while the maximum compensation current pulse-width ($T_{\rm max}$) should not exceed the pulse-width of the turn-off gate current.

C. Proposed Digital Adaptive Voltage Balancing Scheme in 'Hard' Turn-Off Scenario

As discussed earlier in this paper, the voltage imbalance in the 'hard' turn-off scenario is caused by the drain-to-ground displacement currents. Since the switches with the rising drain-to-source voltage are already in the gate-off state during the dv/dt transient, the voltage imbalance can not be suppressed by adjusting the turn-off timing of the switches. One of the strategies is to trigger the gate of the switch that has higher dv/dt during the drain-to-source voltage rising transient to reduce the device impedance, so the average dv/dt during the switching transient is reduced. Then the well-balanced voltage sharing among the switches can be achieved. In [8], the feasibility of this strategy is validated, but the closed-loop implementation is lacked.

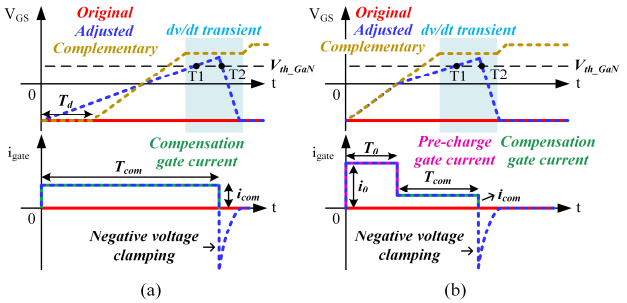

Fig. 5. Different solutions of tuning device turn-off average dv/dt during the 'hard' turn-off transient. (a) Solution 1. (b) Solution 2.

Two solutions can be utilized to regulate the device turn-off average dv/dt for the current source gate driver during the 'hard' turn-off transient, which are shown in Fig. 5. For solution 1 [Fig. 5(a)], the constant compensation gate current is injected into the gate to elevate the device gate-to-source voltage. The active negative voltage clamping takes action right after the compensation current disappears to ensure the safe turn-off for all the switches. The dv/dt transient occurs when the complementary switch gate-to-source voltage reaches the turn-on Miller plateau. During the dv/dt transient, since the adjusted gate-to-source voltage is above the threshold during $T_1 \sim T_2$ interval, the device impedance will be significantly reduced during that interval. Hence, the device turn-off average dv/dt is reduced. However, to achieve the 'fine-tune' of the gate-to-source voltage during the fast dv/dt transient, the compensation gate current amplitude ($i_{\rm com}$) should be significantly smaller than the normal turn-on gate current amplitude. Therefore, the starting timing of the compensation gate current should be advanced by certain amount of time [$T_{\rm d}$ in Fig. 5(a)], which will increase the dead-time duration. To address this drawback, solution 2 is proposed. For solution 2 [Fig. 5(b)], another pre-charge gate current is injected into the gate when the gate-to-source voltage is below zero. The amplitude of the pre-charge current (i_0) is set to be the same as the complementary switch turn-on gate current. Therefore, the two gate-to-source voltages will start to rise at the same time. Meanwhile, the small compensation current is applied after the fixed duration of the pre-charge current (T_0), which will guarantee the 'fine-tune' of the gate-to-source voltage during the fast dv/dt transient. Eventually, the active negative voltage clamping will take action right after the compensation gate current disappears to ensure the safe turn-off of all the switches. Solution 2 can be easily achieved by the proposed current source gate driver. The multilevel gate current can be obtained by enabling different level current mirrors in the paralleled branch. It should be pointed out again that though the gate-to-source voltages of some switches are elevated during the dv/dt transient, the other switches in the series-connected stack are still in the off-state. Therefore, the dc-link shoot-through will not occur, and no significant additional loss

will be produced as well.

For solution 2, since the pulse-width (T_0) and amplitude (i_0) of the pre-charge current are fixed, two control freedoms are available, which are the pulse-width (T_{com}) and the amplitude (i_{com}) of the compensation gate current. Similar to the 'soft' turn-off scenario, T_{com} is selected as the major control variable to adjust the turn-off average dv/dt of the device, because it can be regulated in a large range with the controller minimum time step size. The adaptive tuning of T_{com} is the same as the process for the 'soft' turn-off scenario (shown in Fig. 4). First, the output states of the window comparator are checked to determine the voltage sharing state of the device (under-voltage, desired voltage or over-voltage) based on Table I. Next, in the following control cycle, the pulse-width of the compensation current is adjusted by a unit time step (ΔT) or kept constant according to the voltage sharing state in the previous control cycle. Eventually, the pulse-width of the compensation current should be limited within certain range. The minimum compensation current pulse-width (T_{min}) should be larger than zero, while the maximum compensation current pulse-width (T_{max}) should not exceed the difference between the pulse-width of the complementary switch turn-on gate current (T_{ON}) and the pulse-width of the pre-charge gate current (T_0).

IV. Experimental Verification

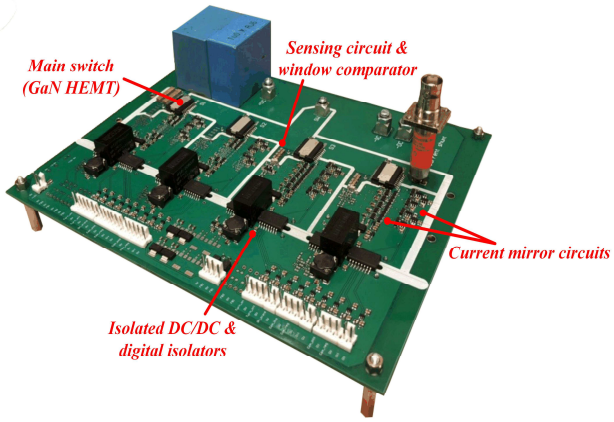

Fig. 6. Prototype of a series-connected GaN-based multiple pulse tester with the proposed closed-loop current source gate driver.

A series-connected GaN-based multiple pulse tester (MPT) prototype with the proposed closed-loop current source gate driver is designed and fabricated as shown in Fig. 6. Infineon 600 V/70 mΩ GaN HEMTs (GIT) are selected to be the main switches. The MPT is basically a half-bridge converter. Two series-connected GaN HEMTs are employed for both the upper arm and the lower arm of the MPT. The schematic of the MPT is the same as the circuit shown in Fig. 1. The two upper arm switches are labeled as S_1 (top-sitting switch) and S_2 (bottom-sitting switch), while the two lower arm switches are labeled as S_3 (top-sitting switch) and S_4 (bottom-sitting switch). Meanwhile, the lower arm switches are regarded as the device under test (DUT), and the lower arm device current is measured by T&M Research SDN-414 current shunt. When the 'soft' turn-off scenario is investigated, an air-core inductor needs to be paralleled with the upper arm switches [shown in Fig. 1(a)]; when the 'hard' turn-off scenario is investigated, an air-core inductor needs to be paralleled with the lower arm switches [shown in Fig. 1(b)]. Although only two switches are connected in series for the prototype, the proposed gate driver and the adaptive voltage balancing scheme can be extended for more switches-in-series scenarios.

Basically, the two series-connected 600 V GaN devices are targeted at 800 V dc-link applications. To evaluate the voltage balancing performance in 800 V dc-link condition, the multiple pulse tests are conducted for both 'soft' turn-off and 'hard' turn-off scenarios. The frequency of the continuous pulses is set to be 500 kHz.

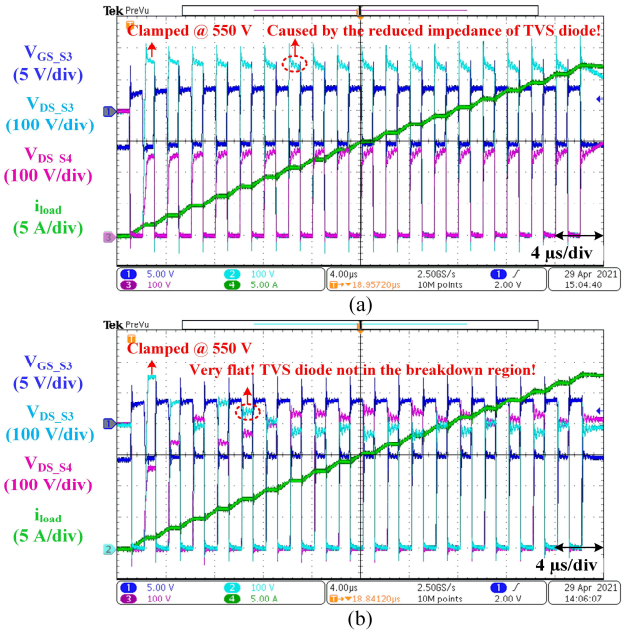

Fig. 7. Multiple pulse test for lower arm switches 'soft' turn-off scenario at 800 V_{dc}. (a) Open-loop. (b) Closed-loop.

The experimental results for the 'soft' turn-off scenario without and with the proposed closed-loop gate current control are shown in Fig. 7. Again, for the 'soft' turn-off experiment, the load inductor is paralleled with the upper arm switches. Meanwhile, the nominal breakdown voltage for the selected TVS diode is 550 V (D_3 in Fig. 2), which is used for the transient over-voltage protection of the main switch. When the closed-loop control is not implemented, as shown in Fig. 7(a), severe voltage imbalance occurs, and the drain-to-source voltage of the top-sitting switch (S_3) is clamped by the TVS diode for every pulse. Due to the accumulated thermal stress, the leakage current of the TVS diode becomes larger with the emerge of more 'over-voltage' pulses. Therefore, the loss generated in the TVS diode will be considerable. If no active voltage balancing strategy is implemented, the TVS diode can be burned eventually. When the proposed closed-loop gate current control is implemented, as shown in Fig. 7(b), the well-

balanced voltage sharing is achieved and the off-state drain-to-source voltage is very 'flat' for all the pulses, which indicates that the TVS diode is not in the breakdown region (except for the first pulse). Therefore, the leakage current in the TVS diode is minimal and the loss generated in the TVS diode is insignificant.

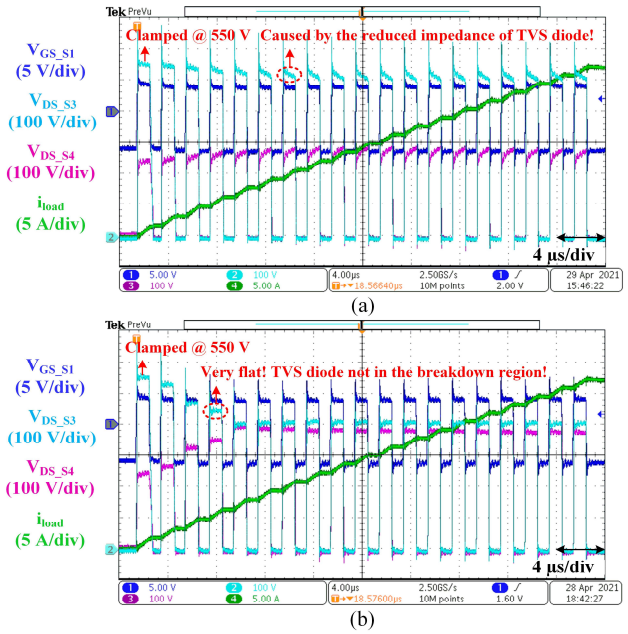

Fig. 8. Multiple pulse test for lower arm switches 'hard' turn-off scenario at 800 V_{dc}. (a) Open-loop. (b) Closed-loop.

The experimental results for the 'hard' turn-off scenario without and with the proposed closed-loop gate current control are shown in Fig. 8. Again, for the 'hard' turn-off experiment, the load inductor is paralleled with the lower arm switches. Similar to the 'soft' turn-off scenario, without the closed-loop gate current control, the TVS diode is in the breakdown region for every pulse to dissipate the 'over-voltage' energy, as shown in Fig. 8(a). After the closed-loop gate current control is implemented, the TVS diode will leave the breakdown region from the second pulse, as shown in Fig. 8(b). Therefore, the loss generated in the TVS diode is insignificant.

To sum, the proposed adaptive voltage balancing strategy works well for both 'soft' turn-off and 'hard' turn-off scenarios in 800 V dc-link condition. Meanwhile, the TVS diode is only used for clamping the voltage for the very first pulse, so the generated loss in the TVS diode is extremely insignificant. The size and power rating of the TVS diode can be very small as well.

V. Conclusion

In this paper, a novel closed-loop current source gate driver is proposed, which addresses the dynamic voltage imbalance issues for series-connected GaN HEMTs. Meanwhile, the effective voltage balancing schemes for both soft switching and hard switching scenarios are presented and validated. A series-connected GaN-based multiple pulse tester is built to validate the performance of the proposed current source gate driver. With the employment of the proposed closed-loop gate current control, the well-balanced voltage sharing is obtained under various operating conditions.

References

[1] Z. Zhang, L. M. Tolbert, D. Costinett, F. Wang, and B. J. Blalock, "A new hands-on course in characterization of wide-bandgap devices," *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9392–9403, 2019.

[2] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial gan power devices and gan-based converter design challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707–719, 2016.

[3] A. Hensler, S. Franz, D. Shapiro, and G. Bunin, "800v synchronous buck converter with series-connected gan power transistors," in *PCIM Asia 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. VDE, 2018, pp. 1–7.

[4] J. Roig, G. Gomez, F. Bauwens, B. Vlachakis, J. Rodriguez, M. R. Rogina, A. Rodriguez, and D. G. Lamar, "Series-connected gan transistors for ultra-fast high-voltage switch (¿1kv)," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 3043–3048.

[5] M. Shojaie, N. Elsayad, H. Moradisizkoohi, and O. A. Mohammed, "Design and experimental verification of a high-voltage series-stacked gan ehemt module for electric vehicle applications," *IEEE Transactions on Transportation Electrification*, vol. 5, no. 1, pp. 31–47, 2018.

[6] A. Marzoughi, R. Burgos, and D. Boroyevich, "Active gate-driver with dv/dt controller for dynamic voltage balancing in series-connected sic mosfets," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 4, pp. 2488–2498, 2018.

[7] C. Liu, Z. Zhang, Y. Liua, Y. Si, M. Wang, and Q. Lei, "A universal block of series connected sic mosfets using current source gate driver," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2021.

[8] Z. Zhang, C. Liu, M. Wang, Y. Si, Y. Liu, and Q. Lei, "A novel current-source-based gate driver with active voltage balancing control for series-connected gan hemts," *IEEE Open Journal of Power Electronics*, pp. 1–1, 2021.

[9] X. Lin, L. Ravi, Y. Zhang, R. Burgos, and D. Dong, "Analysis of voltage sharing of series-connected high voltage sic mosfets and body-diodes," *IEEE Transactions on Power Electronics*, pp. 1–1, 2020.

[10] T. Wang, H. Lin, and S. Liu, "An active voltage balancing control based on adjusting driving signal time delay for series-connected sic mosfets," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 454–464, 2019.

[11] X. Li, L. Zhang, S. Guo, Y. Lei, A. Q. Huang, and B. Zhang, "Understanding switching losses in sic mosfet: Toward lossless switching," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. IEEE, 2015, pp. 257–262.

[12] Z. Zhang, H. Gui, J. Niu, R. Chen, F. Wang, L. M. Tolbert, D. J. Costinett, and B. J. Blalock, "High precision gate signal timing control based active voltage balancing scheme for series-connected fast switching field-effect transistors," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2018, pp. 925–930.

[13] E. Raszmann, K. Sun, R. Burgos, I. Cvetkovic, J. Wang, and D. Boroyevich, "Voltage balancing of four series-connected sic mosfets under 2 kv bus voltage using active dv/dt control," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 6666–6672.

[14] Z. Zhang, M. Wang, C. Liu, Y. Si, Y. Liu, and Q. Lei, "High-dv/dt-immune fine-controlled parameter-adaptive synchronous gate driving for gan-based secondary rectifier in ev on-board charger," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2020.

[15] C. Liu, Z. Zhang, Y. Liu, Y. Si, and Q. Lei, "Smart self-driving multilevel gate driver for fast switching and crosstalk suppression of sic mosfets," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 442–453, 2020.