An Optically Powered, High-Voltage, Switched-Capacitor Drive Circuit for Microrobotics

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***Abstract*— This work presents an efficient high-voltage (HV) drive circuit for mm- and cm-scale electrostatic and piezoelectric microrobotic transducers. Designed in a 650-V SOI CMOS process, a reconfigurable series–parallel switched-capacitor (SC) converter interfaces between either on-chip photovoltaic (PV) cells or a single off-chip battery, and an HV MEMs actuator. The SC converter boosts a nominal ∼3.7–7.4-V input by ∼16× to 60–117 V. By using a pseudo-adiabatic drive process, the converter charges the output sequentially and recovers energy in discharge cycles to reduce power consumption by over 10× compared with a conventional hard-switching driver. On-chip PV cells use deep-trench isolation such that they can be stacked and reconfigured in arbitrary series and parallel voltage domains. Measured results show effective operation with reactive loads up to 20 nF, operating frequencies over 50 kHz, and delivered power levels up to 95 mW.**

***Index Terms*— DC–DC converter, energy harvesting, haptics, microelectromechanical systems (MEMs), switched capacitor (SC), wireless power delivery.**

I. Introduction

DUE to their small size and versatility, microrobotics and microelectromechanical systems (MEMS) have promising applications in biomedicine, optics, industrial diagnostics, and manufacturing. Electrostatic and piezoelectric actuators have been studied extensively for MEMs, robotics, and haptics due to their relatively high energy density, high bandwidth, and high efficiency at mm- and cm-scale form factors [1]–[6]. Contrasting with MEMs resonator applications [7], robotic actuators typically present as dominantly capacitive loads (tens of pF to tens of nF) due to the need for sub-resonant, broadband actuation (see Fig. 1) [4]–[6]. However, these devices typically require high voltage (HV) (30 V to a few kilovolts) to realize their full energy-density capabilities and drive frequencies in the range of 10 Hz–10 kHz to maximize power density.

This motivates an entirely different scope of power management circuits that must operate efficiently at HV while driving dominantly reactive loads [1]. Many systems would ideally operate untethered from physical wires and therefore require small batteries (embedded in the electromechanical platform) or the use of wireless power delivery. Due to the relatively low cell voltages of small-scale batteries (∼1−10 V), battery-based power systems require a significant step-up (boost) conversion ratio to achieve suitable actuation voltages [8]. However, high-conversion-ratio boost converters are especially challenging when constrained to mm- or cm-scale form factors and sub-gram weight limits [8]–[10].

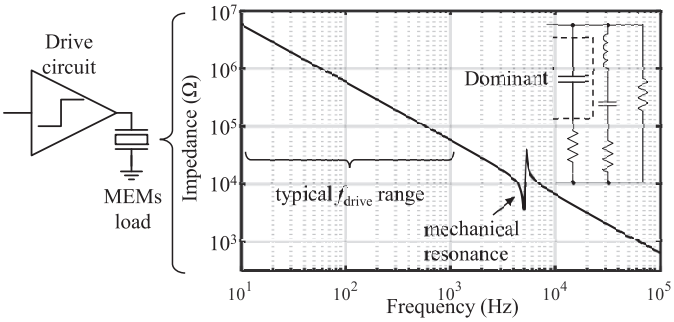

Fig. 1. Representative piezoelectric actuator impedance model.

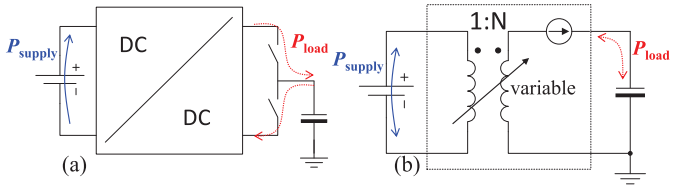

Fig. 2. Representative state-of-the-art MEMs drivers. (a) Hard switching from a boosted dc power supply. (b) Direct drive using a variable dc–dc converter.

Past efforts for driving piezoelectric or electrostatic actuators include hard switching approaches [3], [11] and schemes that drive actuators directly with a variable-boost dc–dc converter [6], [8], [12], [13]. Hard-switching approaches, shown in Fig. 2(a), require a fixed HV dc supply and directly switch the actuator between the HV supply and the ground. Driving a dominantly capacitive load in this way introduces hard-charging loss, which can be quantified as

$$P_{\text{supply}} = C_{\text{load}} V_{\text{out}}^2 f_{\text{drive}} \tag{1}$$

where C_{load} is the load capacitance, V_{out} is the peak-to-peak driving voltage, and f_{drive} is the driving or actuating frequency. Therefore, even with an efficient dc–dc converter,

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hard switching results in high power loss as the reactive power delivered to the dominantly capacitive load is lost in the switching process.

Variable-boost approaches use an efficient dc–dc converter to interface directly with the actuator without the use of additional switches [1]. Assuming that the conversion ratio can be varied between zero and N times the system supply voltage, the scheme shown in Fig. 2(b) can operate as an efficient power amplifier, supplying reactive power to the capacitive load without incurring resistive loss. Furthermore, assuming that the converter is bidirectional, it is possible that the energy stored on the load capacitor can be recovered and returned to the system power supply (e.g., battery). If this is the case, the scheme in Fig. 2(b) can supply and recover reactive power without incurring power loss.

However, there are many challenges in designing a circuit such as that shown in Fig. 2(b). First, in many cases, the system power supply cannot accept bidirectional power. This is the case if the power source is a primary (non-rechargeable) battery, which can supply but not sink current. Second, many HV boost circuits are only practical with diodes in the conduction path. Diodes prevent many boost converters from operating bidirectionally, and thus, they may be efficient in charge cycles, but rely on hard switching to discharge the actuator. In this case, the power loss is approximately $1/2$ of that in (1).

Finally, most HV boost circuits are based on energy storage in magnetic components (inductors or transformers) [9]. Due to fundamental scaling properties, magnetic components scale poorly to small size [14], their performance degrading both in terms of efficiency and power density [15]. This presents practical limits on conversion ratio [9], size [8], and efficiency of most boost dc–dc conversion circuits [10].

Capacitors, on the other hand, scale more favorably to small size [16], with the potential to achieve multiple orders of magnitude higher energy density than inductors at mm-scale form factors [14]. Switched-capacitor (SC) dc–dc converters, which leverage high-energy-density capacitors, hold great promise for electrostatic drive applications and other high-conversion-ratio boost functions [8], [17]. The SC approach is also well-suited for CMOS integration due to the use of scalable and hierarchical switching circuits comprising low-voltage-rated switches.

This work presents an SC drive circuit that can be used for small-scale piezoelectric and electrostatic micro-mechanical actuators. The circuit leverages a reconfigurable series–parallel architecture to step the driving voltage of an MEMs load sequentially in small increments to reduce hard-charging losses and recovers energy during discharge directly in flying capacitors. Operating with either a single off-chip battery or an on-chip photovoltaic (PV) array, the circuit reduces power consumption by over an order-of-magnitude compared with an ideal hard-switching driver. Sections II and III discuss the topology and general operating principles, respectively. Section IV provides the details of the circuit design. Section V describes integrated solar cells and optical power delivery. Section VI provides the experimental results and Section VII provides a conclusion.

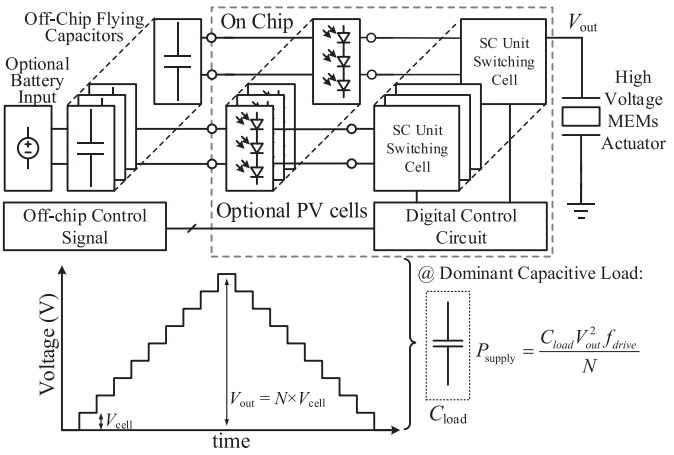

Fig. 3. Block diagram of the proposed system.

II. Topology Overview

A high-level block diagram of the proposed system is shown in Fig. 3. The proposed SC converter comprises a number, N, of independent switching cells, each controlling the configuration of an off-chip flying capacitor. In aggregate, the converter operates as a reconfigurable series–parallel SC converter. The circuit is controlled digitally through an I/O bus and is designed to interface with a single off-chip MEMs load. As shown in Fig. 3, the proposed driver is designed to step the voltage on the MEMs load sequentially in small voltage steps up to a maximum of $N \times V_{\text{cell}}$, where V_{cell} corresponds to the flying capacitor voltage of a given switching cell. By reducing the magnitude of the voltage change in any given switching state, the scheme reduces hard-switching (or $C \times V^2$) power loss when driving dominantly capacitive loads. This process is described as pseudo-adiabatic because in the limit with arbitrarily small V_{cell} and high N, the process approaches lossless reactive power delivery.

Importantly, when discharging or stepping down the MEMs load, energy is recovered (returned to the flying capacitors) such that less total energy is required from the system power supply. Therefore, the flying capacitors (themselves) provide a means to recover and store reactive power such that no power needs to be returned to the system supply. This allows the scheme to work with non-rechargeable power sources and without any additional bypass or storage capacitance.[1]

The pseudo-adiabatic charging and discharging process reduces power consumption compared with a hard-switching driver by roughly the number of switching cells, N, in the converter. This is because with N switching cells, although the hard-charging process is repeated N times, the energy loss in each step is reduced by N^2. Therefore, the total power loss

[1]From the perspective of an individual flying capacitor: when stepping up the load, the capacitor voltage decreases slightly each time the voltage steps as it supplies charge to the load; when stepping down the load, the capacitor recovers a portion (but not all) of this charge—the remainder accounted for by residual hard-charging losses and power consumed by the circuit. At the end of (or during) the stepping process, the system battery or a PV cell must provide charge to bring the capacitor back to its initial starting voltage. This accounts for the (reduced but non-zero) power flow from energy sources in the system.

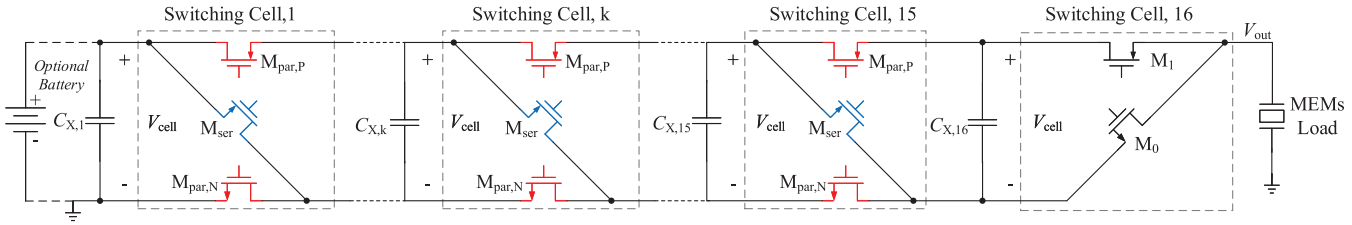

Fig. 4. Modified series–parallel SC converter: red switches ON in parallel state and blue switches ON in series state.

of the converter across a full charge–discharge cycle follows:

$$P_{\text{supply}} = \frac{C_{\text{load}} V_{\text{out}}^2 f_{\text{drive}}}{N}. \tag{2}$$

Going forward, it is important to note several key differences between electrostatic/piezoelectric drive applications and conventional dc–dc converters. In the former scenario, while some real power is delivered, it depends heavily on the load conditions of the actuator and tends to be much smaller than the magnitude of reactive power. Therefore, it is very difficult to quantify efficiency in terms of real load power over real supply power. Here, we define a metric that is useful in quantifying the efficiency of delivering and recovery dominantly reactive power, defined as the power reduction factor (PRF)

$$\text{PRF} = \frac{P_{\text{reactive}}}{P_{\text{supply}}} = \frac{C_{\text{load}} V_{\text{out}}^2 f_{\text{drive}}}{P_{\text{supply}}} \tag{3}$$

where P_{reactive} is the sum of reactive power transfer in both the charge and discharge cycles and P_{supply} is the power taken from the system supply (i.e., battery) across the whole cycle. The PRF metric can be viewed as an effective quality factor, Q, of the power delivery circuit, and thus, a higher value is better. If the converter is lossless, then the PRF (effective Q) would approach infinity. However, in the proposed scheme (Fig. 3), the PRF is the ratio of (1) over (2) or goes with approximately, N, the number of switching stages in the circuit.

A key consideration is biasing and (parasitic) frequency-dependent losses in the circuit. A simple calculation shows that there is an optimum number of stages, N_{opt}, in the circuit when factoring per-stage bias or operating power, P_{cell}. Assuming that total power loss in the circuit goes with

$$P_{\text{total}} = \frac{C_{\text{load}} V_{\text{out}}^2 f_{\text{drive}}}{N} + N \cdot P_{\text{cell}} \tag{4}$$

then a simple convex optimization provides

$$N_{\text{opt}} = \sqrt{\frac{C_{\text{load}} V_{\text{out}}^2 f}{P_{\text{cell}}}}, \text{ and } P_{\text{min}} = \sqrt{C_{\text{load}} V_{\text{out}}^2 f \cdot P_{\text{cell}}} \tag{5}$$

which indicates that minimum achievable power consumption goes as the geometric mean of the total power delivered to the MEMs actuator and the power required per stage for basic operation. Here, P_{cell} is assumed to include any quiescent power required for each cell to operate and can also include parasitic frequency-dependent losses (assuming that they are uniform and proportional to the number of cells). Such power may include gate drive, level shifting, and control circuit power and power required to drive parasitic tub, well, and interconnect capacitance. In many cases, these loss factors may not scale uniformly with the number of cells and so (5) may be considered a rule of thumb rather than an exact optimization.

III. Topology Details

Fig. 4 shows a schematic of the modified series–parallel converter designed in this work. The converter comprises $N = 16$ switching cells, each controlling the state of an off-chip flying capacitor.[2] For each of the first 15 cells, when M_{ser} is "ON," the respective flying capacitor is configured in series with the adjacent cell (on the right). When $M_{\text{par,P}}$ and $M_{\text{par,N}}$ are "ON," the flying capacitor is in parallel with the adjacent cell. The last cell (cell 16) uses two switching devices: M_0, which connects V_{out} to the bottom plate of the last flying capacitor, and M_1, which connects V_{out} to the top plate.

With all of the M_{ser} devices (and M_1 in final cell) "ON," all storage cells are in series, their voltage adding to boost V_{out}. With all of the M_{par} devices (and M_0 in the final cell) "ON," all storage cells are in parallel and V_{out} is shorted to ground. With storage cells in parallel, their charge (voltage) can equalize and/or additional charge can be supplied from a single energy source (e.g., battery) connected across the tap on the first storage cell. The equalization step has important benefits in the PV implementation as it can mitigate mismatch and non-uniform optical power density in the cells as will be discussed further.

Importantly, assuming that each of the switching cells is controlled independently, a range of discrete voltages between zero and $N \times V_{\text{cell}}$, where N is the number of switching cells, can be provided to the output. Thus, as shown in Fig. 5, by controlling the switching sequence in a preset pattern, V_{out} can step up (or step down) in integer increments of V_{cell}. Assuming that the switching process occurs such that the flying capacitor voltages fully settle between transitions, this process maps to the pseudo-adiabatic switching scheme in Fig. 3.

Several features make the modified series–parallel converter attractive for MEMs driving applications. Here, it should be noted that each of the switching devices in Fig. 4 is rated only to block a single low voltage, V_{cell}. Compared with a conventional dc–dc series-parallel SC converter [17], [18], there is no HV rectifying switch, which simplifies the design

[2]Off-chip flying capacitors are used in this application as the magnitude of the load capacitance is too large to be efficiently driven with on-chip (integrated capacitors); however, very small, high-energy-density 0402 capacitors are used in the experimental prototype to keep overall solution size < 1 cm^2.

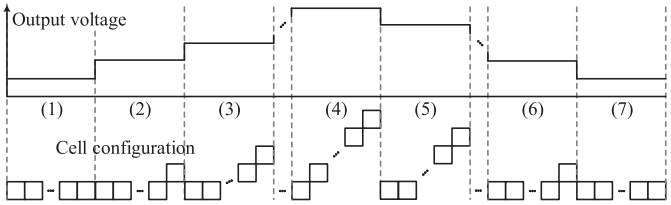

Fig. 5. Representative configuration of switching cells during step up/down.

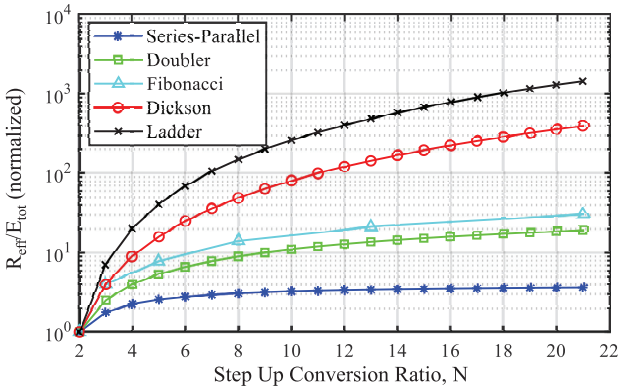

Fig. 6. SC boost comparison: $R_{\text{eff}}/E_{\text{tot}}$ versus conversion ratio (modified perspective of the analysis in [17]).

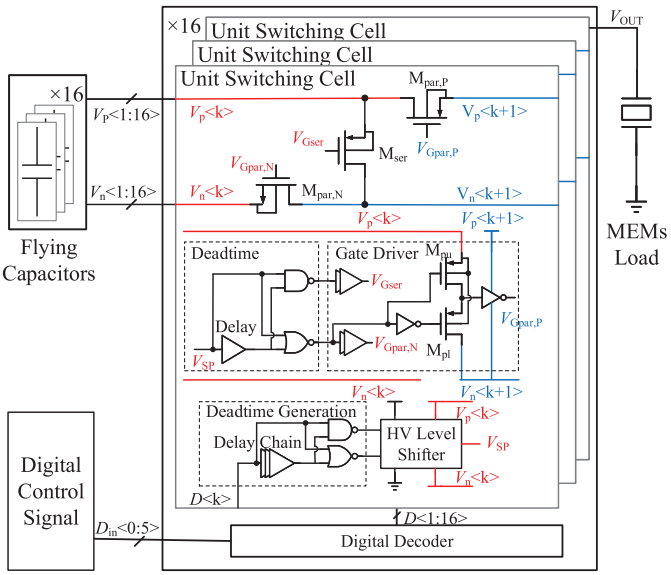

Fig. 7. Detailed circuit block diagram.

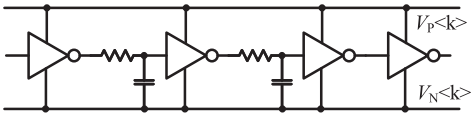

Fig. 8. Delay chain for deadtime implementation in the floating domain.

and improves the $\sum V \cdot A$ product, the sum of rated switch voltage times rated switch current.

The series–parallel converter is also known to have the maximum passive component utilization achievable by any topology [17]. Fig. 6 exemplifies this benefit by plotting the ratio of effective output resistance (R_{eff}), a proxy for output-power driving capability, to total required energy storage ($E_{\text{tot}} = \sum CV^2$) of flying capacitors, a proxy for total flying capacitor volume [19], versus conversion ratio, N. With a fixed total passive component (capacitor) volume, the series–parallel topology can provide the lowest output impedance (highest power delivery); alternatively, at a fixed output impedance, it can use the minimum total capacitor volume of any known two-phase SC converter (it achieves the Wolaver limit defined in [20] and [21]). Thus, for applications primarily constrained by the volume and weight of passive components, the series–parallel converter can be considered an optimal topology.

IV. Circuit Implementation

A. High-Level Circuit Operation

Fig. 7 shows a more detailed block diagram of the circuit architecture implemented in this work. The circuit includes an interface to off-chip digital control, HV level shifters to pass signals to the floating powertrain switches, and nested timing blocks to enforce deadtime and anti-cross conduction. To simplify the digital interface, an on-chip decoding scheme is used to reduce I/O to a 6-bit digital control signal, $\text{D}_{\text{in}}\langle 0{:}5\rangle$. The decoders pass each of 16 differential thermometer coded logic-level CMOS bits to the level shift circuit.

Each bit of the decoded control signal passes through a first deadtime generation circuit, which ensures that the differential level-shift signals are non-overlapping to prevent common-mode current conduction. The control signals then pass through an HV level shifter where they are received in the floating domain of the individual switching cells. A second deadtime generation circuit in the floating domain is used to prevent cross conduction in the powertrain devices. As shown in Fig. 8, the floating-domain deadtime circuit uses an *RC* delay chain, rather than an inverter buffer chain to reduce sensitivity to varying supply voltages in the floating domains.

In the floating (switching cell) domains, the three power switching devices have different considerations for their drive voltages. In the kth switching cell, N-channel device $\text{M}_{\text{par,N}}$ is referenced to $V_{\text{n}}\langle k\rangle$, the common voltage for the switching cell (bottom plate of flying capacitor, $C_{\text{X},k}$) such that its gate $V_{\text{Gpar,N}}$ can be driven directly by a local buffer chain operating between $V_{\text{n}}\langle k\rangle$ and $V_{\text{p}}\langle k\rangle$. *P-channel* device M_{ser} is source-referenced to the local supply voltage $V_{\text{p}}\langle k\rangle$, which simplifies driving of the V_{Gser} terminal to the same domain as for $\text{M}_{\text{par,N}}$. However, device $\text{M}_{\text{par,P}}$ is referenced (its source is connected) to the positive supply voltage, $V_{\text{p}}\langle k+1\rangle$, of the adjacent switching cell. Therefore, a special level shifter is needed to drive the gate, $V_{\text{Gpar,P}}$, of $\text{M}_{\text{par,P}}$ in the $(k+1)$th voltage domain.

Equivalent circuits of the level shifter for the $\text{M}_{\text{par,P}}$ device are shown in Fig. 9. The level shifter uses a PMOS–PMOS inverter-like structure using devices M_{L1} and M_{L2} to pass the drive signal across the adjacent voltage domain. In the parallel state [Fig. 9(b)], $\text{M}_{\text{par,P}}$ is turned on, shorting $V_{\text{p}}\langle k\rangle$ and $V_{\text{p}}\langle k+1\rangle$ through $\text{R}_{\text{on,Mpar,P}}$ (also, $V_{\text{n}}\langle k\rangle$ is shorted to $V_{\text{n}}\langle k+1\rangle$ through $\text{R}_{\text{on,Mpar,N}}$). Here, control signal V_{par} is

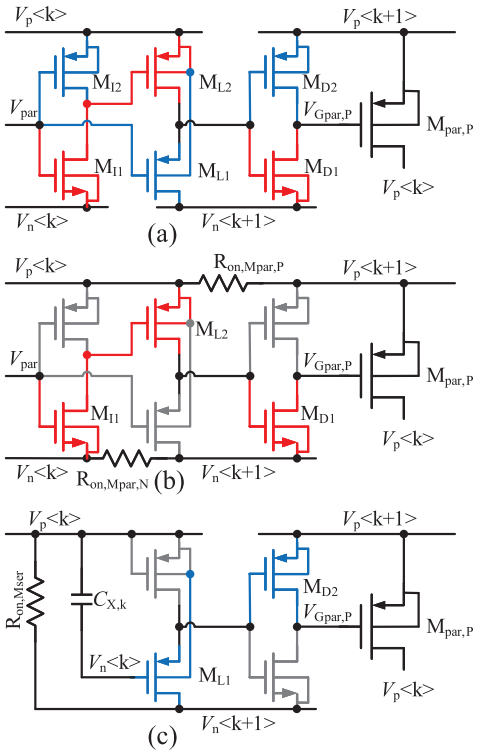

Fig. 9. Local level shifter for $M_{par,P}$ device. (a) Circuit schematic. (b) Equivalent circuit with the adjacent cell in the parallel state. (c) Equivalent circuit with the adjacent cell in the series state.

high, turning on M_{I1}, M_{L2}, and M_{D1}, pulling down the gate of $M_{tpar,P}$, turning it on to connect the domains in the parallel state. In the series state [Fig. 9(c)], $M_{par,P}$ is OFF and M_{ser} is ON such that $V_p\langle k+1\rangle$ is higher than $V_p\langle k\rangle$ by V_{cell}. In this case, V_{par} is low, setting the gate of M_{L1} to $V_n\langle k\rangle$. However, because $V_p\langle k\rangle$ is shorted to $V_n\langle k+1\rangle$ by device M_{ser} through $R_{on,Mser}$, M_{L1} is on, which pulls down the gate of M_{D2}, pulling up $V_{Gpar,P}$ and turning $M_{par,P}$ off.

B. Cascode HV Level Shifter

Fig. 10 shows the schematic of the HV level shift circuit. Each of the 16 switching cells requires an independent control signal to be translated to an arbitrary common-mode level to activate the switching process. To minimize quiescent current consumption and relax timing constraints on the digital control block, signal translation operates with a charge-based level shifter and a latching structure in the floating HV domain. A latch is used to hold the circuit state without using quiescent bias power. A stack of low-voltage cascodes provides signal isolation while preventing over-voltage of any device.

The level shifter works with a ground-referenced signal applied to differential pair, M_A and M_B, at the V_A and V_B terminals. Capacitive degeneration at the source terminals results in a current pulse (sinking) through a respective branch of the cascode level shift circuit. This current pulse drives a linear OTA circuit in the floating domain, which amplifies the injected charge to set the polarity of a weak bi-stable latch. The voltage on degeneration capacitance is reset, antiphase with V_A and V_B to ensure that full charge is delivered during switching. After switching, current in the degeneration

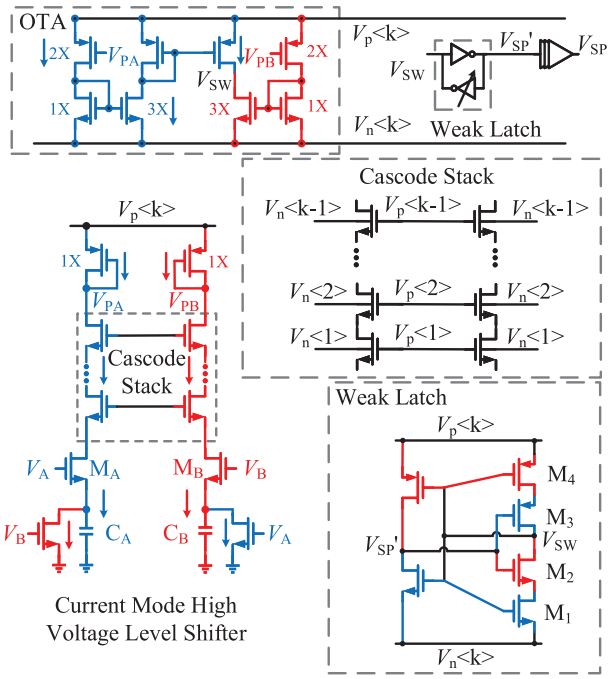

Fig. 10. Circuit diagram of the cascode HV level shifter.

capacitors and cascode branches decays to zero such that hold-state power consumption is negligible; this also simplifies control as the V_A and V_B signals are only level-dependent—no strict timing requirements or pulse generation signals are needed.

Importantly, the cascode branches are implemented with only low-voltage CMOS (5 V rated) devices. The gate of each (differential) cascode pair is connected to the positive voltage terminal ($V_p\langle k\rangle$) of each successive switching cell. This saves significant die area compared to using HV DMOS cascodes but does require that each switching cell has a different number of cascodes in series with the floating OTA (the kth cell requires $k-1$ cascode devices in series). Also, complex metal interconnect is required due to a large number of series cascodes, which also increases capacitive parasitics in the level shifter.

The use of a linear OTA circuit provides symmetric rise and fall propagation delays and eliminates the need for complementary (PMOS) devices in the cascode stack. By amplifying charge in the floating domain, less charge is required in the cascode stack, which would otherwise result in higher power consumption. The OTA drives a weak latch that consists of inverters M_1–M_4 and M_2–M_3, cross coupled but stacked in series to reduce needed drive strength while holding the latched state. The output of the weak latch is passed to the buffer chain and digital circuitry needed to operate the powertrain.

V. Optical Power Delivery

As shown in Fig. 3, the circuit was designed to operate with either a single off-chip battery or an optical power source driving a silicon-integrated PV array. Fig. 11 shows the details of the integrated PV cells and their configuration on-chip. The circuit was implemented in a 1-μm, 650-V SOI CMOS

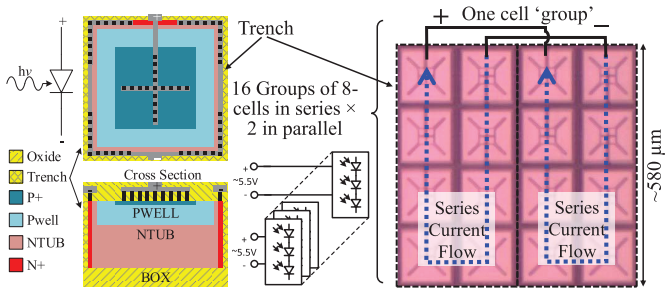

Fig. 11. On-die series-stacked PV cells: layout, cross section, slice of die photograph.

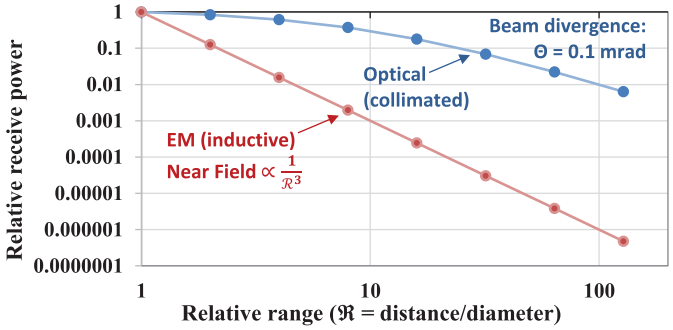

Fig. 12. Effective power delivery versus relative range $\mathscr{R}$, defined as transmission distance over the diameter of the receive antenna (EM coil or PV array).

process with deep-trench isolation. Isolated wells were used to construct small ($\sim$ 140 μm $\times$ 140 μm) solar cells that could float in arbitrary series and parallel voltage domains. Each cell consisted of an isolated n-type bulk region, implanted with a lightly doped p-well to form a vertical photodiode. Contact was made to the cell through a P+ anode contact and an N+ contact to an N-sinker along the oxide trench at the cell periphery.

As in [3] and [11], trench isolation was used to allow arbitrary stacking of cells in series voltage domains to boost the effective voltage of the stack. In this work, because each of the $N = 16$ flying capacitor taps in Fig. 4 operates independently, the design included 16 independent groups of two paralleled strings of 8 cells in series (see Fig. 11). At a nominal (solar-spectrum) optical power level of $\sim$ 1 mW/mm^2, these cell groups provided an open-circuit voltage of $\sim$ 5.5 V and an optical-electrical efficiency of $\sim$ 11.5%.

A primary benefit of optical wireless power delivery is its ability to operate with a relatively high transmission distance compared to the size of the optical receiver. For example, near-field electromagnetic (inductive) coupling has been used in many examples spanning portable communication devices to electric vehicles. However, the dispersion of near-field electromagnetic energy results in a maximum delivered power level that falls off with transmission distance over diameter (of the antenna) cubed [22]. This poses impractical range limitations on robotic applications at the mm-scale [23].

However, as shown in Fig. 12, optical power (as a form of far-field transmission) follows an inverse square law (asymptotically) at long transmission ranges. The difference between a squared and cubic reduction in power with transmission distance provides significant gains, especially at long range. However, laser collimation introduces a scalar factor that (effectively) reduces energy dispersion at short and medium distances—improving power delivery by multiple orders of magnitude compared to near-field electromagnetic transmission. Optical power delivery provides opportunities to tailor the wavelength of the light source to the semiconductor bandgap to improve quantum efficiency. However, it does require a line-of-sight transmission channel.

VI. Experimental Results

Fig. 13 shows the die photograph and circuit-board assembly. Total die area is just under 10 mm^2, and the bulk

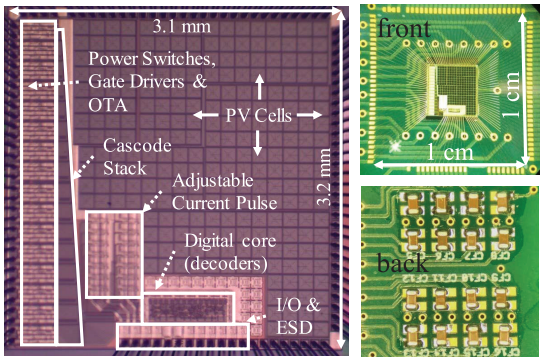

Fig. 13. Die photograph of the chip; active area is just under 10 mm^2.

of the area ($\sim$6 mm^2) is used for on-chip PV cells. The powertrain and floating circuitry required $\sim$1 mm^2, the pulse generation 0.4 mm^2, and the digital control 0.2 mm^2. The remainder of the die area was used for routing, pad ring, and ESD structures. Flying capacitors were placed off-chip (PCB backside) and were 0402 footprint 1.4-μF capacitance (GRM155R61A475MEA), derated at the nominal operating voltage. The active circuit board area was $<$ 1 cm^2.

The integrated circuit was controlled externally with an FPGA that generated a periodic, programmable cell configuration waveform. Switching states were loaded from MATLAB through a UART into switch sequence registers, as shown in Fig. 14. These registers were read sequentially, while the address was enabled. A controller enabled the address block and write permissions into the switch sequence register to ensure the safe operation of the SC circuit. The 3.3-V digital signals coming from the FPGA were passed to an on-board level shifter, which shifted the logic signals into the digital voltage domain of the chip.

The circuit was tested under two conditions. In one test, an external $\sim$7.4-V supply (representative of two lithium battery cells connected in series) was used to quantify the performance of the system. In a second test, the external power supply was disconnected, and system was powered solely by the PV cells.

For optically powered operation, a fiber light with a nominally white spectrum was used to power the arrays. The fiber light produced incident optical power between 1 and 5 mW/mm^2. However, even with the relatively wide optical

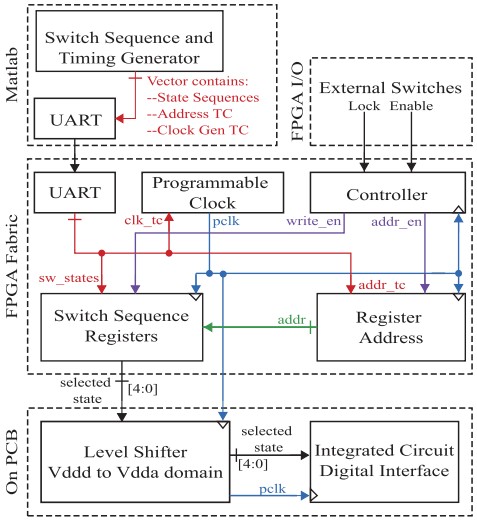

Fig. 14. Digital system architecture.

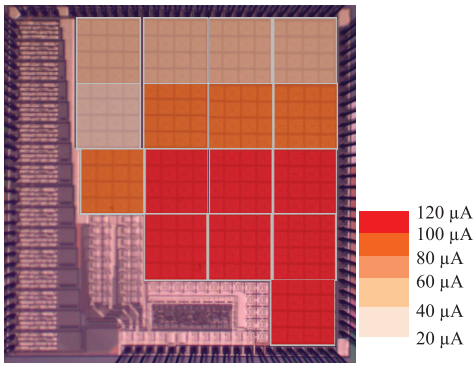

Fig. 15. Measured short-circuit currents' spatial distribution represents the light intensity distribution of the fiber light used in the testing.

cross section of the fiber light, significant nonuniformity in the spatial optical distribution was detected. Mismatch and nonuniformity are expected challenges when using on-chip PVs. In addition to process variation and the potential for dust and debris to settle on the die or optical interface, long-range optical power delivery is also subject to limitations related to the diameter of the incident beam, its position on the array, and other aspects of the optics in the system.

However, an important benefit of the proposed solution is that it can help to alleviate problems with mismatch and variation in the PV array(s). Similar to past work in macro-scale PVs [24], the series–parallel SC converter helps to alleviate mismatch by enforcing voltage equalization of the PV taps. By forcing equivalent voltages across the PV groups, sensitivity to incident power is reduced because the voltage operating point goes only logarithmically with insolation. Therefore, power can be drawn in proportion to available power and is not limited by the worst cell or cell group.

Fig. 15 shows the measured data for the short-circuit current in the individual cell groups, aligned with their spatial distribution while stimulating with a fiberlight. The measured spatial non-uniformity of light distribution has a 1σ mismatch of 29%. A clear region of focus is seen toward the bottom right;

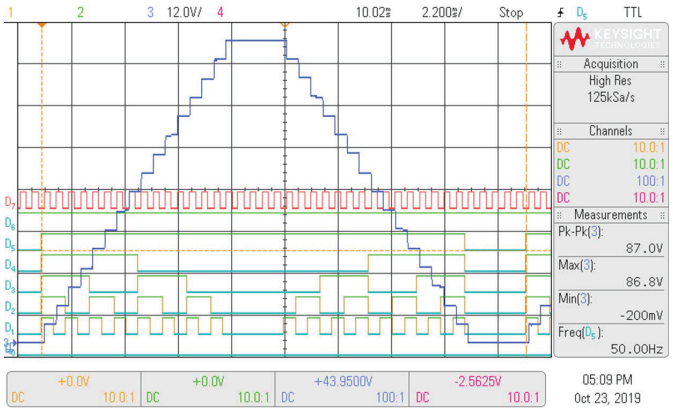

Fig. 16. Oscilloscope screen shot of hardware prototype operation: optically powered while driving 120-pF load at 50 Hz.

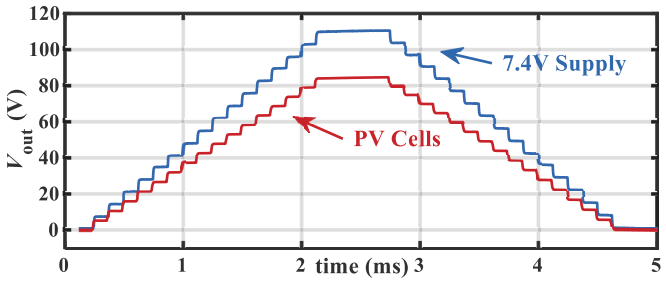

Fig. 17. Time-domain output waveform: 5-nF load at 200 Hz (unfiltered oscilloscope data taken with 100-MΩ HV passive probe).

certain cell groups have anomalously low power indicating random mismatch or dust. However, the series–parallel converter effectively compensates for this mismatch.

Fig. 16 shows an oscilloscope screenshot of the system running with an optical power supply, driving a 120-pF load capacitance[3] at 50 Hz. The pseudo-adiabatic drive waveform (see Fig. 3) is clearly visible and provides an effective boost of $\sim 16\times$ from the roughly 5.5 V_{OC} voltage of the individual PV arrays. Also, it can be seen that the magnitude of the individual voltage steps is roughly the same; this indicates the effective voltage equalization and mitigation of the power mismatch present in the on-chip PV arrays (see Fig. 15). Therefore, despite significant spatial power variation, the circuit operates normally.

Fig. 17 shows a similar perspective but overlays measured data taken with the PV supply and with a single off-chip 7.4-V supply when driving a 5-nF load capacitance at 200 Hz. Here, differences between the PV cell (optical power) and single battery cases should be noted. Measured V_{OC} for PV cell groups was $\sim$ 5.5 V; however, the "single battery" test setup used a 7.4-V supply. Therefore, the peak driving voltages were higher in the latter case.

Fig. 18 shows a more comprehensive plot of the drive voltage peak-to-peak versus frequency for a range of load capacitance. Here, clear limits of the SC drive scheme are

[3]All load capacitors used for testing were Class-I (COG) HV ceramic capacitors.

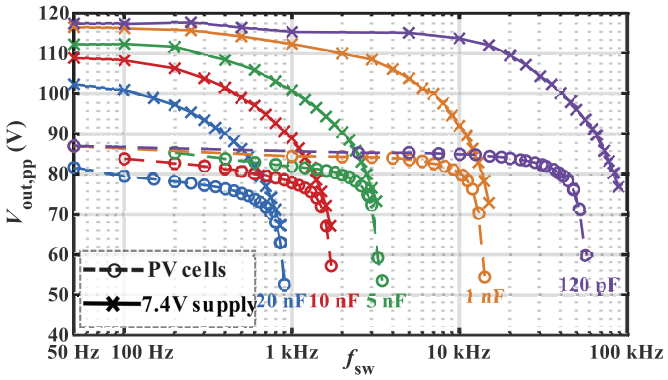

Fig. 18. Peak-to-peak output voltage versus switching frequency and load cap.

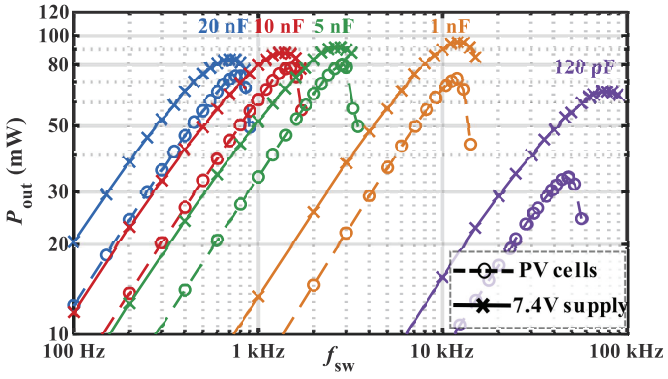

Fig. 19. Reactive output power versus switching frequency and load capacitance.

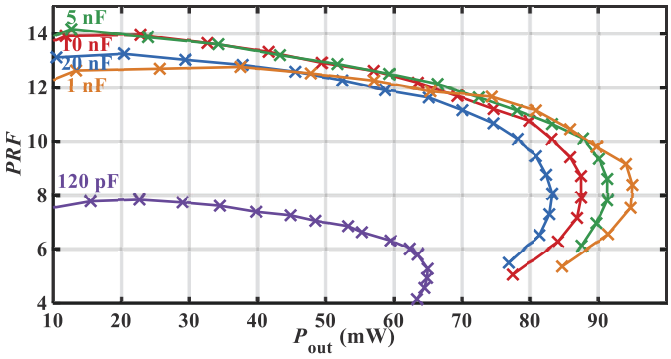

Fig. 20. PRF versus reactive ($CV^2 f_{sw}$) output power.

apparent. At light load (low load capacitance and low switching frequency), the SC circuit is in the slow switching limit (SSL) with maximum peak-to-peak driving capability. At higher load capacitance, the peak-to-peak driving voltage is reduced across the range due to the limitations in the energy storage of the flying capacitors. At higher load (either higher load capacitance or higher frequency), the circuit enters the fast-switching limit (FSL), here limited by switch resistance. For the PV-powered scenario, a third limit exists related to the power availability of the solar cells. For example, if power exceeding that available in the PV cells is required, their voltage will drop, reducing the overall peak-to-peak driving voltage. The fact that the PV and 7.4-V supply curves appear to converge at high load is coincidental; however, it can be seen that peak voltages are in correspondence with the 16× multiplication provided by the circuit in both cases. The peak driving voltage for the 7.4-V supply case was ∼ 117 V; for the PV-powered setup, it was just over 80 V.

Fig. 19 shows a similar perspective to Fig. 18, except that here reactive power is plotted versus frequency. In this case, the reactance of each load capacitor is carefully calibrated to determine the reactive power ($C_{\text{load}} V_{\text{out}}^2 f_{\text{drive}}$) provided across the frequency range. It can be seen that peak power depends, to some extent, on load capacitance. For example with small capacitance loads, high operating frequencies (up to 80 kHz) are needed to deliver maximum load power. In this case, frequency-dependent power consumption (in the level shifters, powertrain, digital logic, and so on) limits the performance of the circuit. On the other hand, for very large load capacitors, the energy stored in flying capacitors is not sufficient to drive the load to its full peak-to-peak voltage.

Notably, the system was able to achieve peak delivered reactive power of ∼95 mW while drawing significantly less real power from the system supply. Fig. 20 shows a plot of the measured PRF, defined in (3) as the ratio of reactive over real (supply) power. The peak PRF was just over 14 and remained above 10 for a wide range of load capacitance, drive frequencies, and delivered power levels. In this range, the circuit can deliver more than ten times higher reactive power than the power consumed from the supply. Phrased differently, compared to a conventional hard-switching driver [3], [11], with the same load and drive frequency, the system reduces real power consumption (from the system power supply, battery, or optical power source) by more than an order of magnitude.

The peak PRF of 14 is ∼88.5% of the ideal PRF of 16 for the 16-stage converter, demonstrating low-power-loss overhead in the converter circuitry. Based on the low-frequency PRF asymptote, quiescent and leakage-related power loss is below 10 μW, and this aligns with measurements of no-load leakage current, which is <250 nA for all supply voltages. Therefore, dominant losses in the converter (other than systematic hard-charging losses) are due to gate drivers, level shifters, and are frequency-dependent. When driving the 120-pF load capacitance, the PRF is reduced due to the higher (up to 80 kHz) switching frequency and associated switching losses in the converter.

Fig. 21 shows a slightly different perspective that is related to the PRF metric. Here, the driver was configured to drive a 10-nF load at a constant voltage of 100 V_{pp} as frequency was swept. Input power from the low-voltage system power supply P_{supply} (representing power as would be consumed from a system battery) was measured and plotted. Using the same 10-nF load, the hard-switching driver (previously published in [11]) was configured to drive the load to 100 Vpp. Note that the circuit in [11] requires an HV supply as it provides no dc–dc conversion. The power, in this case, was measured directly from the 100-V auxiliary supply required for this purpose. Note that in practice, the power consumed by the hard-switching

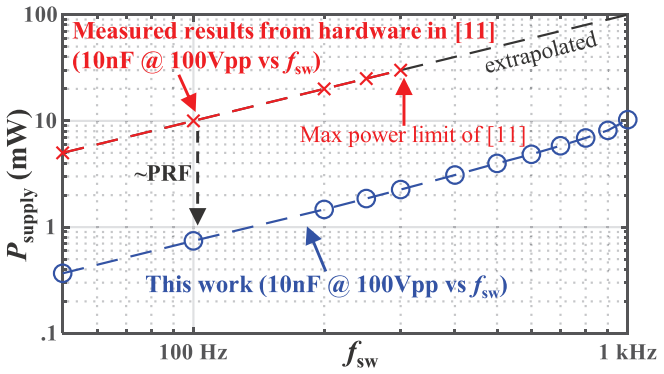

Fig. 21. Comparison to a hard-switching MEMs driver shows supply power, P_{supply} (as would be consumed from a system battery or power supply), versus drive frequency (f_{sw}) for a 10-nF load driven at 100 V_{pp}. It includes measured data from the same hard-switching driver previously published in [11].

driver would be even higher if accounting for the need for a dc–dc boost converter to provide its 100-V supply. As shown in Fig. 21, the power consumed by the pseudo-adiabatic driver (this work) is more than an order of magnitude lower than the power required by the hard-switching driver [11]. Furthermore, the power reduction achieved closely matches the value of the PRF achieved in Fig. 20 for the same conditions. This is because the PRF metric can be interpreted as the ratio of power required for an ideal hard-switching driver [11] over the power required by an efficient solution. This shows more directly the advantages of the approach and helps to highlight the value of the PRF metric for comparison of solutions.

VII. Conclusion

This article presented an efficient, HV MEMs actuator driver in a 650-V SOI CMOS process, powered either by an optical energy source or single off-chip battery. A metric, PRF, was introduced to quantify the performance of systems delivering dominantly reactive power. The system used a reconfigurable series–parallel SC converter to drive reactive MEMs loads with a pseudo-adiabatic process, reducing hard-charging losses and recovering energy during discharge cycles. On-chip solar cells used deep-trench isolation such that they could be stacked and arbitrarily reconfigured in series and parallel domains while receiving energy from an optical power source. The series–parallel converter was able to achieve peak drive voltages of between 80 and 117 V and operating frequencies over 50 kHz. With on-chip PV cells, it was able to mitigate high mismatch and variation, providing effective boost operation and wireless driving capability. The peak PRF was over 10 across a wide range, showing that the system can reduce power consumption by over an order of magnitude compared with conventional hard-switching drivers.

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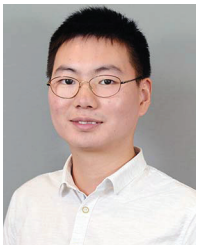

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