Active Channel Impact on SiC MOSFET Gate Oxide Reliability

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***Abstract*— It is well known that SiC MOSFETs have relatively susceptible gate oxide causing reliability concerns. Therefore, it is essential to identify gate oxide fault mechanisms under realistic conditions. The goal of this paper is to evaluate the load current impact on gate oxide degradation of SiC MOSFETs. For this purpose, conventional high electric field test (HEF) and active channel gate bias test (ACGB) are carried out under electro-thermal stress and the results are compared. During ACGB tests, both gate and drain biases applied to the device at high temperatures, and device channel is forced to conduct under various load currents. After tunning both tests, gate oxide degradation precursors such as threshold voltage and gate leakage are investigated, and the findings are compared to each other. In addition, load current impact on device consumable lifetime is evaluated, and possible failures and root causes are discussed. It is shown in the experimental results that the conductive channel with high drain-source current introduces severe device instability due to degradations and conventional HEF tests can be misleading and yield overestimated device lifetime.**

Keywords—Accelerated aging, gate oxide, lifetime, reliability, SiC MOSFET

I. Introduction

Compared to Si based power semiconductors, SiC MOSFET shows superior performance in high voltage, high frequency and high temperature applications. Even though SiC MOSFETs own much lower on-state resistance ($R_{ds\text{-}on}$) compared to Si devices, they have a much thinner and susceptible gate oxide in order to achieve reasonable threshold voltage (V_{th}) and transconductance [1]. Hence, evaluation of gate oxide degradation under various operating conditions is crucial to verify device ruggedness for lifetime assessment.

Because of the thin oxide structure, time dependent dielectric breakdown (TDDB) of SiO_2 layer in SiC MOSFETs is reported as the main reliability concern especially under elevated temperature [2]. Even though the applied gate-source bias barely exceeds the intrinsic breakdown value during normal operation, it can gradually generate defects and degrade the oxide layer [3]. Dielectric lifetime model (E-model) has been widely used to describe the TDDB process of gate oxide with high temperature stress [4]. In E-model, the expected consumable lifetime of gate oxide is reduced depending on the electric field (E-field) across SiO_2 layer and device's junction temperature. On the other hand, compared to Si/SiO2, SiC/SiO2 interface quality is poor since the geometry of SiC surface is not suitable for an abrupt oxide surface [5]. Hence, higher density of defects and trap at the SiO2/SiC interface is hard to avoid during manufacturing. In addition, applied positive gate bias at elevated temperatures increases device V_{th} over the device lifetime [6]. This reported gate-source voltage (V_{gs}) induced device's parametric shift and degradation is called bias temperature instability (BTI) [7].

In order to trigger and assess device degradation within relatively short time, accelerated lifetime tests apply severe electro-thermal stresses to the devices [8]. Among various aging tests tailored for SiC MOSFETs, high electric-field (HEF) test is widely adopted for gate oxide reliability studies including lifetime extrapolation and aging precursor identification [9]. In HEF test, voltage stresses are consistently applied at either gate or drain electrode whereas no load applies to the DUT. However, in real converter operation, a conducted inversion layer is expected compared to conventional HEF test with static stress.

In this study, besides gate bias and high temperature, the channel of SiC MOSFET is actively conducted with various load currents. During which, devices' aging precursors and consumable lifetimes are investigated. For comparative study, conventional HEF stress test is also conducted under the same gate to source voltage (V_{gs}) and junction temperature (T_j). In Section II, the proposed active channel test is illustrated in detail and its comparison with conventional HEF is carried out. Section III evaluates device degradation pattern and aging traits in both tests. Based on device characterization results over lifetime, aging analysis and discussion is carried out in Section IV.

II. Gate Oxide Accelerated Aging

A. High E-field Test

In this study, SiC MOSFET with 1kV blocking voltage, 22A rated drain current (I_d) and 15V rated V_{gs} is used as device under test (DUT). Throughout HEF test, DUTs' gate oxide degradation pattern and consumable lifetime are collected under gate-source bias stress only. In HEF test circuit, drain and source electrodes of each DUT are shorted to ground. In order to apply HEF across gate oxide, positive gate biases are added to gate-source. It can be expected that the DUT may survive over decades if V_{gs} under rated value are used at room temperature. Therefore, V_{gs} values higher than rated gate bias range are employed to accelerate DUTs' aging [6]. In this test, 30V V_{gs} is applied in this study for a 40nm gate oxide in order to achieve E-field strength more than 7 MV/cm.

On the other hand, an external gate resistor ($R_{g,ext}$) is deployed in HEF aging setup for each DUTs which is useful for the test in several aspects. First, $R_{g,ext}$ damps the gate loop with higher RC time constant so that voltage spikes which are generated during HEF test start-up can be mitigated. Second, it mimics the gate driver loop in real

converter applications. Third, by sensing the voltage drop across $R_{g,ext}$, device's ramped gate leakage current (I_{gss}) can be captured as failure precursor in real-time and DUT's lifetime is collected [10]. Additionally, forced air oven is used to provide consistent elevated temperature to the DUT. Throughout DUTs' lifetime in HEF test, DUTs are disconnected from the setup periodically (24 hours) and plugged into automated curve tracer for characterization at room temperature. Electric parameters including V_{th}, I_d-V_{gs} curve are measured over lifetime.

B. Active Channel Gate Bias Test

The schematic of the proposed active channel gate bias (ACGB) test is shown in Fig. 1. Compared to HEF test, the channel of device under test (DUT) conducts under tunable load current. As depicted in Fig.1, the voltage drop across $R_{g,ext}$ is monitored in real-time during accelerated aging. Once the measured I_{gss} exceeds maximum acceptable value which is indicated by datasheet (250nA), gate signal is pulled to low and DUT lifetime is recorded. Similar to HEF test, periodic characterization in automated curve tracer is conducted during the ACGB test.

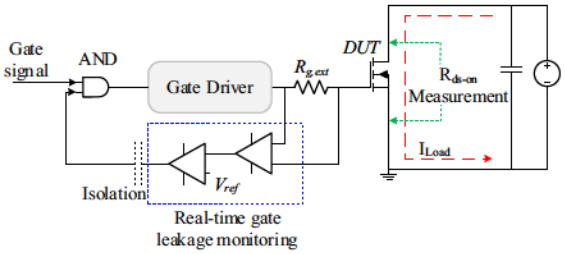

Figure 1. Schematic of proposed ACGB test

Unlike HEF test, a temperature mismatch between junction to case is expected in ACGB test due to device's power dissipation. Hence, accurate real-time T_j sensing is needed during accelerated aging. DUTs are tightly attached to a hot plate for lifetime acceleration purpose and T_j difference caused by load current are compensated to enable accelerated aging under the same temperature in both HEF and ACGB tests. Another challenge during ACGB test is to maintain DUTs' aging conditions consistent over the whole test procedure including gate bias, temperature and load current. Both issues are discussed and verified as follows.

B1. Accurate T_j Sensing

Since directly decapsulating the device mold compound may affect the thermal conductivity of device, temperature sensitive electric parameter (TSEP) is preferred to obtain real-time T_j during the test. Even though TSEPs such as V_{th}, R_{ds-on} can be used to measure T_j, studies have shown that these parameters are also aging dependent [11]-[15]. Considering the high gate bias applied during the test, DUTs' R_{ds-on} are characterized at different V_{gs} in automated curve tracer over temperature before and after HEF stress in Fig. 2. As observed, the shifted V_{th} and R_{ds-on} causes more than 10°C temperature measurement error within DUT's rated temperature range (150°C). However, if higher V_{gs} (27V) is used for channel conduction, the T_j measurement error can be significantly reduced to no more than 1°C.

It can be explained by the correlation between device's channel resistance and threshold voltage in strong-inversion mode under positive gate bias, which is given as follow:

$$R_{CH} = \frac{L_{CH}}{Z\mu_{ni}C_{ox}(V_{gs} - V_{th})} \quad (1)$$

where L_{CH} is the channel length, Z stand for channel width, μ_{ni} stand for electron mobility and C_{ox} stands for gate oxide capacitance per unit area. Equation (1) reveals that when V_{gs} increases, the impact of a fixed value of ΔV_{th} on R_{CH} is gradually decreased. Hence, it can be concluded that the device channel resistance result in slight gate oxide degradation due to high gate bias compared to V_{gs} values normally applied in real converters.

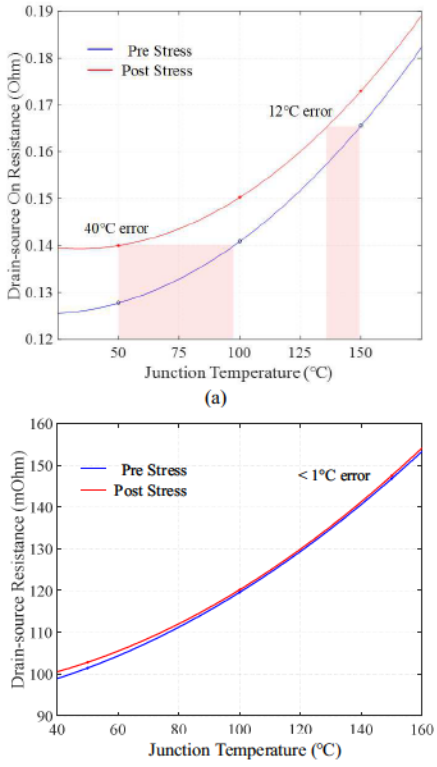

Figure 2: R_{ds-on} shift before and after stress at (a) 15V and (b) 27V V_{gs}

Therefore, DUT's R_{ds} at high gate bias are verified to be temperature dependent but aging independent. In the proposed ACGB test setup, it is employed for DUT's T_j monitoring to enable fair comparisons between conventional HEF test and proposed active channel test.

B2. Aging Condition Consistency

Another advantage of the verified aging independent R_{ds} at strong E-field is keeping DUT's T_j consistent throughout the ACGB test. In order to verify both T_j sensing accuracy and aging condition consistency, a preliminary ACGB test is applied at 30V V_{gs} and 5A load current for 50 hours.

Prior to the test, the samples are characterized first over a temperature range using automated curve tracer and oven. A T_j calibration curve is obtained by collecting its R_{ds} values under 30V V_{gs} at various temperatures. Also, the SiC MOSFET sample is decapsulated by removing mold compound. During the ACGB test, its T_j is directly measured by an IR camera and drain-source voltage is measured by oscilloscope in real-time. As shown in Fig. 3,

over 50 hours of continuous aging, device temperature is proved to be consistent. Furthermore, in order to avoid T_j mismatch, all DUTs are characterized before aging tests and

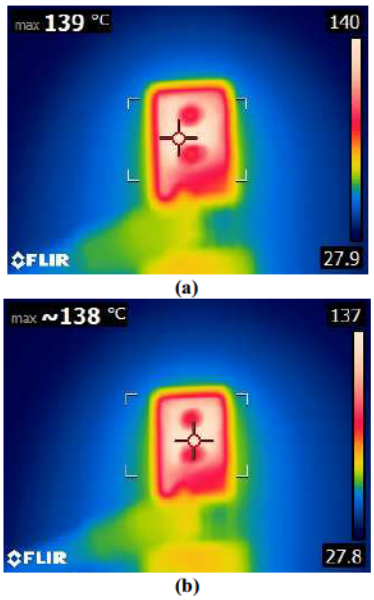

Figure 3. Direct T_j measurement at (a) 0 hour and (b) 50 hours of ACGB test with 30V gate bias

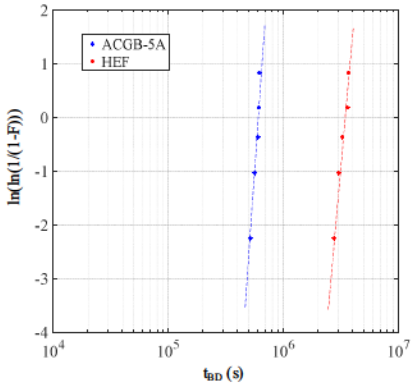

Figure 4. Weibull distribution of t_{BD} in both HEF and ACGB tests

outliers with different $R_{ds\text{-}on}$ compared to others are excluded from both HEF test and ACGB test.

III. Aging Assessment and Characterization

A. Consumable Lifetime

In HEF test, 5 DUTs are simultaneously aged at 140°C under 30V V_{gs}. It is observed that all DUTs function normally for the first 700 hours and the first failure observed after 760 hours. On the other hand, all devices under 30V V_{gs} ACGB test are exhibit gate oxide failure and high gate leakage within 300 hours. The time-to-breakdown (t_{BD}) Weibull distribution of both tests are plotted in Fig. 4. It can be concluded that device degradations are largely accelerated by conducted load current under high gate bias. The effect of different load current levels on gate oxide lifetime is not significant, yet higher load current flowing through device's channel results in shorter consumable gate oxide lifetime.

On the other hand, DUTs' end-of-lifetime failure modes after HEF and ACGB tests are quite different. In HEF test, both drain and gate leakage are observed and device short-

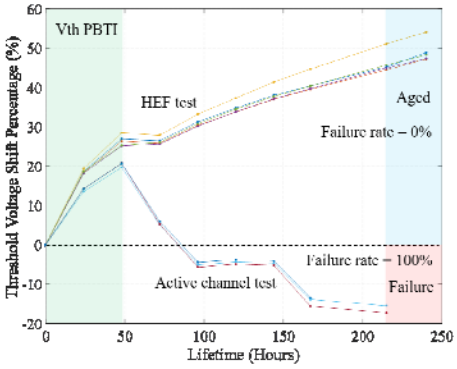

Figure 5. V_{th} comparison of HEF and ACGB tests

circuit is verified as failure event. However, in ACGB test, most DUTs exhibit open-circuit fault with high gate leakage whereas drain leakage current remains low and DUTs still maintain high voltage blocking capability.

B. Device Characterization

During both tests, DUTs' V_{th} and transfer characteristic curve are measured by curve tracer as gate oxide aging precursors [16]. It is revealed in Fig. 5 that in HEF test, device V_{th} increases due to gate oxide degradation with positive-BTI (PBTI). However, the active channel introduces strong instability in device V_{th} and eventually reduces V_{th}.

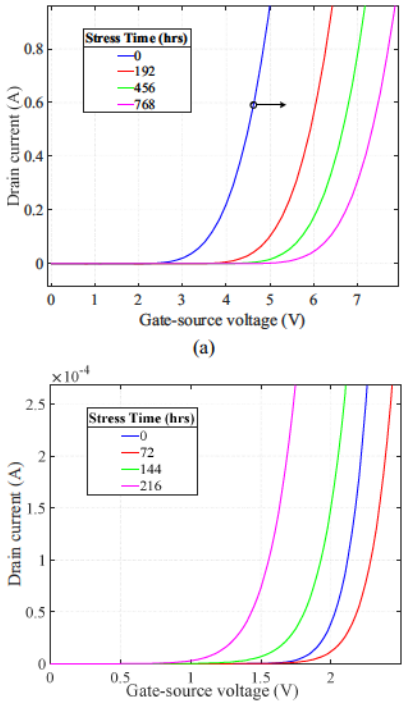

Figure 6. I_d-V_{gs} curve comparison of HEF and ACGB tests

DUTs' transfer characteristic curve changes are depicted in Fig. 6 during aging. Instead of setting V_{ds}=V_{gs} like in V_{th} measurements, a consistent V_{ds} (20V) is applied across the

DUTs, and I-V curves are obtained by sweeping V_{gs} value. Compared to V_{th} assessment results, a subthreshold retardation in I-V curve is observed during HEF test and an unstable I-V shift is observed during ACGB test.

IV. Failure Analysis and Discussions

Since DUT's drain and source electrodes are shorted to ground in HEF test, the E-field applied across SiO_2 layer is evenly distributed. However, due to the load current flowing through channel in ACGB test, finite voltage drop is expected due to DUT's channel resistance. Therefore, a higher E-field is expected across gate-source compared to gate-drain. The widely adopted E-model for dielectric TDDB lifetime is given as:

$$TF = A_o \cdot Exp(-\gamma E_{ox}) \cdot Exp(Q / K_B T) \qquad (2)$$

where A_o, γ, Q and K_B are constant for certain dielectric configuration and E_{ox} stands for E-field across SiO_2. It is expected that the electro-thermal stress is more severe at gate-source. Consequently, high gate leakage is expected at the end-of-life and device fails open. In summary, compared with HEF test which fully degrades the gate oxide layer, ACGB test mimics a real application and more realistic failure modes.

Compared to conventional HEF test, strong transfer characteristic instability is observed after ACGB test. Such result implies that additional aging mechanisms affect device's gate oxide when channel actively conducts at high gate bias. Multiple mechanisms possibly accelerate device degradation and impact gate oxide lifetime as discussed below.

First, the elevated temperature reduces the barrier height between SiC and SiO_2 and causing gate leakage increment. Hence, device lifetime is accelerated because of lower gate-oxide breakdown voltage [17]. In this study, DUTs used in HEF test and ACGB test are subjected to the same junction temperature. Therefore, T_j as the lifetime acceleration factor is compensated and excluded from the root cause of the strong V_{th} instability in ACGB test.

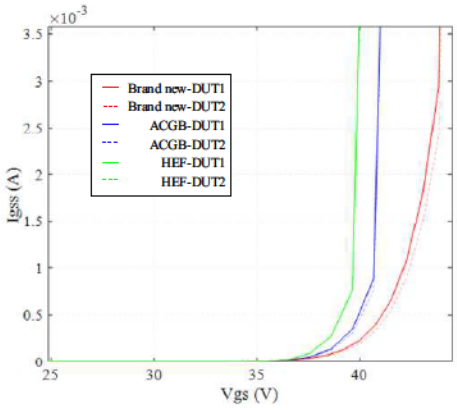

Figure 7. I_{gss} measurement for both HEF and ACGB tests

Second, the injection of electrons into near-interface gate-oxide traps is expected as one of the main root causes of V_{th} increase in HEF test [18]. In case of electron injection, a higher gate breakdown voltage is expected since the applied gate voltage not only needs to provide enough charge for SiO_2 breakdown but also compensate the near-interface E-field relaxation caused by charged traps. For verification, curve tracer is used to measure DUT's I_{gss} under both HEF and ACGB tests after 144 hours, and the result is shown in Fig. 7. As observed here, both tests induce higher gate leakage in DUTs compared to initial conditions and results in lower oxide breakdown voltage. Due to the mismatch between experimental results from both HEF and ACGB test in Fig. 7, it is concluded that such interface trap charge doesn't dominate gate oxide degradation in both tests.

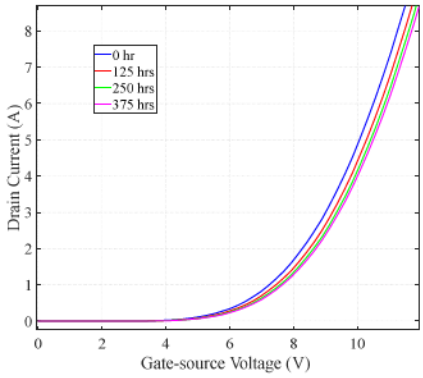

Figure 8. I–V measurement for ACGB test with 15V V_{gs}

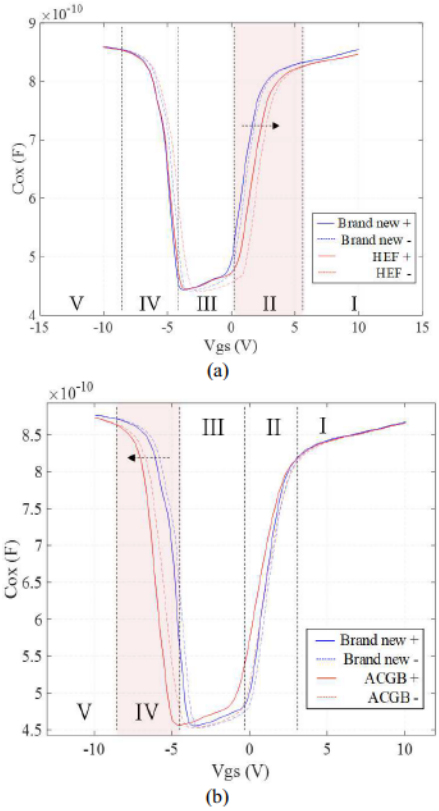

Figure 9. I_d-V_{gs} curves comparison of HEF and ACGB tests

It can be concluded from reduced V_{th} in ACGB test that the electron-charged trap density decreases at both gate-oxide interface and near-interface. As a possible reason, the reemission of electrons trapped at interface is expected to be aggravated in ACGB test due to the applied drain-source voltage [19]. Also, since strong E-field (30V V_{gs}) is applied in ACGB test, Fowler-Nordheim (F-N) tunneling current

dominates gate-oxide current flow instead of trap assisted tunneling [20]. To verify the aging mechanisms difference induced by wide range of gate bias applied during load current conduction, a make-up test is conducted in Fig. 8 by applying the same 5A to the DUT but only 15V gate bias is used. Though it's hard to trigger device's gate oxide failure with such low gate bias, a consistent I-V characteristic retardation and V_{th} increment can be observed. Hence, it can be concluded that when strong E-field applies on SiC MOSFET gate oxide attributed by either high gate bias or thin oxide, device's lifetime is drastically shortened because of the induced F-N tunneling current.

For the same purpose, device gate oxide capacitance (C_{ox}) measurement is obtained over gate bias in wide range. For TO-247 packaged device, its drain and source electrodes are shorted and a high frequency (1MHz) voltage sweep (100mV) is applied on gate for an approximate C_{ox} evaluation. Fig. 9(a) depicts C_{ox} measurement on DUT at healthy and post-HEF stress state, where solid line represents a positive gate bias sweep and dashed line represents a negative sweep. As depicted, a positive shift in section II is observed for HEF test and implies a positive shift of V_{th} and negatively charged traps exists within gate oxide [21]. On the contrary, section IV in Fig. 9 (b) shows an accumulation of positive charge emerges within gate oxide over ACGB test [22]. Therefore, a possible aging mechanism can be concluded for devices which are operated in high bias with active channel. Specifically, F-N tunneling which is exaggerated by high gate bias enables electrons trapped at interface/near-interface to tunnel through the gate oxide. While current flows through the gate oxide, acceptor type traps are generated, results in device's V_{th} instability and accelerated gate oxide lifetime.

In power converters, switching transients with high dv/dt may cause crosstalk in phase-leg configurations [23]. Consequently, V_{gs} overshoot which is higher than rated gate bias range is expected, causing the observed aging mechanism and shorten device's gate oxide lifetime. From gate driver development aspect, gate bias selection and gate driver loop should be optimized in order to obtain both lifetime refinement and high performance with fast switching speed and low $R_{ds\text{-}on}$.

V. Conclusion

In this study, the active channel impact on SiC MOSFET gate oxide degradation is evaluated. Comparison between HEF and ACGB test indicates that device instability is exaggerated when device channel is actively conducted under various load current. In ACGB test, device's V_{th} gradually decreases at degradation state while in HEF test, its V_{th} continuously increases over lifetime. Experimental results also reveal that conducted channel has negative impact on consumable lifetime. Moreover, open-loop fault is observed as device's end-of-life failure mode in ACGB test, which is closer to real system applications compared with conventional gate bias test. It is thought that the root cause of V_{th} decrement and shorter lifetime in ACGB test is electrons re-emission at SiO_2/SiC interface and drastic F-N tunneling. In order to fulfill and verify analytical discussions, comprehensive device interface trap assessment tests including I_{gss} and C_{ox} evaluation are presented.

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