Electrical Insulation Design and Accurate Estimation of Temperature via an Electrothermal Model for a 10 kV SiC Power Module Packaging

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***Abstract*— Wide-bandgap (WBG) power devices can tolerate higher currents and voltages than their silicon (Si)-based counterparts. However, the realization of their superior characteristics is tied to the reliability of their packaging, where thermal management and reliable electrical insulation design are the most challenging tasks to this end. Not taking care of the former one leads to thermal runaway, and the latter one causes the electric breakdown of the whole module. In this paper, the packaging design of a 10-kV SiC diode is studied by addressing both challenges above. Electrical insulation design is carried out through a finite element method (FEM) electric field calculation model developed in COMSOL Multiphysics, meeting both the one-minute insulation and PD tests based on IEC 61287-1. Through developing an electrothermal model and for considered dimensions, an accurate estimation of the junction temperature is obtained to determine the maximum load current of the module.**

I. INTRODUCTION

Due to the increasing demand for small-footprint, low-weight, and cost-effective power conversion systems, WBG power modules made from SiC and GaN that are capable of tolerating higher currents, voltages, and temperatures than Si-based ones have attracted noticeable attention. From the electrical insulation side, since besides targeting higher voltages, the size of the WBG power packages are being reduced, this translates into higher electric stress within the module. This high electric field creates an extremely poor environment for insulation systems in envisaged high voltage high-density WBG modules where partial discharges (PDs) have the most impact on insulation degradation [1-13]. Four solutions have been proposed for electric field reduction and PD control within envisioned high voltage, compact packaging design of power modules: 1) geometrical techniques [14-16], 2) applying nonlinear field-dependent conductivity (FDC) materials as coatings on high field regions [17] or field-dependent permittivity (FDP) fillers in silicone gel [18], 3) using high-temperature (up to 350°C) insulating liquids as a potential replacement for silicone gels [19], and 4) combined geometrical techniques and applying nonlinear field-dependent conductivity layers [20-28]. As an example of the trend towards higher currents, the existing maximum heat flux of IGBTs in hybrid electric vehicle power electronics of 100-150 W/cm^2 is expected to reach up to 500 W/cm^2 soon [29]. However, operating at higher currents, the chip junction temperature increases significantly due to the Joule heating. Heat losses are caused due to 1) conduction loss in the on-state situation and 2) switching losses. Although SiC and GaN-based devices can survive at temperatures much higher than Si-based ones that are limited up to 150°C for 6 kV [30], due to the limit on the operating temperature of packaging materials, especially silicone gel, their junction temperature is limited to 175°C [31]. Thus, in this paper, this limit (175°C) is considered when determining the maximum load current of the SiC module. The thermal increase within the module also impacts the electrical characteristics of different components in the power module. Double-sided cooling, jet impingement, spray cooling, and microchannel heatsink, [32-34], are thermal mitigation solutions introduced to date. The packaging components of a power module experience a combination of electrical, thermal, and mechanical stresses, which may affect each other as well. Thus, considering the impact of each stress without taking account of the effect of other stresses on it may result in inaccurate evaluation. On the other hand, experimental methods presented to measure the junction temperature of the chip are via thermocouple, infrared thermal scanner, and pressure drop method. In addition to the lack of sufficient accuracy, the mentioned experimental techniques cause permanent damage to the device as well as they are not cost-effective especially for designing a new prototype. To address these issues, Multiphysics models have been developed in either circuit simulators such as PSpice and Simulink based on RC network models or FEM-based tools such as COMSOL Multiphysics and ANSYS, or analytical approaches, [35-37] to consider coupling effects of stresses and obtain an accurate estimation of temperature within a power module. Each of these methods has drawbacks such as insufficient accuracy, high computational time, or applicable for elementary geometries, respectively. In this paper, using the method introduced in [35] as a combination of FEM simulations and RC network modeling, temperature distributions within the chips are obtained in a fast and accurate way. The method is used to design the packaging for a 10-kV module consisting of 9 SiC PiN diodes. Temperature-dependency of the electrical characteristics of the chip is considered and the maximum load current is determined. The paper provides a framework for dimensioning and ratings of the next-generation of WBG power module packaging to address both electrical insulation and thermal stress challenges.

II. ELECTRICAL INSULATION DESIGN AND THERMAL ANALYSIS

The 3D schematic of the proposed 10 kV power module modeled in COMSOL Multiphysics is shown in Fig. 1. In the power module, SiC PiN diodes are soldered in parallel on a

DBC layer. The DBC layer, which consists of a ceramic substrate sandwiched between two copper layers, provides electrical insolation between the dies on its top-side and the grounded heatsink at its bottom side.

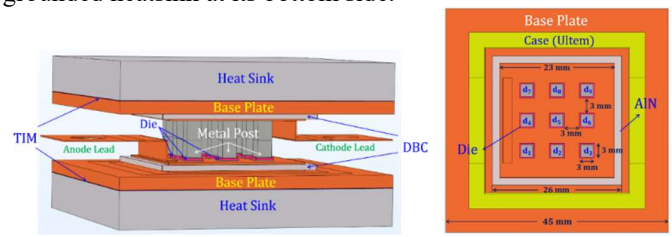

Fig. 1. 3D schematic view of the 10-kV power module with its dimensions.

Although Al_2O_3 is the most economical choice, it has a thermal conductivity of 10-15 times smaller than AlN. Thus, AlN is considered as the substrate in this paper, as shown in Fig. 1. Using a double-sided heat sink provides two paths for the heat transfer to the ambient and ensures better cooling. To reduce the parasitic inductance and eliminate the risk of wire-bond breakage in thermal cycling, metal posts introduced in [38] and made from Molybdenum (MO) are used for chips interconnection and circuit joints. The usual existing encapsulant, silicone gel, is used to avoid PD from occurrence with air and protect the module components against environmental impact.

A. Electrical Insulation Design

The only available standard for testing PD and electrical breakdown performance of power modules is IEC 61287-1. From its one-minute insulation test, the minimum thickness of the ceramic substrate can be determined where a 50/60 Hz ac voltage with an RMS value of $2U_b/\sqrt{2}+1\ kV$ (U_b $[kV]$: blocking voltage) is applied to the DBC for one minute. Considering the dielectric strength of the metalized AlN of 25 kV/mm [20], a minimum thickness of 0.86 mm is required to pass the test. This thickness of AlN was used for simulations of the PD test. To simulate the PD test recommended in IEC 61287-1, the maximum voltage applied to the chips should be $1.1U_b$ =11 kV. To reduce the electrical stress on the chips, this voltage is applied to the module symmetrically: $V = 5.5\sin(100\pi t)$ kV to the Anode lead and $V = -5.5\sin(100\pi t)$ kV to the Cathode lead. Because of the symmetry and for reducing the computational time, the electric field simulations were carried out for the 2D model. Guidelines for choosing proper meshing strategy and measuring lines (L_1 in AlN and L_2 in silicone gel) presented in [20, 21] are followed. Figs. 2a and 2b show electric field distribution and measuring lines, and meshing strategy, respectively. The maximum electric stresses on L1 and L2 are 18.02 kV/mm and 18.5 kV/mm, respectively that are less than the dielectric strength of AlN (25 kV/mm) and silicone gel (25 kV/mm at T=25°C).

B. Thermal Analysis

In a power module, the heat generated in dies at the on-state is transferred through the beneath layers including solder and DBC to the base plate and heat sink, and then to the ambient. Typically, a thin layer of thermal grease, 100 µm, is added between the base plate and heat sink shown in Fig. 1 as TIM to reduce the contact thermal resistance [39]. The total thermal resistance of the module is determined by the sum of thermal resistance of all layers available within the conduction path. As mentioned in Section I, the thermal management of the module aims to maintain the junction temperature below the maximum temperature of 175°C. Among all types of heat transfer in solids—conduction, convection, and radiation— the dominated one in power modules is conduction [39]. As in power modules, the source of heat flux is semiconductor dies, the factor of the position-dependent heat source can be eliminated from the heat conduction equation and it can be simplified to:

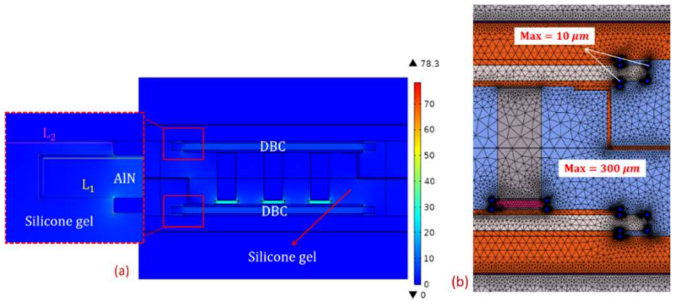

Fig. 2. (a) Electric field distributions and measuring lines (L_1 and L_2), (b) meshing strategy.

$$\kappa\left(\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}\right)=\rho c\frac{\partial T}{\partial t} \tag{1}$$

where κ is the thermal conductivity, ρ is the mass density, and c is the specific heat capacity. Since the ratio of the thickness to the width for each layer within the power module is close to zero, the heat conduction process can be reduced to a one-dimensional problem, from the top of the chip to the bottom of the heat sink. Considering z as the heat conduction direction, (1) is simplified to:

$$\kappa\left(\frac{\partial^2 T}{\partial z^2}\right)=\rho c\frac{\partial T}{\partial t} \tag{2}$$

The boundary conditions for the thermal analysis can be defined as heat flux at the top surface of each chip, (3), and the convection heat transfer from the heat sink to air, (4).

$$\kappa_c\frac{\partial T_c(z)}{\partial z}\left[z=z_{\text{chip\_topside}}\right]=-Q_{in}=-\frac{P_{in}}{A} \tag{3}$$

$$\kappa_H\frac{\partial T_H(z)}{\partial z}\left[z=z_{\text{Heatsink\_bottomside}}\right]=-h(T_H-T_{Amb}) \tag{4}$$

where κ_c and κ_H are the thermal conductivity of chips and heat sink, respectively; Q_{in} is the input flux, P_{in} is the input power, A is the surface area perpendicular to the heat flux direction, and h is the convection flux coefficient. T_{Amb} is the ambient temperature which is set as 293.15 K (20°C) and T_H represents the heat sink temperature. The natural free heat convection to air at room temperature is 5-25 $W/m^2.K$ that is corresponding to the dissipated heat flow of 150-1500 W/cm^2 [39]. A slab made from Aluminum 6063-T83 is considered for the heat sink that is cooled by a mix of water and ethylene glycol (50%/50%).

Fig. 3 shows different heat transfer layers for die #5 of the packaging design shown in Fig. 1 where temperatures at nodes a, b, c, and d located on the active-chip top-surface, active-chip bottom-surface, bottom of the DBD copper layer, and bottom of the base plate, respectively, are obtained from an

electrothermal model developed in COMSOL. Temperature values are inserted in (5) and (6) to obtain the thermal resistance corresponding to each layer and the cross-heating of the chips.

$$R_{ill'} = \frac{T_m - T_{m-1}}{P_{loss-d_i}} \quad l, l' = J, S, D, B, A\,;\ m = a, b, c, d \quad (5)$$

$$R_{i-jC} = \frac{T_{d_j} - T_A}{P_{loss-d_i}} \qquad i, j = 1 \ldots 9 \quad (6)$$

where $R_{ill'}$ is the thermal resistance between layers l and l', and R_{i-jC} represents the thermal resistance of the neighboring chips induced by the power loss in the active chip. P_{loss-d_i} is the power loss in the active chip. The letters $J, S, D, B,$ and A are assigned to junction, solder, DBC, base plate, and ambient.

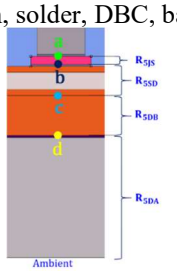

Fig. 3. Thermal resistance of different heat transfer layers for die #5.

The self-thermal resistance of diode i is the sum of thermal resistance of each layer placed within the conduction path:

$$R_{iS} = R_{iJS} + R_{iSD} + R_{iDB} + R_{iBA} \quad (7)$$

where R_{iJS}, R_{iSD}, R_{iDB}, and R_{iBA} are self-thermal resistance of junction to solder (node a-b), solder to DBC (node b-c), DBC to base plate (node c-d), and base plate to ambient (node d to ambient). Junction temperature of each chip within the device, T_{Jd_i}, is calculated through the following thermal resistor matrix:

$$\begin{bmatrix} T_{Jd_1} \\ \vdots \\ T_{Jd_9} \end{bmatrix} = \begin{bmatrix} R_{1S} & \cdots & R_{1-9C} \\ \vdots & \ddots & \vdots \\ R_{9-1C} & \cdots & R_{9S} \end{bmatrix} \times \begin{bmatrix} P_{loss\ 1} \\ \vdots \\ P_{loss-d_9} \end{bmatrix} + \begin{bmatrix} T_A \\ \vdots \\ T_A \end{bmatrix} \quad (8)$$

The thermal grease layer which is used usually between the base plate and heat sink imposes a nonlinearity on the heat diffusion process within the module. Thus, the calculated junction temperature without considering the nonlinearity characteristics of the thermal path parameters is not accurate. In this regard, the nonlinearity equation for R_{iBA} and the coupling thermal resistances (R_{i-jC}) should be considered. The convection coefficient, h, can be determined by (9)

$$h = \frac{9 \times P_{loss-d_i}}{(T_{\text{base plate}} - T_{\text{amb}}) \times S} \quad (9)$$

As seen from (9), for a given amount of S, different power losses in chips result in different values of h. Thus, to have an accurate electrothermal simulation, it is essential to obtain the nonlinear equations corresponding to each thermal resistance which will be later used as the parameters of the Foster R-network. Thus, as the first step, the thermal resistance of each layer of the module is calculated at different h values. Considering $T_{\text{base plate}}$ and T_{amb} as 40 and 20°C, respectively, the heat sink area of $S = 45 \times 45\ mm^2$, for $h = 1000$, 2000, 3000, 4000, 5000, 6000, and 7000 $W/m^2.K$, P_{loss-d_i} will be 4.5, 9, 13.5, 18, 22.5, 27, and 31.5 W, respectively. The next step is to determine the thermal resistance of different layers of the module at each h and P_{loss-} . To calculate the thermal parameters for the Foster R-network, seven steady-state FEM simulations using COMSOL Multiphysics are carried out for seven values of h and P_{loss-d} mentioned above and the calculated thermal resistances are fitted as a power equation of $F(x) = ax^b + c$. To build the electrothermal model, the Foster R-network with considering the coupling effect of the chips and the nonlinearity behavior of thermal resistances at different loads is modeled in PLECS which is a simulation platform for power electronic systems. The aim of the electrothermal analysis in this paper is to estimate the maximum amount of current that can flow through each chip to meet the junction temperature limit of 175°C. In electrothermal simulations, power loss is provided by an electrical circuit that is coupled to the thermal circuit. The on-resistance of the semiconductor die has a decisive role in the magnitude of power loss generated in the chip. The on-resistance of dies, R_{on} , is temperature-dependent as shown in Fig. 4 for the SiC PiN diode considered in this paper of the GA01PNS80-CAL model [40].

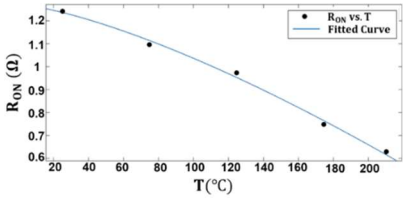

Fig. 4. R_{on} of GA01PNS80-CAL vs. temperature [40].

Accordingly, to improve the accuracy of the junction temperature calculations, the R_{on} of the active chip was considered as a function of the temperature. To determine the maximum load current that the package can withstand regarding the junction temperature limit of 175°C, several simulations in PLECS were performed for different current sources in the 2-12A range as shown in Fig. 5. The simulation results indicate that at $I = 10\ A$ for each die, the junction temperature reaches 180.31°C, and the temperature at solder, DBC, and base plate are 175.5°C, 147.6°C, and 143.13°C, respectively. Since the SiC chip can survive at temperatures much higher than 200°C, and the estimated temperature at the other locations of the module is 175°C or less, the maximum load current of the module should not exceed 9×10=90 A.

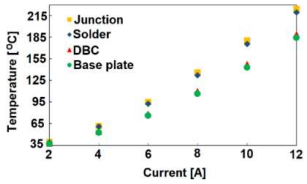

Fig. 5. The calculated temperature at different locations of the power module vs. different load currents.

III. Conclusions

The compact packaging design of envisaged high voltage WBG power modules brings many challenges in terms of thermal management and electric field enhancement. The thermal issues within the power module originated from the heating of the chips in their on-state while electric stress occurs at the off-state of the chips and close to their breakdown voltage. To ensure reliable operation of WBG power modules in both states, accurate thermal and electric field analyses are essential. In this paper, a packaging design with a double-sided cooling system

and parallel metal posts to hold 10-kV SiC PiN diodes on a DBC made from AlN is presented. Through FEM electric field simulations in COMSOL, the thickness of AlN was determined. In the thermal side, through FEM simulations carried out combined with thermal network analysis developed in PLECS, the convectional coefficient of the cooling system and the junction temperatures for different loads were obtained and for the proposed packaging design, a maximum load current of 90 A for the module has resulted.

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