

Heterogeneous Integrated Sparse Optical Phased Array for Free-Space Optical Communication

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Abstract—We present a new design for high-power, large-scale optical phased arrays (OPA) based on heterogeneous integration of SOI and SiN photonics. The OPA consists of sparsely spaced subarrays on SOI chiplets 3-D integrated on a SiN interposer. Simulation results demonstrate the performance.

Index Terms—Optical phased array, 3-D integration, sparse array, free-space optical communication.

I. INTRODUCTION

Free-space optical (FSO) communication technologies are well suited for future space and airborne systems such as unmanned aerial vehicles (Fig. 1) if they can meet the stringent performance goals and SWaP-C (Size, Weight, Power and Cost) requirements. We seek to develop solid-state FSO devices operating at near-infrared (NIR) with large optical power, narrow beamwidth, and agile beamforming/beamsteering capabilities. An integrated optical phased array (OPA) is a photonic integrated circuit (PIC) that can form and steer laser beams across a 3-D target space. Integrated OPAs offer significant advantages in SWaP and reliability as compared to conventional solutions, because they leverage existing silicon photonics technologies based on mature semiconductor infrastructures. Specifically, silicon photonics offers low-loss high performance waveguide devices for two main components of an OPA: diffractive grating emitters and phase shifters (thermo- or eletro-optic). Silicon, however, presents some challenges in high-power, large-scale OPA devices. First, silicon waveguides have relatively low optical power handling capability due to the large optical loss at high power caused by its nonlinearity (e.g., two-photon absorption). Secondly, silicon photonic devices are typically built on the top silicon layer of a silicon-on-insulator (SOI) chip. This single photonic layer severely limits routing waveguides that connect the array of emitters to the phase shifters in 2-D OPA designs. In this paper, we propose a new design for high-power, large-scale OPAs by heterogeneous integration of SOI, SiN, and III-V photonics.

II. HETEROGENEOUS INTEGRATED OPA SPARSE ARRAY

In this new OPA design, as shown in Fig. 2-ab, a SiN photonic chip is used as a *passive* interposer. Optical waveguides are constructed with one or potentially multiple SiN layers on the interposer to route optical signals. SiN waveguides have much higher optical power handling capability than the silicon ones at NIR, and are well suited for the power distribution

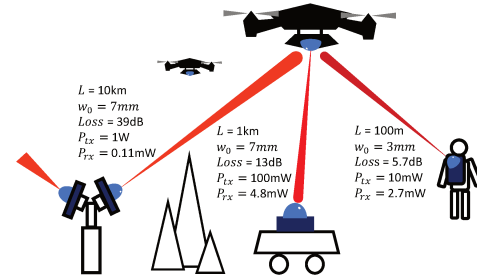


Fig. 1. OPA devices for FSO communication in a conceptual UAV application: the base station and mobile units in the ad-hoc network are wirelessly connected through the UVA hub. The link performance is illustrated at several distances and at the NIR wavelength of 1550 nm.

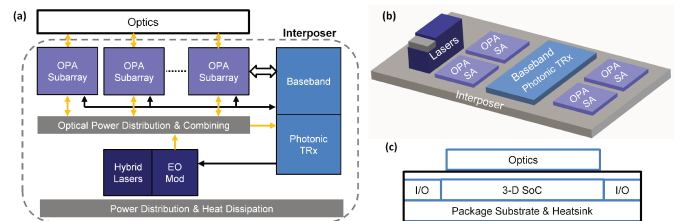


Fig. 2. Architecture of the proposed heterogeneous integrated OPA: (a) System diagram; (b) interposer and chiplets; (c) conceptual structure of the OPA device module.

network in a large-scale, high-power OPA. Multiple SOI silicon photonic *chiplets*, each of which serves as a subarray in the OPA, are 3-D integrated on the interposer. Silicon is more suitable for compact grating emitters due to its better light confinement. Thermo-optic phase shifters are implemented on the SiN interposer, as well as thermo- or electro-optic ones on the SOI chiplets. A hybrid laser can be heterogeneously integrated on the SiN interposer. The laser is externally modulated to carry RF signals for FSO communication. The 3-D chip is housed in a PIC package with FSO components (e.g. front lenses) mounted on top, as shown in Fig. 2-c.

An OPA design with subarrays reduces the chip area for phase shifters [1]. It simplifies waveguide routing in the subarray aperture which now has a fraction of the total number of emitters. The 3-D integration approach also significantly reduces the overall system cost by shrinking the chip size of the SOI chiplets, which are typically fabricated in a

more costly *active* silicon photonic process than the passive SiN interposer. Further, 3-D integration improves waveguide routing due to the additional waveguide layer(s) in the SiN interposer. When the SiN photonic layers are incorporated in future CMOS technologies, an *active* interposer can house the CMOS electronics for OPA controls, data converters, microcontrollers, and digital signal processing (DSP) circuitry. Such a system-on-chip (SoC) will greatly improve the OPA system performance while reducing its SWaP.

Because of the required spacing between the chiplets, however, the OPA subarrays are spaced further apart than in a monolithic integration design. Side lobes resulted from the relatively large subarray pitch size degrade the OPA's angular resolution. We propose to utilize the sparse array techniques to suppress the side lobes by spreading the their power [2]. The sparse array design is also necessary to accommodate variabilities in the precise placement of chiplets during 3-D integration.

III. DESIGN AND SIMULATION RESULTS

To evaluate the performance of the proposed OPA architecture, we characterize the components and overall OPA using photonic device and phased array simulations. We choose the wavelength of 1550 nm in the following designs. The SOI chiplets are implemented in a standard silicon photonics technology with a 220-nm top silicon layer and 2- μ m BOX layer, in which strip waveguides are 450-nm wide.

Fig. 3-ab show the layout of a 2-D OPA subarray with 4x4 emitters and that of a grating emitter. The latter's compact size is tailored for the OPA application, and results in a wide beamwidth (FWHM=31°(Az)/22°(EL)), as shown in the simulated beam profile (Fig. 3-c), which enables a large beam-steering range for the OPA. The grating's emission efficiency is 46.5%.

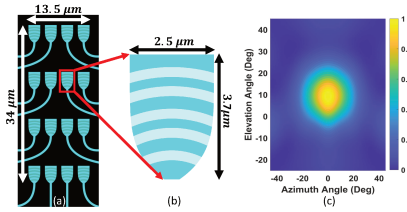


Fig. 3. Layout of (a) the OPA subarray with 4x4 grating emitters and (b) the grating emitter; (c) the beam profile of a single emitter.

In the following analyses, we use the same grating emitter and subarray designs, and construct the OPA as a sparse array with 1xN subarrays. The focus is on the azimuth direction characteristics, and the results can be extended easily to the elevation direction by adopting the same designs in the OPA's longitudinal direction to create sparse arrays with MxN subarrays.

Fig. 4 illustrates the sparse-array OPA's beamforming performance. With increasing number of subarrays, the main lobe is compressed, its peak intensity increases, and side lobes are created due to aliasing.

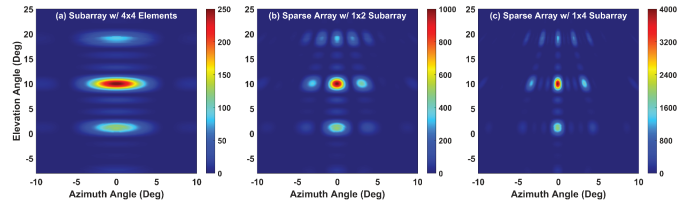


Fig. 4. Beam profiles of (a) the 4x4 subarray on each SOI chiplet, and the sparse arrays with (b) 1x2 and (c) 1x4 subarrays.

As shown in Fig. 5, by optimizing the location of the subarrays in the sparse array, the OPA's side lobes are spread in the spatial spectrum and hence suppressed with increasing number of subarrays.

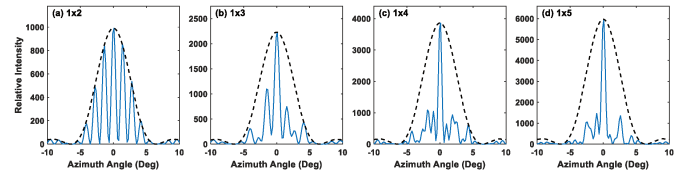


Fig. 5. Azimuth beam profiles of several 1xN sparse array designs based on the 4x4 subarray in Fig. 4-b. The subarray's beam profile is shown as the envelope.

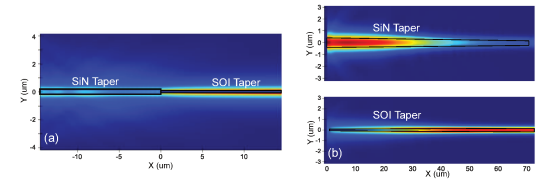


Fig. 6. SiN-to-Si waveguide coupler designs simulated in FDTD: (a) Edge-to-edge coupling; (b) Vertically-overlapped tapers. E-field is shown in colors.

The critical component of SiN-to-Si waveguide coupling is designed and simulated to characterize the additional optical loss due to heterogeneous integration. Using FDTD simulations, we model two coupling designs: (a) Coupling between two chip-edge couplers; (b) Vertical coupling between two inverse tapered waveguides [4]; as shown in Fig. 6-ab, respectively. Both designs show negligible optical loss (0.5 and 0.02 dB).

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REFERENCES

- [1] P. Rocca, G. Oliveri, R. J. Mailloux, and A. Massa, "Unconventional Phased Array Architectures and Design Methodologies—A Review," *Proceedings of the IEEE*, vol. 104, no. 3, pp. 544-560, 2016.
- [2] F. Smith, W. Wang, and H. Wu, "Sparse Optical Phased Array Design," in *IEEE 16th International Conference on Group IV Photonics*, 2019.
- [3] F. Smith and H. Wu, "Photonic Phased Array Design by Synthesis," in *IEEE 15th International Conference on Group IV Photonics*, 2018.
- [4] W. D. Sacher et al, "Monolithically integrated multilayer silicon nitride-on-silicon waveguide platforms for 3-D photonic circuits and devices," *Proceedings of the IEEE*, vol. 106, no. 12, pp. 2232-2245, 2018.