Package Degradation's Impact on SiC MOSFETs Loss: A Comparison of Kelvin and Non-Kelvin Designs

Fei Yang
High Voltage Power Business Unit
Texas Instruments
Dallas, TX, 75243, USA
fei.yang@ti.com

Shi Pu, Bilal Akin
Department of Electrical and Computer Engineering
The University of Texas at Dallas
Richardson, TX, 75080, USA

Stephanie W. Butler, Gangyao Wang
High Voltage Power Business Unit
Texas Instruments
Dallas, TX, 75243, USA

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***Abstract*—Aging-related electrical parameter shifts in SiC MOSFETs can adversely affect the power converter performance. In this paper, the package degradation's effect on the device's switching loss is comprehensively investigated. Both the TO-packaged 3-pin and 4-pin devices are evaluated, and the device's on-resistances and switching losses are compared before and after the package degradation. From the experimental results, it is observed that the wire bond degradation can significantly affect the switching loss of the 3-pin devices: more than 23.8% / 27% turn-on/off loss increase is observed, and it becomes more noticeable at higher current and faster switching conditions. The increased package resistance and electrical coupling to the gate loop contribute to the loss variation. In contrast, the switching loss in the 4-pin Kelvin connected SiC MOSFET is not affected by package degradation as the Kelvin-source connection helps to decouple the package degradation's impact on gate drive circuits. The findings serve as a guideline for SiC MOSFETs based converter designs to ensure robust operation and avoid potential thermal instability issues in the long-term operation.**

Keywords—SiC MOSFETs; switching loss; package degradation; reliability

I. INTRODUCTION

Silicon Carbide (SiC) MOSFETs are desirable for high-efficiency and high-power-density power electronics converters in various industrial applications due to the low on-resistance and junction capacitance [1]–[3]. However, its long-term reliability has been a concern in mission-critical applications, and the device's performance can be affected by different aging mechanisms.

Previously, both gate oxide and package degradations have been observed in SiC MOSFETs [4]–[9]. Specifically, a high density of traps still exists in the SiC-SiO_2 interface even with the state-of-art manufacturing process. These interface or near interface traps can cause threshold voltage instability after long-term operations [4]–[6].

On the other hand, the package of the SiC MOSFETs also degrades due to the thermal-mechanical stress among the device and packaging materials with different coefficients of thermal expansion (CTE). As a result, the wire bond liftoff/crack and the solder joint void have been observed in discrete packaged devices [7] while additional baseplate solder crack has been reported in some power module packages [8].

From the application's point of view, it is essential to understand these degradations' impact on the SiC MOSFET's performance such that certain design margins can be considered in the initial converter design stage.

In the literature, various aspects of aging's impact on SiC MOSFET performance have been investigated. It is reported that the gate oxide degradation induced threshold voltage shift can cause on-resistance variations [10]–[15] and potentially lead to increased conduction loss after long-time operation [16]. Moreover, the switching transient of the SiC MOSFETs can also be affected [15]–[20]. Regarding package degradation, the wire bond liftoff/crack can, not only causes the on-resistance increase but also contributes to a significant switching loss increase [16].

However, the previous studies only focus on the 3-pin TO-packaged SiC MOSFETs where the gate loop and power loop are coupled by the common source connection. For the emerging 4-pin TO-package devices or power modules with Kelvin source connection, the package degradation's impact on the device performance remains unknown. Therefore, this paper considers both the Kelvin and non-Kelvin connected packages and comprehensively evaluates the wire bond degradation's impact on SiC MOSFETs' performance.

The paper is constructed as follows: the test procedure is first introduced in Section I to mimic a wire bond degradation in commercial 3-pin and 4-pin TO packaged SiC MOSFETs. The static parameter shifts and the transfer characteristic's variation are explored in Section II. Afterward, the package degradation's impact on the device's switching loss is investigated, and the test results on Kelvin and non-Kelvin packaged SiC MOSFETs are discussed. Section IV summarizes the results and provides a design guideline to consider SiC MOSFET's performance degradation in different packages.

II. TEST PROCEDURE AND SETUP

To have a complete understanding of package degradation's impact on the device performance, both the TO-247 3-pin and TO-247 4-pin packaged SiC MOSFETs are used in the experiments. In the 3-pin TO-package, the gate drive loop and power loop shares the same source connection as shown in Fig. 1, and it represents a non-Kelvin connection.

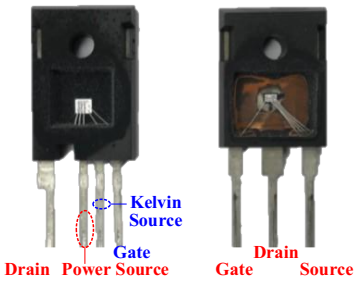


Fig. 1. Package bonding scheme for 3-pin and 4-pin TO Packages.

TABLE I. DEVICE INFORMATION.

Voltage/Current	1200 V/ 30 A	1200 V/ 30 A
$R_{ds,on}$ at 25°C	70 mΩ (20 A)	70 mΩ (20 A)
Package	TO-247-3 Pin	TO-247-4 Pin
Total # of Power Source Wire Bonds	3 thick wires	3 thick wires
Gate Drive Voltages	15 V/ -4 V	15 V/ -4 V

This package is inherited from the traditional Si power MOSFETs or IGBTs. However, due to the common-source inductance in the non-Kelvin TO-247 3-pin package, the SiC MOSFET's switching speed cannot be fully exploited [21] and spurious voltage spikes can be generated during the switching transients raising concerns about the device's robustness [22]. The 4-pin TO package or power module package provides an additional source pin and can minimize or eliminate the common-source inductance by decoupling the gate loop from the power loop. As a result, the device performance is optimized, and the package with Kelvin source for gate drive is becoming commercially available from different SiC MOSFETs manufacturers.

In this study, package degradation's impact on devices with different packages is considered. To have a fair comparison between the Kelvin and non-Kelvin packages, the devices with the same die are chosen in the test, and the device information is summarized in Table I.

Normally, power cycling or thermal cycling is implemented to degrade the device's package [23]–[25]. However, the test takes a long time, and additional gate oxide degradation is introduced in the power cycling test due to the gate voltage stress at elevated junction temperature [6]. To expedite the test and target solely at the package degradation, the wire bond on the power source is cut to mimic a wire bond lift-off after thermal-mechanical stress. Specifically, a new device is partially de-capsulated on the source wire bond areas as shown in Fig. 2, and the wire bonds can be cut manually. The partial decapsulation allows the device to still operate at high voltage switching conditions and the device's switching characteristics before and after cutting the wire bonds.

Before and after each wire bond modification, the static parameters and switching characteristics of the device are characterized. Fig. 3 shows the test procedure: the device's static characteristics are obtained from the Keysight B1506A curve tracer while the switching loss data is measured in a double-pulse test (DPT) setup.

Fig. 2. New device with de-capsulation on the sourece-pin area.

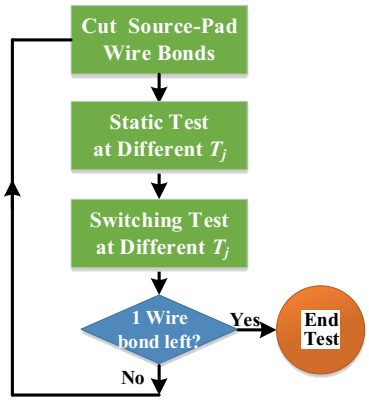


Fig. 3. New device with de-capsulation on the sourece-pin area.

III. STATIC PARAMETER SHIFT COMPARISON WITH DIFFERENT PACKAGES

For both TO-247 3-pin and TO-247 4-pin devices summarized in Table I, there are three thick wire bonds on the power source as shown in Fig. 2. After cutting the source pad wire bonds, the static characteristics are compared in this section.

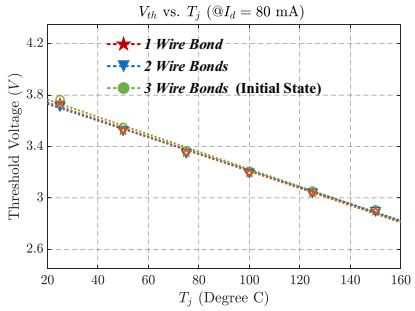
A. Threshold Voltage Change

The threshold voltage shifts are first shown in Fig. 4. In the test, the threshold voltage is defined as the gate to source voltage when the drain current reaches 80 mA. Since there is no long-time gate bias stress applied to the device, the threshold voltage shifts are negligible in both the Kelvin and non-Kelvin devices. It can be seen that the package modification is not affecting the device's characteristics.

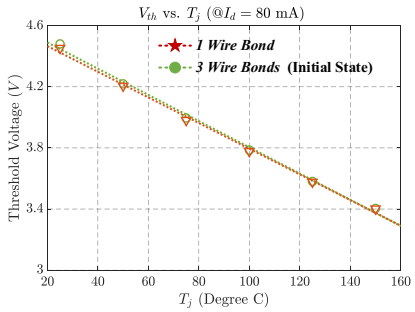
B. Package Degradation's Effect on Reverse Voltage Drop

The package degradation's effect on the reverse characteristics is also investigated. Initially, the reverse voltage at low current (100 mA) and negative gate-to-source voltage bias (-4 V) is considered as indicated in Fig. 5. The negative V_{gs} ensures that all the current will go through the body diode of the SiC MOSFETs. At low current, the variation of reverse voltage drop due to the package modification is small and can be hardly differentiated from the experimental measurements.

However, when the reverse current is increased to a higher value (3 A), the reverse conduction voltage V_{SD} start to increase as the number of source-pad wire bonds decreases, and the change is consistent across a junction temperature

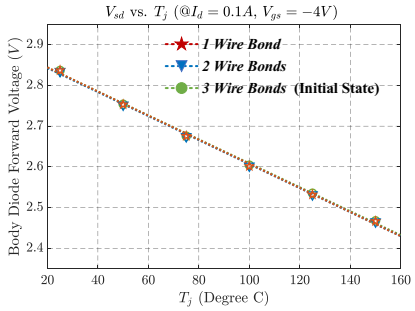


(a) Non-Kelvin device with TO-247 3-pin package

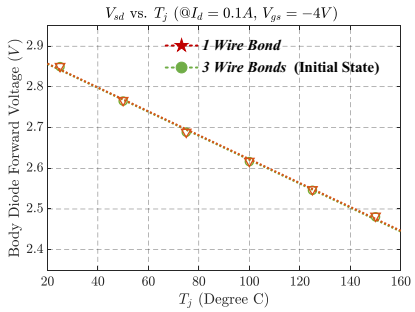


(b) Kelvin device with TO-247 4-pin package

Fig. 4. Threshold voltage change of devices after package modifications.



(a) Non-Kelvin device with TO-247 3-pin package



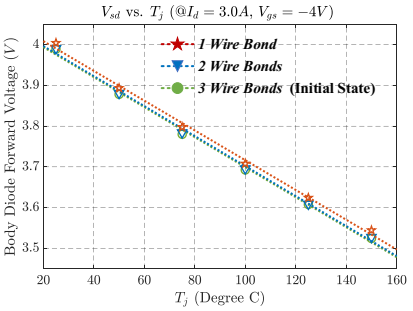
(b) Kelvin device with TO-247 4-pin package

Fig. 5. Reverse voltage change (low current) after package modifications.

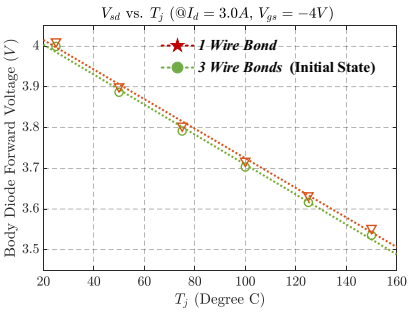
range from 25 ℃ to 150℃ as shown in Fig. 6.

C. *Aging's Effect on On-Resistance*

Similarly, the package degradation can also affect the the on-state resistance, and Fig. 7 illustrates the on-resistance

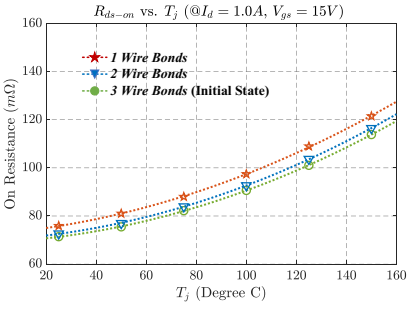


(a) Non-Kelvin device with TO-247 3-pin package

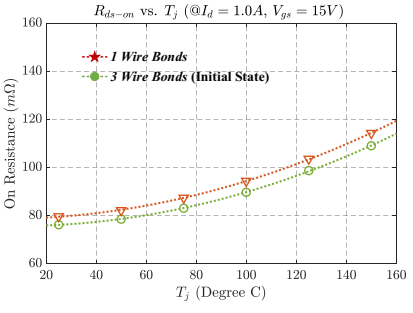


(b) Kelvin device with TO-247 4-pin package

Fig. 6. Reverse voltage change (high current) after package modifications.



(a) Non-Kelvin device with TO-247 3-pin package

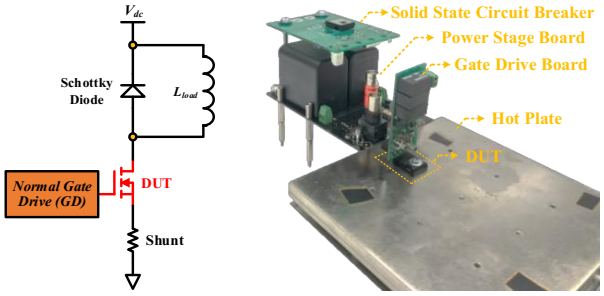


(b) Kelvin device with TO-247 4-pin package

Fig. 7. On-resistance change of devices after package modifications.

$R_{ds,on}$ variations over package modifications at different T_j. The device's on-resistance composes of the channel resistance R_{ch}, drift region resistance R_d, substrate resistance R_{sub} and package resistance $R_{package}$ as expressed in (1):

$$R_{ds,on} \approx R_{ch} + R_d + R_{sub} + R_{package} \quad (1)$$



(a) Circuit diagram (b) Setup

Fig. 8. Double pulse test circuit diagram and setup.

As can be seen, due to the wire bond cut-off, the overall on-resistance of both devices goes up. Specifically, at 150 °C, the on-resistance of the TO-247 3-pin device increases from 113.9 mΩ to 121.8 mΩ, while the $R_{ds,on}$ of TO-247 4-pin device elevated from 109 mΩ to 114.5 mΩ. Up to 6.9% on-resistance is observed by cutting the source-pad wirebond. In real applications, the on-resistance increase can be more significant (e.g. 20% towards the end of a lifetime) considering together the solder crack and wire bond crack. The increased package resistance can cause excessive conduction loss and end up with more electrical stress on the remaining wire bond.

IV. Comparison of Switching Loss Variation with Different Packages

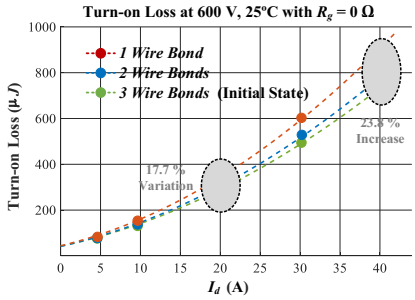
The switching loss of the same device is obtained from the double-pulse test, and the package degradation's impacts on devices with Kelvin and non-Kelvin connections are compared in this section.

The circuit diagram of the double-pulse test setup shown is in Fig. 8 (a), and the experimental setup is illustrated in Fig. 8 (b). The low-side SiC MOSFET is the device under test, and a SiC Schottky diode is used on the high-side. The isolated gate driver UCC5390SC from Texas Instruments is used, and it has a 10 A sink/source capability. The hot plate is placed beneath the device such that its junction temperature can be adjusted through the hot plate's temperature setting. Note that to achieve an accurate junction temperature setting in the device, the thermal resistance in between the device and hot plate is also considered, and the body diode's voltage drop at low current and negative bias is used to calibrate the device's T_j and hot plate's temperature setting [15]. From the DPT setup, the device's switching loss can be characterized at different junction temperatures.

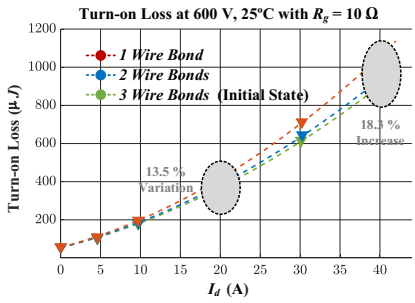
A. Turn-on Loss Change Over Aging

1) Turn-on Loss Variation in Non-Kelvin Packaged Device:

Fig. 9 illustrates the room temperature turn-on loss variation of non-Kelvin connected TO-247 3-pin device after the modifications. The test results at different turn-on gate resistances are presented. As can be seen, when the source-pad wire bonds start to degrade, the turn-on switching loss



(a) External turn-on gate resistance of 0 Ω



(b) External turn-on gate resistance of 10 Ω

Fig. 9. Turn-on loss shift in 3-pin devices due to package modification.

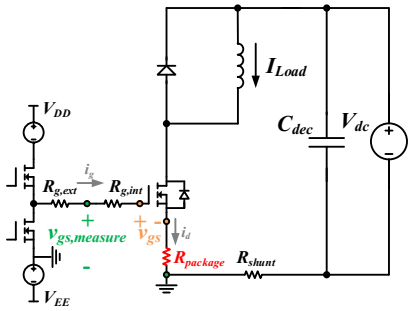


Fig. 10. Turn-on circuit diagram considering package resistance degradation in a TO-247 3-pin non-Kelvin connection package.

increases significantly for both the 0 Ω and 10 Ω external gate resistance cases. At 600V and 20 A condition, the 6.9% package resistance change in the source wire bond can introduce more than 17.7% and 13.5% turn-on switching loss's increase for $R_{g,ext}$ = 0 Ω and $R_{g,ext}$ = 10 Ω respectively. Also, it is observed that the turn-on loss increment becomes more significant at higher load conditions. At 40 A and 0 Ω external gate resistance, more than 23.8% additional switching loss is observed. The increased turn-on switching loss can affect the device's performance and system efficiency in the long run. In the worst case, thermal run-away can be induced due to the excessive switching loss. Therefore, it has to be taken into consideration in the initial converter design stage, and a 20% or higher thermal margin is recommended based on the testing results.

As discussed in [16], the increased source-pad package resistance contributes to the additional turn-on switching loss. Specifically, Fig. 10 illustrates the circuit diagram of the DPT

circuit considering the package resistance in the TO-247 3-pin non-Kelvin package. During the turn-on current rise period, the gate voltage of the device v_{gs} increases from the threshold voltage to the miller plateau voltage V_{miller} following an RC time constant formed by the total gate loop resistance and the device's input gate capacitance C_{iss}:

$$V_{gs} = V_{DD} \cdot (1 - e^{-\frac{t}{(R_{g,int}+R_{g,ext}+R_{pacakge})\cdot C_{iss}}}) \quad (2)$$

The gate loop resistance consists of the internal gate resistance $R_{g,int}$, the external gate resistor $R_{g,ext}$, and the package resistance in the source pad $R_{package}$. As the package resistance goes up after cutting the source-pad wire bonds, the RC time constant is increased thus increasing the turn-on loss during the current rise period. Meanwhile, since the package resistance is shared by the gate loop and power loop, an additional voltage drop is introduced across the package resistance $R_{package}$ when the device's drain current i_d starts to commutate the load current during the current rise period. As a result, the equivalent gate drive voltage of the device is reduced. Combining with the increased RC time constant, the real gate-to-source voltage of the device increases more slowly after the package degradation, and an elevation of turn-on switching loss is expected during the current rise period.

During the turn-on voltage falling or *dv/dt* period, the gate current i_g is discharging the miller capacitance and can be described as:

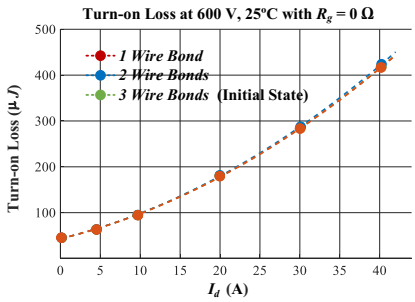
$$i_g = \frac{V_{DD} - V_{th} - \frac{I_L}{g_m} - i_d \cdot R_{package}}{R_{g,int}+R_{g,ext}+R_{package}} \quad (3)$$

V_{DD} is the positive gate drive voltage, and V_{th} is the threshold voltage of the SiC MOSFETs. In the denominator, the package resistance reduces the gate current. At the same time, the additional voltage drop term $i_d \cdot R_{package}$ in the numerator makes the gate current smaller. Consequently, the voltage falling period is extended, and the turn-on loss tends to increase as the source-pad package degrades. The loss increase also varies with the load conditions, and a larger loss increase is expected at a higher load current according to (3).

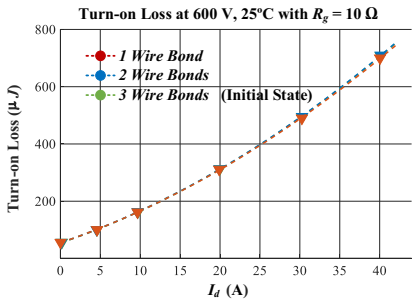
2) Turn-on Loss Variation in Kelvin Packaged Device:

The same test procedure is applied to the TO-247 4-pin device with a Kelvin source connection, and its turn-on switching loss variation after cutting the power source wire bonds is summarized in Fig. 11. As can be seen, different from the 3-pin non-Kelvin connected device, the turn-on switching loss remains the same and it is not affected by the wire bond degradation in the power source. The main reason is: with the Kelvin-source connection, the gate drive loop is decoupled from the power loop, and the gate drive capability remains the same regardless of the power source wire bond modifications.

Meanwhile, with minimized common-source inductance between gate loop and power loop, the turn-on switching loss of the Klevin connected 4-pin device is much smaller than the non-Kelvin connected 3-pin device under the same gate driver and operating conditions.



(a) External turn-on gate resistance of 0 Ω



(b) External turn-on gate resistance of 10 Ω

Fig. 11. Turn-on loss shift in 4-pin devices due to package modification.

From the comparison with non-Kelvin connected 3-pin SiC MOSFETs, it can be observed that the Kelvin connected SiC MOSFETs not only have lower switching losses but also provides a more consistent turn-on switching loss without being affected by the package degradation. Therefore, from the application's point of view, the device with Kelvin connect is more robust in long-term operation and requires less thermal margin in the converter design stage.

B. Turn-off Loss Change Over Aging

The turn-off loss variation over package degradation is also compared in between the 3-pin and 4-pin packaged devices, and the results are summarized in Fig. 12 and Fig. 13.

Similar to the turn-on switching loss variation case, the SiC MOSFETs with a non-Kelvin connection show a turn-off loss increase. At 600 V, 40 A with an external gate resistance of 0 Ω, the turn-off loss in TO-247 3-pin packaged device can increase from 178 μJ to 226 μJ, and more than 27% loss increase is observed. On the contrary, the devices with Kelvin connection demonstrate a consistent turn-off loss, which is independent of the power source package degradations. The package resistance, which is shared in between the gate drive loop and power loop in the 3-pin package case, is contributing to the difference in turn-off loss variation.

V. CONCLUSIONS

This paper experimentally evaluates the package degradation' impact on the performance of SiC MOSFETs. A partial decapsulation is implemented to the device, and the

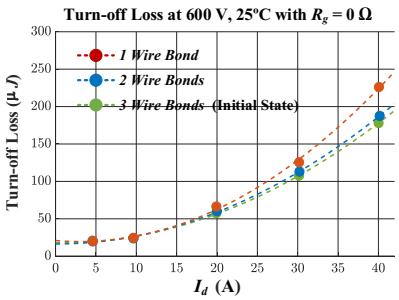
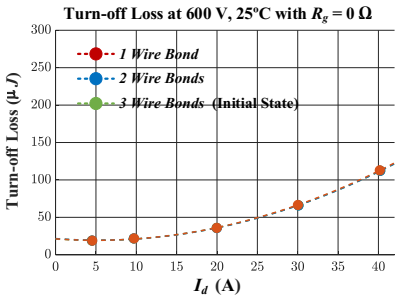


Fig. 12. Turn-off loss shift in 3-pin devices due to package modification.



(b) External turn-on gate resistance of 10 Ω

Fig. 13. Turn-off loss shift in 4-pin devices due to package modification.

source-pad wire bonds are cut to mimic a wire bond degradation. In the evaluation, both the non-Kelvin package (TO-247 3-pin) and the Kelvin package (TO-247 4-pin) are considered, and the variations of static and switching characteristics at different package degradation conditions are compared. The key findings of this paper are:

- In term of static characteristics, cutting the source-pad wire bonds have the same impact on 3-pin and 4-pin devices: the on-resistance is increased and the reserse conduction voltage goes up especially at the high current region.
- Regarding wire bond degradations' impact on switching characteristics, differen behaviors are observed for the non-Kelvin and Kelvin packaged SiC MOSFETs. For the TO-247 3-pin package with non-Kelvin connection, the gate loop is coupled to the power loop, and both turn-on and turn-off switching loss increase as the package resistance goes up. The loss increase is more significant at faster switching speed (lower external gate resistance) and larger load current conditions. More than 23% and 27% loss increase are observed for turn-on and turn-off process respectively. However, on the TO-247 4-pin devices with Kelvin connection, no switching loss variation is observed.
- From long-term reliability's point of view, the Kelvin connection is preferred for SiC MOSFETs as its switching loss is consistent and independ of the wire bond degradation status.

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REFERENCES

[1] F. Wang and Z. Zhang, "Overview of silicon carbide technology: Device, converter, system, and application," *CPSS Trans. Power Electron. Appl.*, vol. 1, no. 1, pp. 13–32, 2016.

[2] X. Ding *et al.*, "Analytical and Experimental Evaluation of SiC-inverter Nonlinearities for Traction Drives Used in Eletric Vehicles," *IEEE Trans. Veh. Technol.*, vol. 67, no. 1, pp. 146–159, 2018.

[3] Y. Cui *et al.*, "High efficiency data center power supply using wide band gap power devices," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2014, pp. 3437–3442.

[4] T. Aichinger, G. Rescher, and G. Pobegen, "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs," *Microelectron. Reliab.*, vol. 80, pp. 68–78, 2018.

[5] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic Mechanisms of Threshold-Voltage Instability and Implications for Reliability Testing of SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 316–323, 2015.

[6] E. Ugur, F. Yang, S. Pu, S. Zhao, and B. Akin, "Degradation Assessment and Precursor Identification for SiC MOSFETs under High Temp Cycling," *IEEE Trans. Ind. Appl.*, vol. 55, no. 3, pp. 2858–2867, 2019.

[7] S. Dusmez, S. H. Ali, M. Heydarzadeh, A. S. Kamath, H. Duran, and B. Akin, "Aging Precursor Identification and Lifetime Estimation for Thermally Aged Discrete Package Silicon Power Switches," *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 251–260, 2017.

[8] N. Heuck, R. Bayerer, S. Krasel, F. Otto, R. Speckels, and K. Guth, "Lifetime analysis of power modules with new packaging technologies," in *Proc. Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, 2015, pp. 321–324.

[9] Z. Ni, X. Lyu, O. P. Yadav, B. N. Singh, S. Zheng, and D. Cao, "Overview of Real-Time Lifetime Prediction and Extension for SiC Power Converters," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7765–7794, 2020.

[10] H. Luo, F. Iannuzzo, and M. Turnaturi, "Role of Threshold Voltage Shift in Highly Accelerated Power Cycling Tests for SiC MOSFET Modules," *IEEE J. Emerg. Sel. Top. Power Electron.*, p. 1, 2019.

[11] U. Karki and F. Z. Peng, "Effect of Gate-Oxide Degradation on Electrical Parameters of Power MOSFETs," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10764–10773, 2018.

[12] K. Puschkarsky, H. Reisinger, T. Aichinger, W. Gustin, and T. Grasser, "Understanding BTI in SiC MOSFETs and Its Impact on Circuit Operation," *IEEE Trans. Device Mater. Reliab.*, vol. 18, no. 2, pp. 144–153, 2018.

[13] S. Pu, F. Yang, B. T. Vankayalapati, E. Ugur, C. Xu, and B. Akin, "A Practical On-Board SiC MOSFET Condition Monitoring Technique for Aging Detection," *IEEE Trans. Ind. Appl.*, vol. 56, no. 3, pp. 2828–2839, May 2020.

[14] E. Ugur, C. Xu, F. Yang, S. Pu, and B. Akin, "A New Complete Condition Monitoring Method for SiC Power MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1654–1664, 2021.

[15] F. Yang, E. Ugur, and B. Akin, "Evaluation of Aging's Effect on Temperature Sensitive Electrical Parameters in SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6315–6331, 2020.

[16] F. Yang, E. Ugur, S. Pu, B. Akin, and M. Das, "Investigation of Aging's Effect on the Conduction and Switching Loss in SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, 2019, pp. 6166–6173.

[17] S. Pu, E. Ugur, F. Yang, and B. Akin, "In situ Degradation Monitoring of SiC MOSFET Based on Switching Transient Measurement," *IEEE Trans. Ind. Electron.*, vol. 67, no. 6, pp. 5092–5100, 2020.

[18] Z. Ni, Y. Li, X. Lyu, O. P. Yadav, and D. Cao, "Miller plateau as an indicator of SiC MOSFET gate oxide degradation," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2018, pp. 1280–1287.

[19] S. Pu, E. Ugur, F. Yang, C. Xu, and B. Akin, "Thermally Triggered SiC MOSFET Aging Effect on Conducted EMI," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, 2018, pp. 51–55.

[20] F. Yang, S. Pu, C. Xu, and B. Akin, "Turn-on Delay Based Real-Time Junction Temperature Measurement for SiC MOSFETs With Aging Compensation," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1280–1294, 2021.

[21] Z. Chen, D. Boroyevich, and R. Burgos, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," in *Proc. Int. Conf. Power Electron., ECCE Asia (ICPE-ECCE Asia)*, 2010, pp. 164–169.

[22] W. Zhang, Z. Zhang, F. Wang, D. Costinett, L. Tolbert, and B. Blalock, "Common source inductance introduced self-turn-on in MOSFET turn-off transient," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2017, pp. 837–842.

[23] F. Yang, E. Ugur, and B. Akin, "Design Methodology of DC Power Cycling Test Setup for SiC MOSFETs," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 4, pp. 4144–4159, 2020.

[24] B. T. Vankayalapati, F. Yang, S. Pu, M. Farhadi, and B. Akin, "A Highly Scalable, Modular Test Bench Architecture for Large-Scale DC Power Cycling of SiC MOSFETs: Towards Data Enabled Reliability," *IEEE Power Electron. Mag.*, vol. 8, no. 1, pp. 39–48, 2021.

[25] L. R. GopiReddy, L. M. Tolbert, and B. Ozpineci, "Power Cycle Testing of Power Switches: A Literature Survey," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2465–2473, 2015.