MeF-RAM: A New Non-Volatile Cache Memory Based on Magneto-Electric FET

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Magneto-Electric FET (**MEFET**) is a recently developed post-CMOS FET, which offers intriguing characteristics for high-speed and low-power design in both logic and memory applications. In this article, we present *MeF-RAM*, a non-volatile cache memory design based on **2-Transistor-1-MEFET** (**2T1M**) memory bit-cell with separate read and write paths. We show that with proper co-design across MEFET device, memory cell circuit, and array architecture, MeF-RAM is a promising candidate for fast **non-volatile memory** (**NVM**). To evaluate its cache performance in the memory system, we, for the first time, build a device-to-architecture cross-layer evaluation framework to quantitatively analyze and benchmark the MeF-RAM design with other memory technologies, including both volatile memory (i.e., SRAM, eDRAM) and other popular non-volatile emerging memory (i.e., ReRAM, STT-MRAM, and SOT-MRAM). The experiment results for the PARSEC benchmark suite indicate that, as an L2 cache memory, MeF-RAM reduces **Energy Area Latency** (**EAT**) product on average by ~98% and ~70% compared with typical 6T-SRAM and 2T1R SOT-MRAM counterparts, respectively.

CCS Concepts: • **Hardware → Spintronics and magnetic technologies;**

Additional Key Words and Phrases: Magneto-electric FETs, non-volatile memory, memory bit-cell, cache design

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1 INTRODUCTION

Over the past decade, **Non-Volatile Memories** (**NVM**) have been actively explored with the main goals of satisfying robustness, minimizing standby leakage, achieving high speed, and integration density as major requirements to replace conventional fast volatile memory technologies in main memory (i.e., DRAM) or cache (i.e., SRAM) [13, 16, 17, 31]. Robust NVM could, optimistically, boost memory capacity and performance, especially when it comes to the on-chip cache for embedded applications and low-power IoT systems. However, there are very few NVM technologies still surviving in this arena. Among the popular NVM technologies, ReRAM [2] and PCM [29] offer higher ON/OFF ratio, thus higher sense margin, and packing density than DRAM (∼2–4×) [29]. However, they suffer from slow and power-hungry write operations as well as low endurance ($\sim 10^5$–10^{10}) [14, 16]. The **ferroelectric transistor random access memories** (**FERAMs**) [13] offer high endurance and sense margin but suffer from a destructive read operation. FE-FET memories [23, 45], however, offer FERAMs' benefits with a reduced 1–10 ns [23] write time and could be a possible alternative. The downside is their large write voltage (>4.0 V) and power consumption [34, 43, 44]. Recent experiments and fabrication of spin-based NVMs show the ability to switch the magnetization using current-induced **Spin-Transfer Torque** (STT) or Spin-Orbit Torque (SOT) with high-speed (sub-nanosecond), long retention time (10 years), and less than fJ/bit memory write energy (close to SRAM) [7, 8, 19, 46]. However, such NVMs have poor ON/OFF ratios (typically much less than 10). Moreover, the current densities in current-driven spin devices impose reliability issues and large power dissipation [5, 6, 19].

Recently, another promising spintronic device, based on the antiferromagnetic **Magneto-Electric** (**ME**) phenomena [16, 17, 48, 51], has shown superior performance in terms of switching speed, energy, ON/OFF ratio, and so on. The principal innovative feature of this emerging device that significantly differs from the traditional spintronic devices is that its switching speed is much faster and only limited by the switching dynamics of antiferromagnetic ME material of the voltage-controlled spintronic devices [17, 35, 39]. With coherent rotation, as the domain switching mechanism, the switching speed might be as fast as <20 ps [39] as it doesn't require the switching of a ferromagnet or movement of a ferromagnetic domain wall. Therefore, this may be considered to be spintronics without a ferromagnet, achieving fast write speeds (<20 ps) [35, 39, 50], a low energy cost (<20 aJ) [50], combined with great temperature stability (operational to 400 K or more), and improved scalability.

While there are proposals for logic design based on ME devices, such as ME-MTJ [50, 52] and MEFET [17, 35, 37, 51], as well as NVM design based on ME-MTJ [30, 36, 49], there is no detailed analysis and benchmarking works to investigate both the benefits and limitations of MEFET-based NVM design. In this article, we present *MeF-RAM*, a non-volatile cache memory design based on **2-Transistor-1-MEFET** (**2T1M**) memory bit-cell with separate read and write paths. We show that with proper co-design across MEFET device, memory cell circuit, and array architecture, MeF-RAM is a promising competitor for current non-volatile on-chip cache memory. Our main contributions in this work are summarized as follows:

- We discuss a MEFET Verilog-A circuit model based on our prior four-terminal MEFET device structure to enable further analysis and benchmarking at the MeF-RAM memory cell circuit and array architecture levels.
- We present a 2T1M memory bit-cell circuit design with separated write/read paths, high speed, and low read/write energy suitable for on-chip cache memory.
- We develop a bottom-up (device-to-architecture) evaluation framework to extensively assess and benchmark MeF-RAM cache performance with current both volatile and NVMs, including SRAM, eDRAM, ReRAM, STT-MRAM, and SOT-MRAM.

2 MAGNETO-ELECTRIC SPIN FIELD EFFECT TRANSISTOR

2.1 Device Characterization

The **Magneto-Electric spin Field Effect Transistor** (**MEFET**) is structurally very similar to the conventional CMOS FET device. Figure 1(a) shows the basic single source version of MEFET as a four-terminal device with gate (at T1), source (T2), drain (T3), and back gate (T4) terminals [12, 17]. The device is a stacked structure of a narrow semiconductor channel sandwiched by two dielectrics, i.e., ME material (e.g., Chromia (Cr_2O_3)) and insulator (e.g., Alumina (Al_2O_3)). There are two electrodes contacting the stacked structure, at the bottom gate via ME layer (T1) and at the top via the back gate alumina layer. The channel as shown in Figure 1(b) is made of tungsten diselenide (WSe_2), enabling an on-off ratio of up to $\sim 10^4$–10^6 [12, 17] and high hole mobility comparable to CMOS. The source (at T2 terminal) could be made of both a fixed spin **ferromagnetic** (**FM**) polarizer or a conductor. MEFET operates based on the programming of the semiconductor channel polarization, so-called **Spin-Orbit Coupling** (**SOC**), by the boundary polarization of the ME gate, through the proximity effect. In other words, the channel can be polarized by the ME layer on extremely low voltage of around ±100 mV [17, 48, 51] at T1 while T4 is grounded.

The ME layer has high boundary layer polarization which can be controlled by vertical voltage [17]. Chromia here is a promising ME gate dielectric that has the potential to induce spin polarization in an over-layer channel [17]. Applying a voltage across the gate and back gate terminal is equivalent to the charging of the ME capacitor. Therefore, depending on the positive or negative voltage applied to T1, a vertical electrical field across the gate is created. In response to the electrical field, paraelectric polarization and **Anti-Ferromagnetic** (**AFM**) order in the ME insulator layer are switched. It first changes the direction of orientation of chromia spin vectors through SOC. The ME boundary polarization can have an exchange interaction with a semiconductor channel to polarize the carriers' spins in the channel and induce preferred conduction, i.e., much lower resistance, in only one direction along the channel. This high spin boundary polarization was predicted independently by Andreev [4] and Belashchenko [11] and has been experimentally confirmed, for ME chromia, by a wide variety of techniques [17]. In other words, the influence of surface magnetization on the channel induces a directionality in the conductance, which is not possible through conventional gate dielectrics, as depicted in Figure 1(d). Therefore, in the end, the channel spin vector changes to either the "up" or "down" direction. The current versus voltage dependent on the direction of ME polarization is obtained by NEGF transport simulation [3, 17] in a 2D ribbon with a width of 20 nm and band mass of $0.1m_e$. We consider here a conservative value of exchange splitting of 0.1 eV, T3-T2 = 0.1 V, at 300 K. As shown in Figure 1(e), chromia induces a very high level of spin polarization in the WSe_2 channel, virtually 100% at the top of the valence band for hole conduction. Such an induced polarization interaction with chromia is shown in Figure 1(f). After biasing the SOC channel, the charge current is injected through the source generating a spin-polarized current at the T3. Figure 1(b) and (c) show the 2D view of the MEFET device and its transistor circuit representation used in this work. As T4 is grounded, the simplified three-terminal scheme is used hereafter.

Compared to a >200 ps coupling delay of the **Magneto-Electric Magnetic Tunnel Junction** (**ME-MTJ**) [50], MEFET achieves an extremely low switching delay (somewhere in the region of 10–00 ps [33], by avoiding the excessive delays associated with exchange-coupled ferromagnets. Such device shows the feature of non-volatility due to the non-volatile AFM ordering of ME, and a very high and sharp turn-on voltage due to the sharp turn-on of ME-switching [47]. It is worth pointing out that for sensing of device resistance, a more energy-efficient read circuitry could be expected for MEFET as it shows a much higher ON/OFF ratio compared with **Tunneling Magneto-Resistance** (**TMR**) sensing in traditional spin-based devices. The ON/OFF current ratio

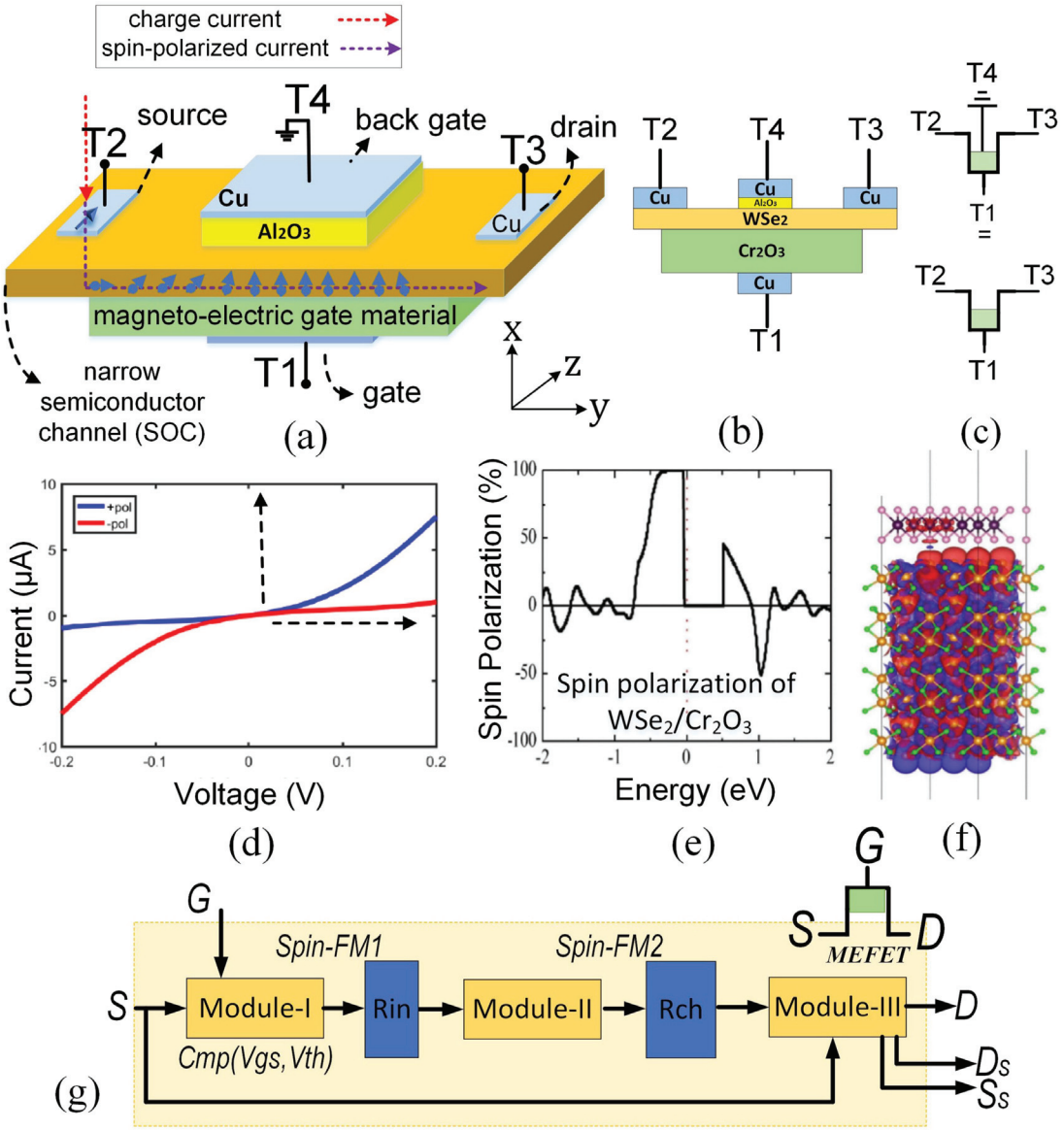

Fig. 1. (a) The basic Magneto-Electric spin-FET (MEFET) with gate, source, drain, and back gate. The narrow semiconductor channel can be made of any suitable material (e.g., graphene, InP, GaSb, PbS, WSe_2). (b) A 2D view of MEFET. (c) The proposed MEFET circuit scheme. (d) Sample Source to drain current vs. voltage at T1 in the MEFET. The SOC channel polarized in opposite directions (+ or −) by the ME gate. (e) Induced spin polarization in WSe_2. (f) Interaction with chromia adapted from [17]. (g) Verilog-A modules developed for MEFET modeling.

for WSe_2 [18] is experimentally shown to extend up to 10^6, while the TMR effect in MTJs typically is smaller than 10. Regarding MEFET fabrication, MEFET does not need an external magnetic field to operate. The deterministic toggling of states in prototypical ME antiferromagnet Cr_2O_3 is experimentally demonstrated without an applied magnetic field at CMOS compatible temperatures between 300 and 400 K [32]. However, there exist many experiments proving that with a magnetic field, the chromia's magnetic order could be switched back and forth via applying an electric field [28, 55].

The main challenges for MEFET fabrication and integration center around the following: (1) making the ground plane contact reliable, so the growth of chromia has few imperfections

Table 1. Compact Model Parameters of the MEFET, Used in the Verilog-A Model Adapted from [47, 50]

Parameter	Value	Description of Parameter and Units
ϵ_{ME}	12	Dielectric constant of chromia [27]
$\epsilon_{Al_2O_3}$	10	Dielectric constant of Alumina
t_{ME}	10	Thickness of magneto electric layer, nm
$W_{ME} \times L_{ME}$	900	Area of magneto-electric layer, nm^2
t_{ox}	2	Oxide barrier thickness, nm
V_t	0.05	Threshold of chromia state inversion, V
V_g	0.1	Voltage applied across ME layer, V
R_{on}	1.05	ON Resistance, $k\Omega$
R_{off}	63.4	OFF Resistance, $M\Omega$

so that it is a good gate dielectric (i.e., the goal is insignificant leakage currents); (2) adding more boron to see if the critical temperature can be raised even higher than 400 K, so that the blocking temperature is raised much higher than 360 K; and (3) getting a good 2D semiconductor onto chromia, with large SOC, so the transistor widths can be reduced to less than 10 nm without edge scattering, but the ON/OFF ratio can be increased to 10,000 or more.

2.2 Device Modeling

In this work, we consider two aspects in developing the MEFET device/circuit model: First, ME control of the channel spin polarization based on the proximity-induced polarization in the narrow 2D channel. Second, spin injection/detection function at the source/drain [47, 51]. The model is developed in Verilog-A with three distinct modules as shown in Figure 1(g). In the presented MEFET model, T2 and T3 are utilized to inject the spin-polarized current and detect it, respectively.

In the Verilog-A model shown in Figure 1(g), we consider the experimental switching parameters for chromia layer and SOC channel. Module-I receives the gate-source voltage, and compares it with the threshold of chromia state inversion voltage (Vth = 0.050 V [51]), initializes the memory, and assigns back to the voltage across the drain and source terminal. Module-II considers the delay factor in the transition from source to drain. We consider here that a computed delay element is associated with the boundary magnetization between the ME film and the interface of the channel. The switching time of the MEFET device is then limited by the switching dynamics of ME. Module-III assigns the proper channel resistance (R_{ch}) and calculates corresponding electrical parameters output voltage at the drain. R_{ch} across the two-dimensional (2D) narrow channel is considered in series to the input resistance R_{in} to define the boundary conditions for switching. Besides, we consider two spin-state terminals ("Ss" and "Ds") to validate the spin state injected/detected at the source/drain terminals as shown in Figure 1(g). The "up" and "down" spins are represented by constant voltage sources with "+1 V" and "−1 V," respectively, at the "Ss" terminal. Before running the simulation, the injected spin orientation can be selected, making the model flexible to be used in various CAD tools such as the Cadence platform. The spin current then can be detected at the drain ("Ds" in Figure 1(g)). In our compact model, the processional delay across the FM layer was taken into account by a fixed delay assumed to be 200 ps. This assumption is based on the best estimate of the coupling delay [35]. Table 1 lists the parameter values used in our Verilog-A model. Please note that the I-V curve and Ron-Roff ratio shown in Figure 1(d) is scaled up and benchmarked with the reported number in Table 1.

3 MEF-RAM MEMORY

The presented non-volatile 2T-1MEFET RAM bit-cell, called MeF-RAM, consists of one MEFET as the main storage element and two access transistors, as shown in Figure 2(a). By virtue of the

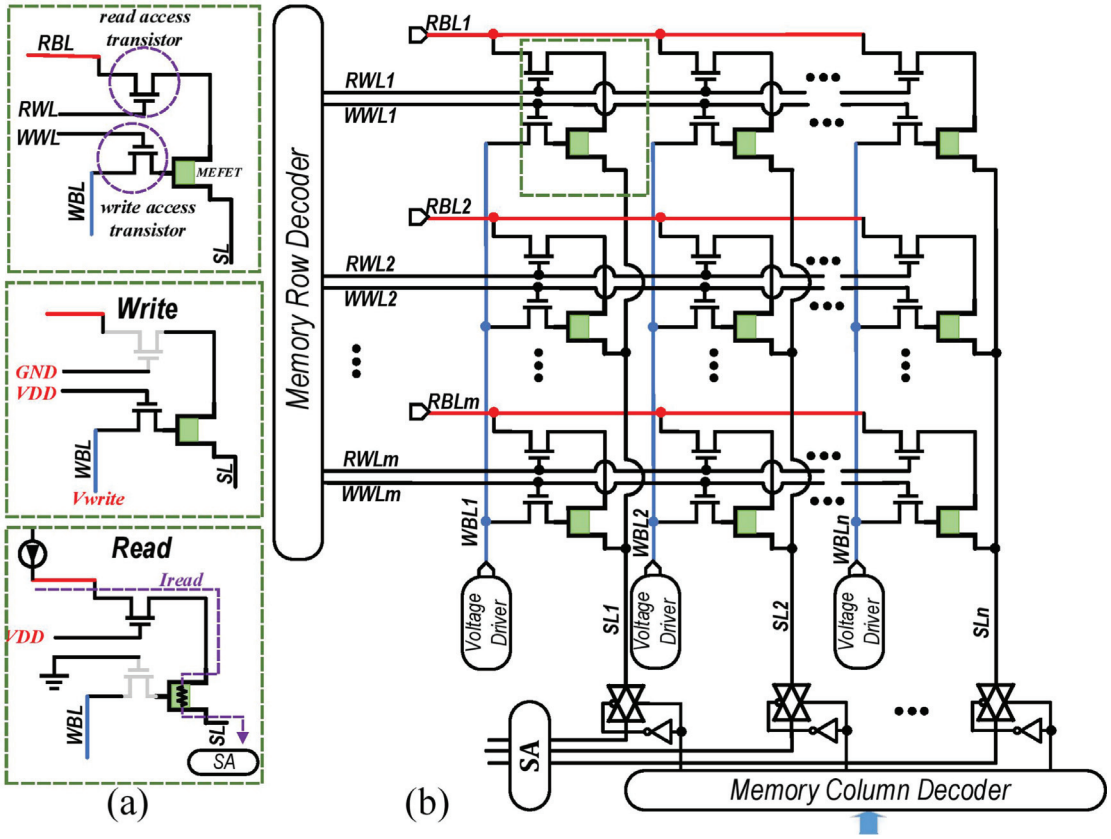

Fig. 2. (a) The 2T-1MEFET RAM (MeF-RAM) bit-cell with Read and Write signals. (b) An m × n MeF-RAM array with peripheral circuitry.

three-terminal structure of MEFET, depicted in Figure 1(c), we design the memory bit-cell to have separate read and write paths which facilitates independent optimization of both operations, as well as avoiding common read-write conflicts in many 1T1R resistive NVM designs. Each cell is controlled by five controlling signals, i.e., **Write Word Line** (**WWL**), **Write Bit Line** (**WBL**), **Read Word Line** (**RWL**), **Read Bit Line** (**RBL**), and **Source Line** (**SL**). The read/write access transistor is controlled by RWL/WWL enabling selective read/write operation on the cells located within one row. An m × n MeF-RAM array developed based on the 2T1M bit-cell is shown in Figure 2(b). The WLs and RBLs are shared among cells within the same row and WBLs, while SLs are shared between cells in the same column. The WLs are controlled by the memory row decoder (active–high output). The column decoder (active–high output) controls the activation of the read current path through the SL. The voltage driver component is designed to set the proper voltage on the WBL. In the following, we will explain the detailed read and write operations, respectively.

3.1 Read Operation

The concept behind MeF-RAM's read operation is to sense the resistance of the selected memory cell and compare it by a reference resistor using a **Sense Amplifier** (**SA**), as shown in Figure 2(a). At the array level, shown in Figure 3(a), the row and column decoders activate the RWL and SL paths, respectively. When a memory cell is selected, by applying a very small sense current (sub-micro) to RBL, a voltage (V_{sense}) is generated on the corresponding SL, which is taken as the input of the sense circuit, as shown in Figure 3(b). Owing to the low or high resistance state of the selected 2T-1MEFET RAM bit-cell (R_{M1}), the sense voltage is V_{low} or V_{high} ($V_{low} < V_{high}$),

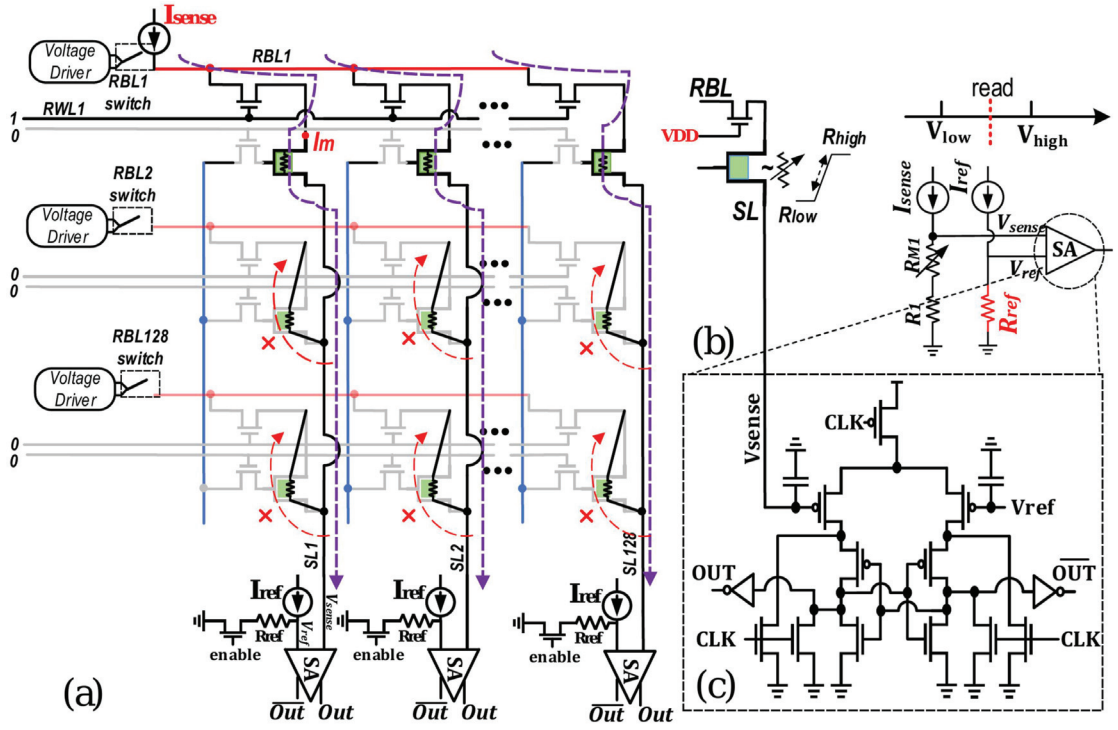

Fig. 3. (a) The array-level read operation. It can be seen that read access transistors isolate the un-accessed cells avoiding sneak paths. (b) The idea of voltage comparison between V_{sense} and V_{ref} for memory read. (c) The Sense Amplifier (SA).

respectively. Thus, through setting the reference voltage at $(V_{low} + V_{high})/2$, the SA outputs binary "1" when $V_{sense} > V_{ref}$, whereas output is "0." We designed and tuned the sense circuit based on StrongARM latch [42] shown in Figure 3(c). Each read operation requires two clock phases: pre-charge (CLK "high") and sensing (CLK "low"). During the pre-charge phase, both SA's outputs are reset to ground potential. Then, in the sensing phase, the input transistors provide various charging currents based on the gate biasing voltages (V_{sense} and V_{ref}), leading to various switching speeds for the latch's cross-coupled inverters. The biasing condition for the read operation is tabulated in Table 2. It is noteworthy that there is no tangible scalability issue in MEFET arrays compared with other resistive crossbars as the ON/OFF current ratio for WSe_2 is experimentally shown to extend up to 10^6. Accordingly, the read margin is higher than certain RRAM crossbars with ON/OFF ratio typically around 10^2. However, several RRAM technologies show a high ON/OFF ratio close to 10^5 ratio, where the IR drop effect will be insignificant. We simulated and measured IR drop on various size memory array, i.e., 16×16, 32×32, 64×64, 128×128, 256×256, and observed a negligible voltage drop.

3.2 Write Operation

The write operation, shown in Figure 2(a), is accomplished by activating WWL and asserting appropriate bipolar write voltage ($V_{write}/-V_{write}$) through a voltage driver on WBL. As detailed above, the voltage provides enough vertical electrical field magnitude across the gate to switch the spin vectors of the underlying chromia layer and channel of MEFET. The RBL and SL don't require to be grounded for the write period as seen in other memory technologies such as FEFET [44]. The unaccessed rows are isolated by driving the corresponding WLs to GND by a row decoder. This is necessary to avoid unwanted current paths that can cause false write/read states. The biasing condition for the write operation is tabulated in Table 2.

Table 2. Bias Configuration of MeF-RAM Array

	Operation	WWL	RWL	WBL	RBL	SL
Accessed	Read	0	1	-	I_{sense}	-
Unaccessed		0	0	-	-	-
Accessed	Write	1	0	$-V_{write}/-V_{write}$	-	-
Unaccessed	("1"/"0")	0	0	-	-	-
All	Hold	0	0	-	-	-

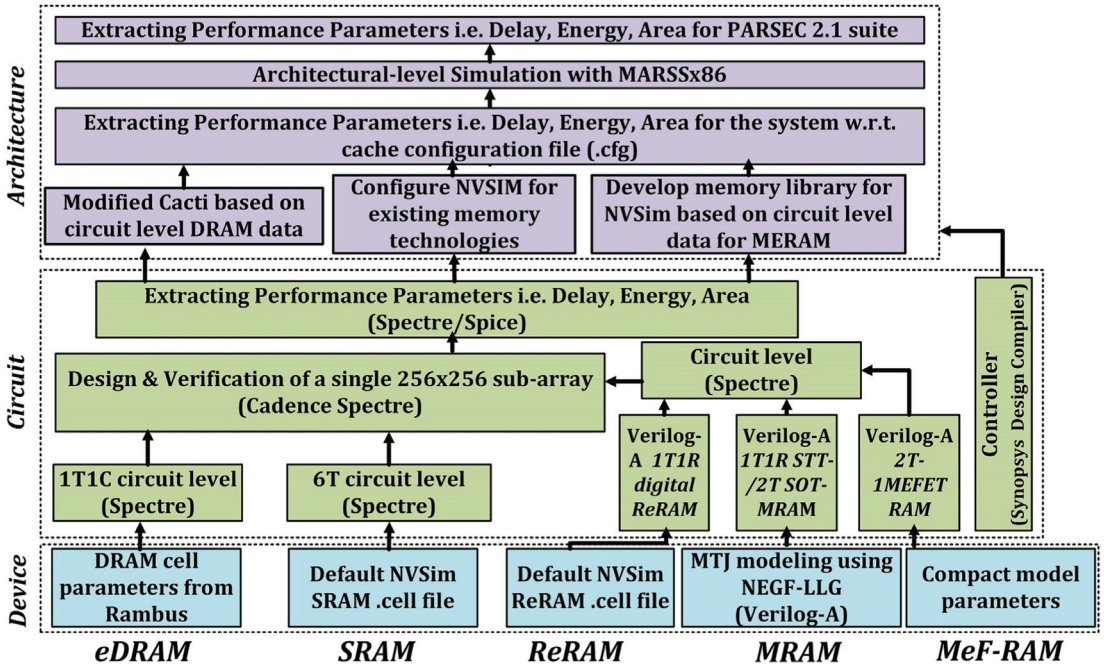

Fig. 4. The bottom-up evaluation framework developed for cache memory evaluation.

4 EVALUATION

4.1 Bottom-Up Evaluation Framework

We developed a comprehensive bottom-up cross-layer framework for cross-technology evaluation and comparison, as shown in Figure 4. The device-level model of each technology was first developed/extracted from various models and assessments. For MeF-RAM, we used the Verilog-A model developed in preliminary work [51]. For STT-MRAM and SOT-MRAM, we jointly use the **Non-Equilibrium Green's Function** (**NEGF**) and **Landau-Lifshitz-Gilbert** (**LLG**) equations to model the bit-cell, developed in preliminary work [9, 10, 20]. We leveraged the default ReRAM (HfO_2) and SRAM cell configuration of NVSim [15]. The eDRAM cell parameters were adopted and scaled from Rambus [26]. The array-level evaluation on FEFET for cache memory was inevitability skipped in this work since we were not able to access the experimentally benchmarked device-level models of this emerging memory technology. At the circuit level, we developed a 256×256 memory sub-array for each memory technology with peripheral circuitry, simulated in Cadence Spectre with the 45-nm NCSU **Product Development Kit** (**PDK**) library [1].

For architecture level, a PIM support evaluation tool is developed for the NVSIM [15] named PIMA-SIM[1] as shown in Figure 5 to model the timing, energy, and area of various PIM

[1]The initial version of PIMA-SIM is available at https://github.com/ASU-ESIC-FAN-Lab/PIMA-SIM.

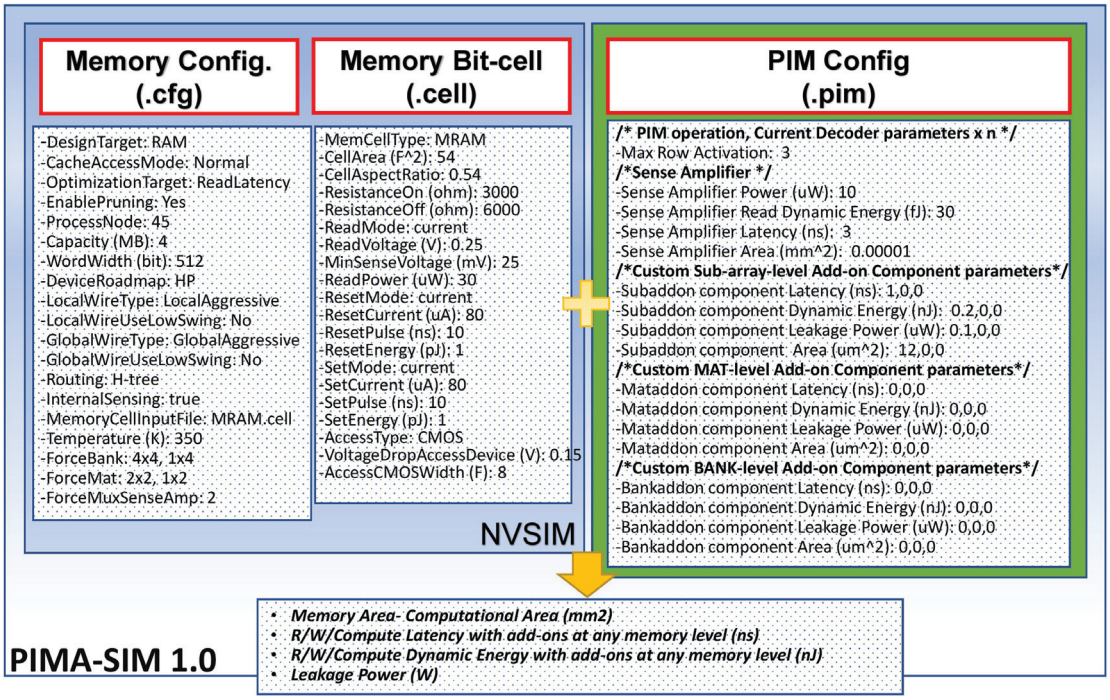

Fig. 5. PIMA-SIM as a PIM support evaluation tool developed to model the timing, energy, and area of various PIM technologies. The data reported in the figure is just for example.

technologies. This tool offers the same flexibility in memory configuration regarding bank/mat/subarray organization and peripheral circuitry design as NVSIM while supporting PIM-level configurations. PIMA-SIM can be configured using three configuration files. At the cell level, it uses NVSIM's .cell file to save the device–circuit-level info. At the architecture level, it uses NVSIM's .cfg file to configure the memory organization and optimization target. In addition, as depicted in Figure 5, at the PIM level, PIMA-SIM's .pim file is designed to save the PIM-level parameters. PIMA-SIM's .pim file gives the following flexibilities to study the PIM behaviors: (1) users can specify the number of row activation for PIM purposes; (2) users can insert their customized sense amplifier designs; and (3) users can add any number of customized add-ons at the sub-array/mat/bank-level. The PIM libraries are accordingly developed for each platform on top of NVSIM [15] and Cacti [54] based on device/circuit-level data. Accordingly, the performance data (i.e., latency, energy, and area) could be extracted for different PIM platforms w.r.t. a single input memory configuration file (.cfg). The results are then fed to the cycle-accurate MARSS × 86 simulator [40] for each memory technology to show the architecture-level performance.

4.2 Device and Circuit Level

Figure 6 shows the transient simulation results of a 2T-1MEFET RAM cell located in a 256 × 256 sub-array based on the architecture shown in Figure 2(b). Here, we consider two experiment scenarios for the write operation, as indicated by the solid blue and the dotted red line in Figure 6. For the sake of clarity of waveforms, we assume a 3 ns period clock synchronizes the write and read operation. However, <1 ns period can be used for a reliable read operation. During the pre-charge phase of SA (Clk = 1), the V_{write} voltage is set (= −100 mV in the first experiment or +100 mV in the second experiment) and applied to the WBL to change the MEFET resistance to R_{low} = 1.05 $k\Omega$ or R_{high} = 63.4 $M\Omega$. Before the evaluation phase (Eval.) of SA, WWL and WBL are grounded while RBL is fed by the very small sense current, I_{sense} = 900 nA. In the evaluation phase, RWL goes high

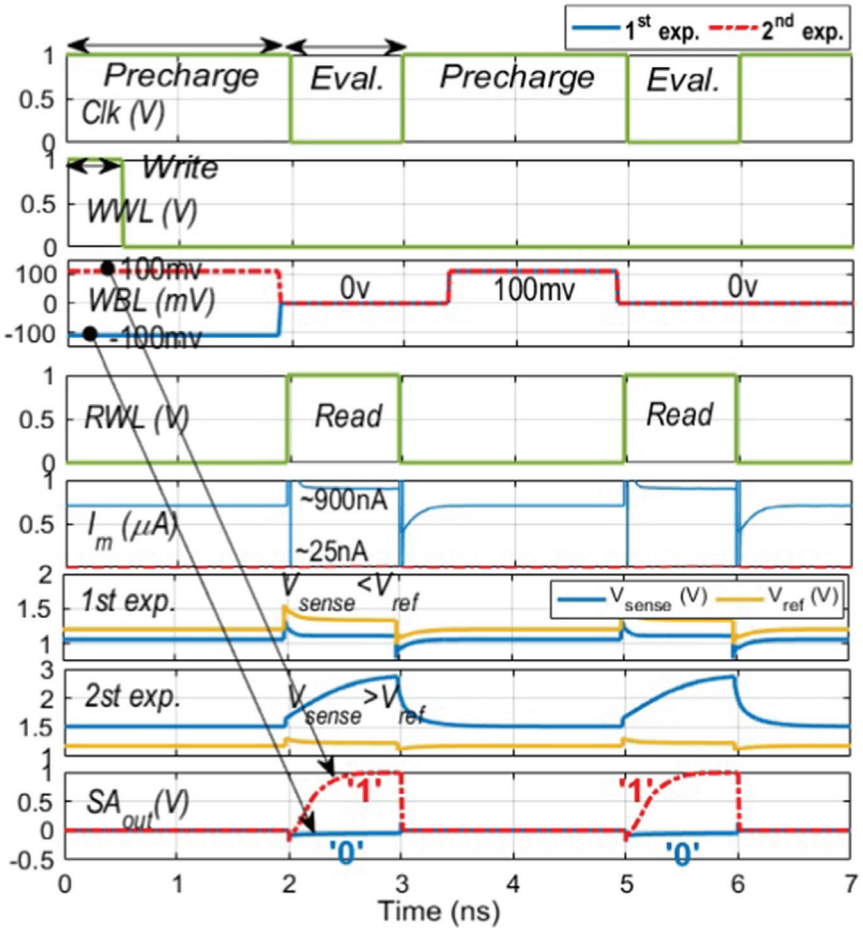

Fig. 6. The transient simulation results of two experiments on MeF-RAM cell.

and depending on the resistance state of MeF-RAM bit-cell and accordingly SL, V_{sense} is generated at the first input of SA, when V_{ref} is generated at the second input of SA. The comparison between V_{sense} and V_{ref} for both experiments is plotted in Figure 6. We observe when $V_{sense} < V_{ref}$ (first experiment), the SA generates the binary output "0," whereas the output is "1" (second experiment). As can be seen, the same value can be sensed again in the next sensing cycle (3–6 ns) regardless of WBL voltage since WWL is deactivated, so the MeF-RAM bit-cell remains unchanged.

Table 3 compares the row performance of six various memory technologies, i.e., volatile SRAM and eDRAM with non-volatile ReRAM, STT-MRAM, SOT-MRAM, and MeF-RAM integrated as a 4 MB L2 cache with 64 Bytes cache line size. It is worth pointing out that the data is extracted from our bottom-up evaluation framework and architecture-level simulators. Here, we discuss the results reported in Table 3. Additionally, the radar plot in Figure 7 further investigates and intuitively shows the pros and cons associated with each technology compared with MeF-RAM in the array level that could be employed to build high-density arrays.

4.2.1 Latency. As listed in Table 3, we observe that MeF-RAM shows a remarkable improvement in a cache hit and miss latency (0.65/0.22 ns) compared with other platforms. In terms of cache write, MeF-RAM achieves the second shortest latency after volatile SRAM. It can achieve a 0.94 ns cache write operation, which is ~4× shorter than the best NVM (SOT-MRAM-3.93 ns) but not faster than the SRAM counterpart (0.78 ns). This comes from the fact that MeF-RAM's switching speed is only limited by the switching dynamics of antiferromagnetic ME material of the

Table 3. Estimated Row Performance of Various Memory Technologies as a 4 MB Unified L2 Cache with 64 Bytes Cache Line Size

Metrics	ReRAM (HfO_2)	ReRAM (Ag-Si)	STT-MRAM	SOT-MRAM	SRAM	eDRAM	MeF-RAM
Non-volatility	Yes	Yes	Yes	Yes	No	No	Yes
# of access transistors	1	1	1	2	6	1	2
Area (mm^2)	1.77	1.95	5.42	5.85	12.4	4.46	6.94
Cache Hit Latency (ns)	2.55	2.89	3.14	5.07	1.59	3.1	0.65
Cache Miss Latency (ns)	1.21	1.48	1.28	1.32	0.34	-	0.22
Cache Write Latency (ns)	20.5	28.1	10.7	3.93	0.78	3.1	0.94
Cache Hit Dynamic Energy (nJ)	0.33	0.43	0.52	0.21	0.73	0.24	0.22
Cache Miss Dynamic Energy (nJ)	0.033	0.051	0.044	0.03	0.017	-	0.037
Cache Write Dynamic Energy (nJ)	0.82	1.07	1.27	0.27	0.72	0.24	0.27
Cache Total Leakage Power (W)	0.38	0.52	0.79	0.21	6.2	0.57	0.19
Endurance	$\sim 10^5$–10^{10}	$\sim 10^5$–10^{10}	$\sim 10^{10}$–10^{15}	$\sim 10^{10}$–10^{15}	Unlimited	$\sim 10^{15}$	$\sim 10^{17}$
Data Over-written Issue	No	No	No	No	No	Yes	No

voltage-controlled spintronic devices [17, 35, 39]. With coherent rotation, as the domain switching mechanism, the switching speed might even be much faster [39] as it doesn't require the switching of a ferromagnet or movement of a ferromagnetic domain wall. Therefore, MeF-RAM meets the requirements of a high-speed non-volatile cache unit.

4.2.2 Energy Consumption. The energy budget for various cache operations is shown in Table 3. The proposed MeF-RAM design achieves a comparable dynamic energy consumption for a cache hit to eDRAM and SOT-MRAM as the most energy-efficient designs. While SRAM, SOT-MRAM, and ReRAM achieve the least energy consumption for cache miss. Moreover, we observe SOT-MRAM, and MeF-RAM platforms consume the smallest cache write dynamic energy among all the NVM platforms due to their intrinsically low-power device operation. However, eDRAM shows the least energy consumption. MeF-RAM consumes 0.27 nJ for the write operation, which is ~2.6× smaller than the SRAM platform. MeF-RAM writing technique averts dissipative currents and is thus energy-efficient, and inerts against detrimental impacts of Joule heating [17]. The cache total leakage power is also reported in Table 3. We observe that MeF-RAM and SOT-MRAM consume the least leakage power compared to other candidates. Thus, MeF-RAM could be considered as a promising non-volatile unit in terms of energy-efficiency.

4.2.3 Endurance. The inorganic MEFET easily lasts to 10^{17} switches [51]. The reason here is the required current densities are very low, which considerably reduces the device failure rate from what has been seen in other spintronic devices, which require much higher current densities (10^{10}–10^{15}) [21].

4.2.4 Area. The MeF-RAM bit-cell requires two minimum-sized access transistors (W:L = 90:50 at 45 nm technology node) to enable separate read and write paths. Since the write current to switch between space is very small, such a reduced-sized access transistor could be readily leveraged to design an MeF-RAM bit-cell, while state-of-the-art spintronic devices typically require ~1.5–3×-width access transistors. In this way, MeF-RAM occupies 6.94 mm^2 to implement a 4 MB cache, which turns out to be a larger chip area than other NVMs and eDRAM. However, it achieves ~1.7× smaller area than the 6T SRAM platform. Therefore, the MeF-RAM array couldn't be considered an area-efficient NVM candidate compared to ReRAM and STT-MRAM.

4.2.5 Integration with CMOS. The device characteristics of chromia layer make this material interesting for integrating into the **back end of the line** (**BEoL**). The feasibility of integration of chromia with silicon was experimentally demonstrated in [38, 41]. The bit-cell layout of single-port MeF-RAM, shown in Figure 8(b), was estimated using λ-based layout rules (λ: half of the minimum feature size, F, here λ:22.5 nm) [24]. The proposed cell takes an estimated $40\lambda \times 16\lambda = 640\lambda^2$, in

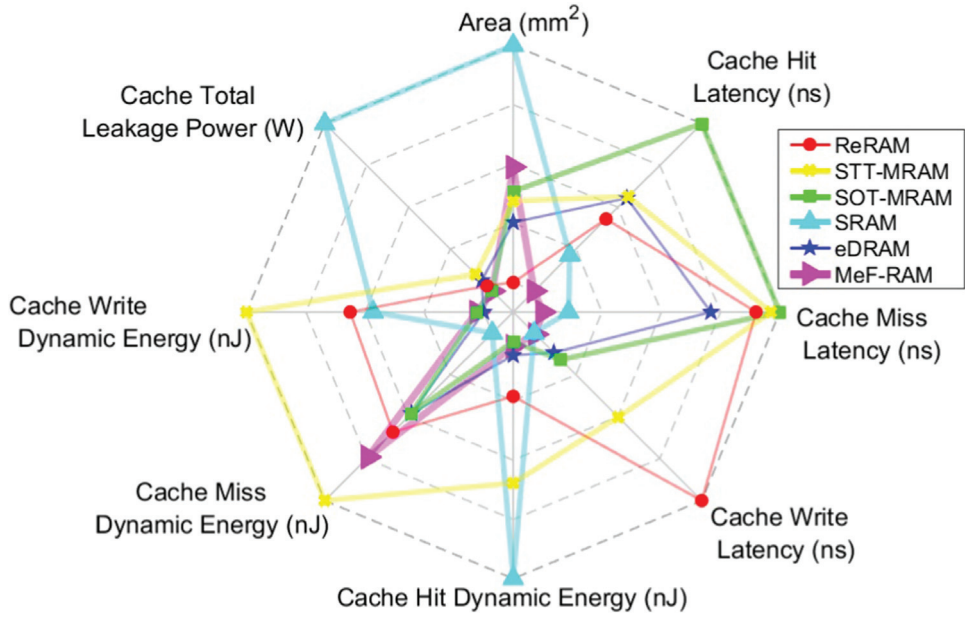

Fig. 7. Benchmarking radar plot of MeF-RAM vs. other technologies.

Table 4. System Configuration

CPU	4 cores, 3.3 GHz, Fetch/Exec/Commit width 4
L1	private, 32 KB, I/D separate, 8-way, 64 B, SRAM, WB
L2	private, 4 MB, unifed, 8-way, 64 B, memory tech. candidate, WB
Main Memory	8 GB, 1 channel, 4 ranks/channel, 8 bank/rank

contrast to $2000\lambda^2$ of layout of baseline 6T-SRAM adapted from [25]. The layout of the 4×4 MeF-RAM array with controlling signals is illustrated in Figure 8(a).

4.2.6 MeF-RAM vs. ReRAM. To explore the impact of chosen material in ReRAM when compared with MeF-RAM, two ReRAM implementations are considered in Table 3, i.e., the NVSIM's default .cell that belongs to HfO_2-based MOS-accessed ReRAM prototype in [53] and the Ag-Si memristor device parameters in [22]. We observe that HfO_2 shows a shorter cache hit/miss/write latency than the Ag-Si implementation. Moreover, the HfO_2 could be selected as the more energy-efficient design compared with the Ag-Si implementation. Overall, MeF-RAM outperforms both designs w.r.t. various metrics as tabulated in Table 3.

4.3 Architecture Level

4.3.1 Experiment Setup. The cycle-accurate simulator MARSS $\times$ 86 [40] was used to evaluate the efficiency of our proposed circuit-to-architecture cross-layer framework. The cache controller was modified to realize the functionality of L2 architecture with various memory technology candidates. We configured the simulator with the parameters listed in Table 4. We selected 11 various benchmarks from the PARSEC 2.1 suite for testing the performance of MeF-RAM compared to the existing cache technologies. The cache in the simulator warmed up with 5 million instructions. The 500 million instructions starting at the **Region Of Interest** (**ROI**) of each workload was executed afterward. The collected reports were used to analyze the L2 cache candidates based on **Energy Area Latency** (**EAT**) product. The EAT metric can holistically identify the preferred L2 candidate by considering several essential metrics in the cache design.

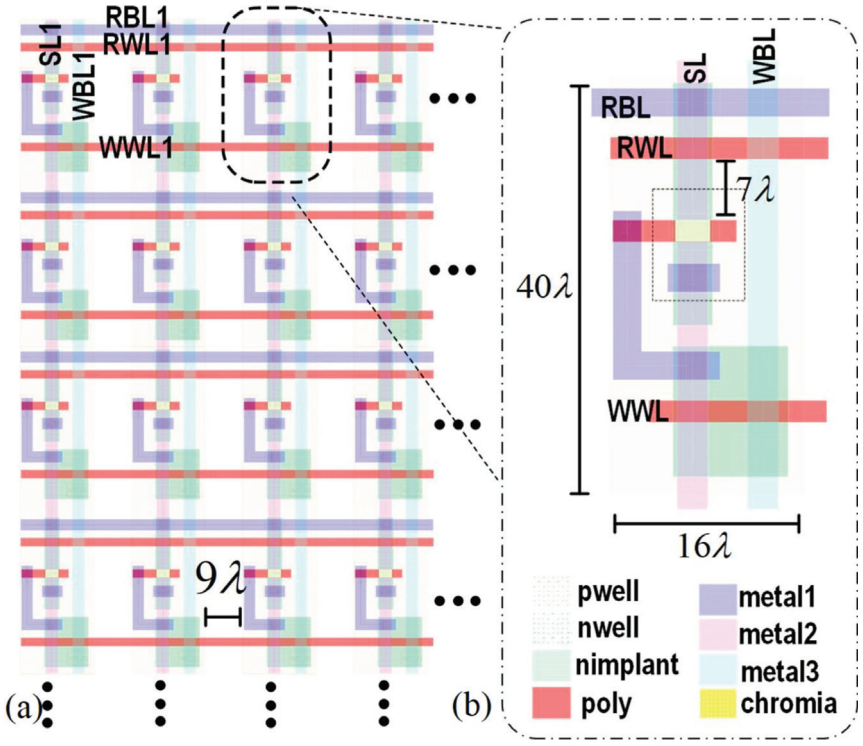

Fig. 8. Layout of (a) 4 × 4 MeF-RAM array and (b) MeF-RAM bit-cell.

4.3.2 Energy Comparison. Figure 9(a) shows the dynamic energy consumption comparison among L2 candidates. The dynamic energy consumption varies based on the workload characteristics (e.g., read/write intensity), and the power required for read/write operation in the given memory technology. In particular, the workloads with higher $\frac{write}{read}$ ratio impose considerably more dynamic energy in the candidates with high write energy consumption such as STT-MRAM. As an example, the dynamic energy consumptions for heavily write-intensive `facesim` and `ferret` are 6.09 mJ and 5.22 mJ, respectively, in the STT-MRAM-based L2 candidate, which are considerably higher than other candidates. On the other hand, the read-intensive workloads such as `streamcluster` experience a relatively higher number of read accesses. Thus, running the read-intensive workloads incurs considerable high dynamic energy consumption in the candidates with relatively energy-costly read access. Among the L2 candidates, the SOT-RAM and MeF-RAM consume the least dynamic power compared to other candidates due to leveraging innovative approaches to control the magnetic state of the memory cell.

The execution time of each workload along with the leakage power unit for each L2 candidate was used to compute the leakage energy. As is noticeable in Figure 9(b), the SRAM incurs significantly higher leakage power, primarily due to its subthreshold leakage paths and the gate leakage current. Among the L2 candidates, the MeF-RAM consumes the least leakage energy due to its intrinsically energy-efficient operations. Since the leakage energy is the major contributor to the overall energy consumption, the low leakage power consumption can significantly reduce the corresponding EAT for that individual L2 candidate.

4.3.3 Latency Comparison. We utilized the key parameters acquired from NVSim, CACTI, and our MeF-RAM memory library, to compute the overall access latency for read/write operations based on the cache access pattern for each workload, as illustrated in Figure 10(a). To reduce the standard deviation of the simulation results w.r.t. the commercialized design, we integrated the

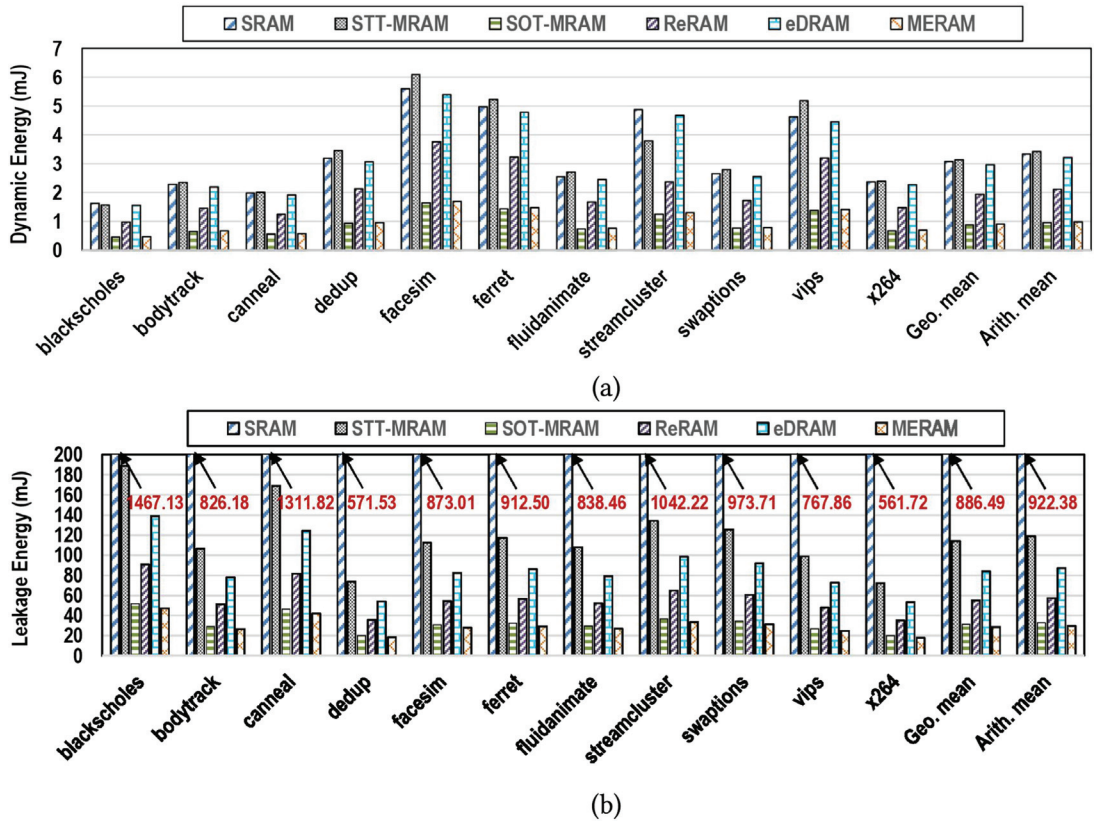

Fig. 9. L2 cache (a) dynamic energy and (b) leakage energy breakdown for SRAM, STT-MRAM, SOT-MRAM, ReRAM, eDRAM, and MeF-RAM.

acquired profiles with the latency associated with the peripheral circuits. The SRAM offers rapid read/write access compared to other L2 candidates because of its symmetrical structure that enables easily detectable minor voltage swings. The MeF-RAM is the closest candidate to SRAM, which offers significantly low read/write latency. This means that SRAM and MeF-RAM should benefit from their low overall latency while estimating EAT for each L2 candidate.

4.3.4 EAT Product. The MeF-RAM offers an SRAM-competitive performance, superior energy consumption, and admissible area overhead compared to other candidates, making it the preferred L2 candidate. As illustrated in Figure 10(b), the MeF-RAM delivers the least EAT among the L2 candidates. Compared to SOT-RAM, which was considered the superior alternative, MeF-RAM reduces the EAT by 70.81% on average. In the heavily write-intensive workloads like `vips` and `facesim`, the EAT is reduced by 71.74% and 71.44%, respectively, relative to delivered EAT in SOT-RAM. This trend is also seen in the read-intensive `streamcluster` workload, whereby the EAT reduced by 68.63% w.r.t. delivered EAT in the SOT-MRAM candidate. To be specific, MeF-RAM decreases the EAT by 80.26%, 82.48%, 94.57%, and 98.12% w.r.t. ReRAM, eDRAM, STT-MRAM, and SRAM, respectively.

5 CONCLUSION

In this work, we presented a non-volatile 2T-1MEFET memory bit-cell with separate read and write paths. We designed a device-to-architecture cross-layer evaluation framework to quantitatively analyze and compare the proposed design with other memory architectures. Our simulation results showed that MeF-RAM offers an SRAM-competitive performance, superior energy consumption,

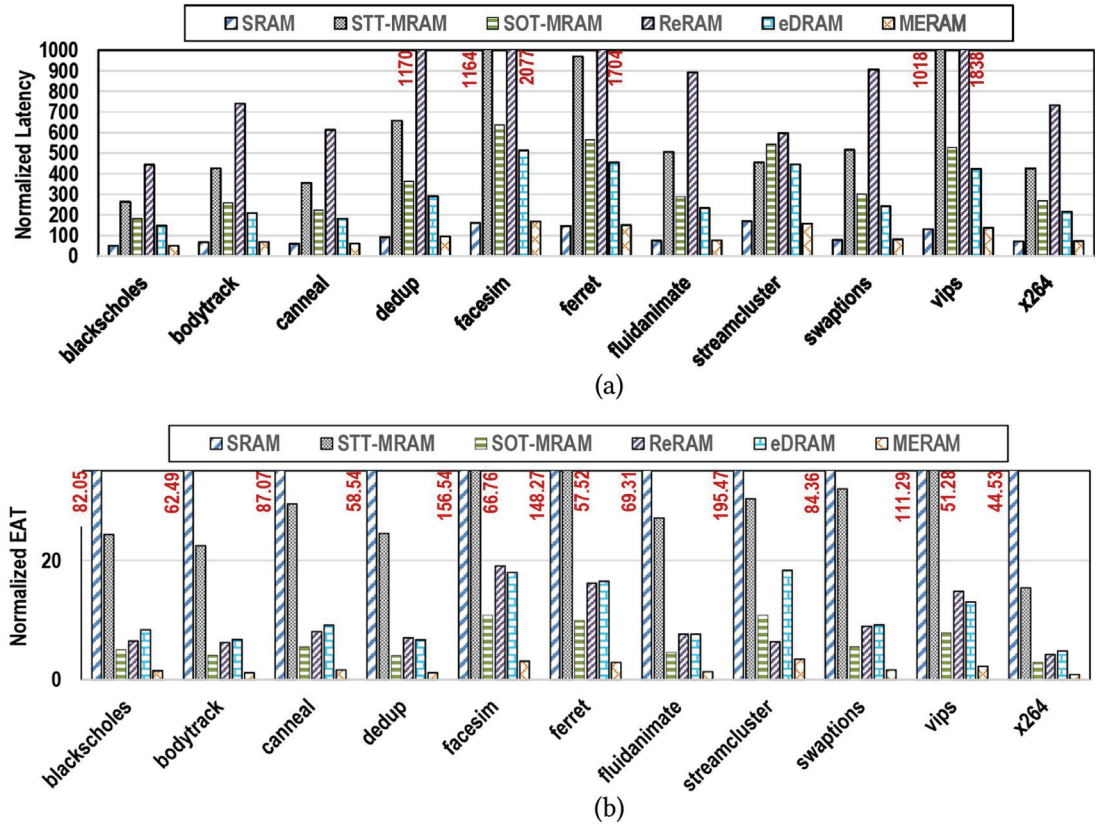

Fig. 10. (a) Latency comparison and (b) EAT comparison of various L2 candidates. The results are normalized w.r.t. the average of latency (ns)/EAT for SRAM across all workloads and among various L2 candidates.

and admissible area overhead compared to other candidates, making it the preferred L2 candidate. As an L2 cache alternative, MeF-RAM reduces EAT product on average by ~98% and ~70% relative to the 6T SRAM and 2T SOT-MRAM platforms, respectively. We believe such circuit/architecture experiments can bring important motivation and guidance to device-level researchers in this domain to see the potential performance of this new emerging paradigm.

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