Electro-Thermal Investigation of GaN Vertical Trench MOSFETs

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***Abstract*— An electro-thermal co-design study has been performed on vertical GaN transistors (oxide, GaN interlayer based vertical trench MOSFETs; OG-FETs). Vertical (GaN-on-GaN) and quasi vertical (GaN-on-sapphire) devices were investigated. Vertical devices showed a 60% lower device peak temperature rise as compared to the quasi-vertical OG-FETs. Using electro-thermal device simulation, the internal electric field and heat generation distributions within the OG-FETs were analyzed. The temperature rise of a hexagonal honeycomb structured scaled array of OG-FETs was characterized using thermoreflectance thermal imaging and infrared thermography. A 3D thermal model was used to evaluate the impact of design variables including the number of cells, the pitch between individual cells, and the aspect ratio of the array configuration on the self-heating behavior of multi-cell arrays of OG-FETs.**

***Index Terms*— Electrothermal effects, gallium nitride, power MOSFET, thermoreflectance imaging, thermal management of electronics.**

I. Introduction

GALLIUM nitride (GaN) is one of the most promising semiconductors for building high-frequency and high-power electronic devices due to its wide bandgap, high saturation velocity, large breakdown field and good bulk thermal conductivity [1], [2]. GaN power devices commercialized to date include lateral AlGaN/GaN high electron mobility transistors (HEMTs) and vertical Schottky barrier diodes [1] However, the lateral HEMT structures are limited to medium voltage (650-900V) power switching, and do not scale effectively to support higher voltages. In order to design a HEMT for larger breakdown voltages, the gate-to-drain spacing needs to be increased, resulting in a larger device footprint and a reduction in the effective current density per unit area, leading to increased chip size and cost. Furthermore, this negatively impacts the high-speed switching performance of the device due to the increased parasitic elements. In contrast, for vertical devices, the blocking voltage is enhanced by increasing the drift layer thickness, without compromise of the device footprint. Additional advantages for the vertical configuration includes larger threshold voltage, peak electric field buried in the GaN bulk, and the absence of current collapse. [3], [4]

Recent advancements in three-terminal GaN vertical devices include the development of the current aperture vertical electron transistor (CAVET) [5]–[9] and other forms of MOSFETs [10]–[12], including the oxide-GaN interlayer-based field effect transistor (OG-FET/OGFET) [9], [13]. While the CAVET is similar to a double-diffused metal oxide semiconductor, the OGFET is similar to a trench MOSFET that includes a GaN interlayer grown via metal organic chemical vapor deposition (MOCVD) to reduce the device ON-resistance. [3]

Work by Ji *et al.* [3] has shown the superior electrical performance and power handling capability of OGFETs fabricated on GaN substrates (vertical OGFET; V-OGFET) as well as sapphire substrates (quasi-vertical OGFET; QV-OGFET). While a breakdown voltage of 700 V was demonstrated, a current density of ~0.5 A was observed for scaled multi-cell arrays with an area of 400 μm × 500 μm. In this work, the thermal characteristics of single-cell and multi-cell arrays of both QV-OGFETs and V-OGFETs were investigated using high resolution optical thermography techniques and coupled electro-thermal modeling.

II. Device Description

The V-OGFET and QV-OGFETs were fabricated atop a hydride vapor phase epitaxy (HVPE)-grown n+ GaN and sapphire substrates, respectively, using metal organic chemical vapor deposition (MOCVD). A MOCVD-regrown unintentionally doped GaN layer of 10 nm thickness serves as the channel in these devices. Details of the fabrication procedure and device design are in reference [3]. An optical image of a V-OGFET and its cross-section are shown in Figs. 1 (a) and (c), with Fig. 1 (b) showing the planar view of a scaled V-OGFET array. Fig. 1 (c) shows measured and simulated I-V characteristics of the V- and QV-OGFET. Transfer characteristics of the devices are shown in Fig. 1(e) [3].

III. Single Cell Device Characterization

Fig. 2 (a) shows the temperature rise of these devices under varying power conditions as obtained from experimental and

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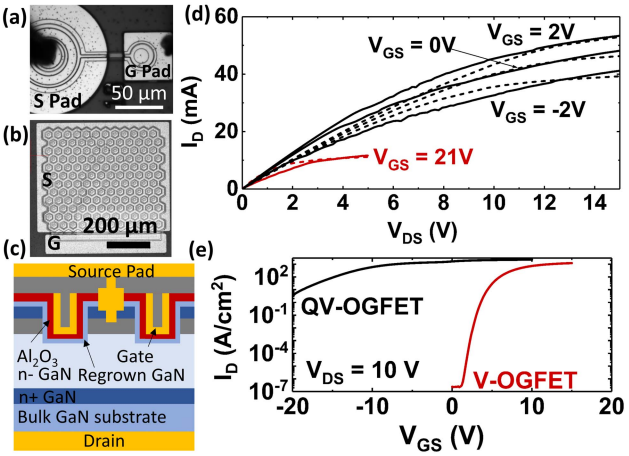

Fig. 1. Top-view of (a) single cell and (b) scaled array of V-OGFETs. (c) Cross-sectional schematic of a V-OGFET. For a similar QV-OGFET, the drain is located near the edge of the device die surface. (d) Output I-V characteristics from measurements (solid-lines) and electro-thermal simulation (dashed-lines). (e) Transfer characteristics for QV- and V-OGFETs. The black and red curves are for a QV-OGFET and a V-OGFET, respectively.

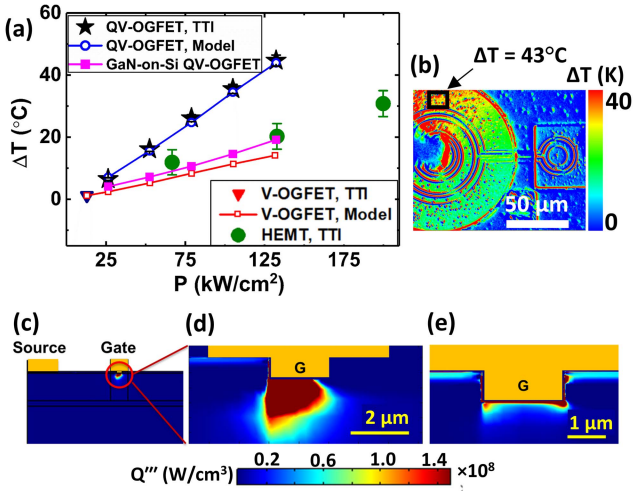

Fig. 2. (a) The temperature rise vs. areal power density of the QV- and V-OGFETs, and an AlGaN/GaN HEMT, obtained from TTI measurements. Also shown are simulation results for the OGFETs, including a GaN-on-Si QV-OGFET. (b) 2D temperature map of a QV-OGFET. (c) Cross-sectional view of the heat generation distribution (Q‴) within a V-OGFET. Zoomed in views of (d) a V-OGFET near the active region and (e) a QV-OGFET near the active region. The areal power densities for (a), (c) (d) and (e) are 132 kW/cm^2.

simulation studies. Both the V- and the QV- OGFETs were characterized via thermoreflectance thermal imaging (TTI) and results were confirmed using infrared (IR) thermography, both of which are in-situ optical thermography techniques. While IR thermography works for high-emissivity surfaces and offers relatively low spatial resolution (~3 μm), TTI is particularly suitable for measuring metallization temperatures, with a higher spatial resolution (~0.78 μm in this study). Details of the thermal characterization procedures can be found in [15].

Fig. 2 (b) shows the 2D temperature map of a QV-OGFET under a power dissipation level of P = 500 mW (132 kW/cm^2; areal power density based on the area enclosed by trench sidewalls) at V_{GS} = 0V and V_{DS} = 13.3V. The device temperature rise (ΔT) is represented by the average temperature within the rectangular region of interest shown in Fig. 2 (b). For the V-OGFETs, the maximum power level during testing was limited to 50 mW (13.2 kW/cm^2) due to the low current levels, resulting in a minimal ΔT.

To compare the self-heating behavior of the V- and QV-OGFETs at higher power conditions, an electro-thermal model was built by coupling a 2D electrical model (Synopsys Sentaurus) with a 3D finite element thermal model (COMSOL Multiphysics). The electrical model accounts for temperature dependent parameters such as electron mobility, electronic bandgap, and thermal conductivity. Details of the coupled modeling procedure can be found in references [16], [17]. The thermal conductivity of the GaN substrate and various GaN layers (with different doping schemes/levels) were adopted from our previous work and a report by Song *et al.* [18] and Beechem *et al.* [19]. The electrical and thermal modeling outputs for both QV- and V-OGFETs were validated as illustrated in Fig. 1 (c) (I-V curves) and Fig. 2 (a) (device surface temperatures).

A comparison between the V- and QV-OGFETs and a typical GaN-on-Si AlGaN/GaN HEMT is shown in Fig. 2 (a). Also shown is the simulation result for a GaN-on-Si QV-OGFET with an identical device design as the GaN-on-Sapphire QV-OGFET. Details of the HEMT structure and thermal characterization results can be found in the authors' prior work [15]. The V-OGFET, GaN-on-Si QV-OGGET and the lateral HEMT exhibit a comparable ΔT for similar areal power densities (i.e., heat flux conditions). However, the channel ΔT the GaN-on-sapphire QV-OGFET was ~3× higher under identical power dissipation levels, as shown in Fig. 2 (a). This difference is mainly attributed to the poor thermal conductivity of the sapphire substrate (κ = 35-40 W/mK at 300 K) as compared to bulk GaN (κ ~ 200 W/mK at 300 K). [18]

Fig. 2 (b) shows a surface temperature map of an operational QV-OGFET under V_{GS} = 0V, V_{DS} = 13.3V, P = 500 mW (132 kW/cm^2). Hotter regions form near the gate ring, also confirmed via electro-thermal modeling. As shown in Figs. 2 (c)-(e), for both the V- and QV-OGFETs, the internal heat generation profile, Q‴ (x,y) is mainly concentrated within the GaN interlayer. Here Q‴ (x,y) is the distribution of volumetric heat generation (units: W/cm^3) representative of the internal Joule heating. This concentrated pattern of Q‴ is a result of the electron current density fields within these devices (not shown), that exhibit similar patterns as the Q‴. However, in case of a V-OGFET, a relatively large portion of Q‴ occurs within the drift region underneath the trench, as compared to a QV-OGFET. The heat generation is more distributed in the vertical device since the current flows through the n+ GaN substrate. The differing Q‴ profiles of each device configuration determine the distinct surface temperature patterns for the two types of OGFETs. It should be noted that Q‴ (x,y) is also a function of the drift region resistance. With an order of magnitude reduction in the drift region doping density, the peak Q‴ near the center of the trench can reduce by ~30%.

To evaluate the fractional contributions of the device configuration and the substrate thermal conductivity to the higher peak temperatures observed in the QV-OGFET, simulation was performed to model a QV-OGFET employing a GaN substrate, at P = 500 mW (132 kW/cm^2), identical to the case of Fig. 2(a). It was found that the QV-configuration (which determines the current and Q‴ distributions) and the lower

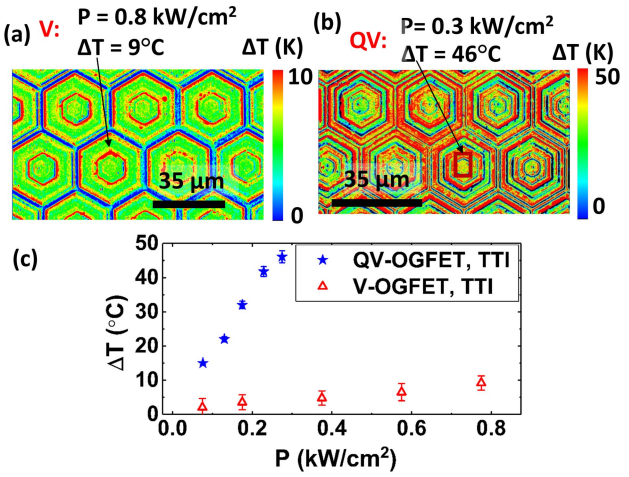

Fig. 3. Surface temperature maps of (a) V-OGFET and (b) QV-OGFET arrays. (c) Increase in ΔT vs. power density for V- and QV-OGFETs.

κ of sapphire contribute 13% and 87%, respectively, to the higher ΔT observed in the QV-OGFET.

IV. High Density Cell Arrays of OGFETs

In order to overcome the relatively low current level of the single cell V-OGFETs, high density V-OGFET arrays with an active area as large as 0.4 mm $\times$ 0.5 mm have been demonstrated in the authors' previous work. [3] The surface ΔT of these cell arrays were determined using the TTI technique, as shown in Fig. 3. Fig. 3 (a) shows a temperature map of a V-OGFET scaled array with a 12×12 honeycomb cell arrangement, which is dissipating 2 W of power (0.8 kW/cm^2). A temperature map of a 42 $\times$ 12 QV-OGFET array is shown in Fig. 3 (b) under a power dissipation level of 0.3 kW/cm^2. Similar to the case of single cell devices, the QV-OGFET cell array exhibits higher temperatures, as shown in Fig. 3 (c). The ΔT is considerably higher than the V-OGFET arrays even under lower power density operation.

V. Thermal Design of the Multi-Cell Arrays

The cell arrays can be arranged with different aspect ratios and with different pitch between adjacent cells. These can lead to varying levels of device peak temperatures even under identical power density conditions, that will impact the device performance and reliability [20]. Thermal models were used to investigate the impact of these design variables. It was observed that the V-OGFET arrays would show ΔT ~19°C under ~1.2 kW/cm^2 power density conditions (demonstrated in [3]). Results are summarized in Fig. 4 (a) and (b).

Fig. 4 (a) shows that the ΔT for the center unit cell of a 50 $\times$ 10 scaled cell array can be more than ~30$\times$ hotter than a single cell OGFET dissipating an identical power per unit cell condition of 100 mW (4.6 kW/cm^2). This reveals the amplified self-heating that individual cells will experience for scaled array configurations, as compared to single cell devices. The higher ΔT for these scaled cell-arrays is attributed to the Neuman (adiabatic) thermal boundary condition formed between single cells at the planes of symmetry. In other words, the thermal cross-talk among individual cells impede the lateral (in-plane) heat diffusion towards the die periphery, thus increasing the device thermal resistance.

Fig. 4 (b) shows that by increasing the distance between two neighboring devices, ΔT can be reduced by a large extent,

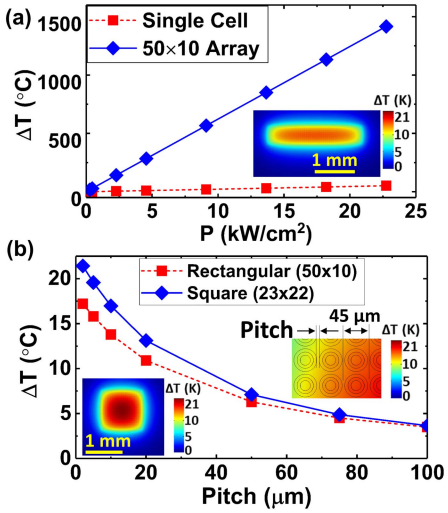

Fig. 4. (a) Surface peak temperature rise (ΔT) of a unit cell device and a 50 $\times$ 10 cell array as a function of power dissipation. (b) The ΔT of cell arrays with different aspect ratio and inter-cell pitch. The insets in (a) and (b) show thermal modeling results for 50 $\times$ 10 and 23 $\times$ 22 cell arrays, respectively, with a pitch of 2 μm, operating under 6 mW/cell.

albeit at the cost of the device footprint. On the other hand, packing cells in a lower aspect ratio design is unfavorable in terms of thermal performance as a square-shaped scaled design of 23 $\times$ 22 cell arrangement (504 cells) shows ~20% higher ΔT, as compared to a rectangular-shaped 50 $\times$ 10 (500 cells) scaled cell array. These findings substantiate the importance of the cell packing arrangement on the overall device thermal resistance. The superiority of higher aspect ratio designs in terms of thermal performance has been reported for multi-finger GaN HEMTs. [21], [22]

To understand the thermal response of the OGFET arrays under transient conditions similar to power switching operation, thermal simulations were run at frequencies of 100 kHz and 1 MHz, [23] under an on-state power dissipation level of 100 W (~9.1 kW/cm^2) and 10% duty cycle. Under such switching speeds, the QV- and V-OGFETs showed identical ΔT. This is attributed to the limited extent of thermal diffusion of the generated heat from the active region so that the substrate thermal conductivity is rendered inconsequential. The resulting ΔT was observed to be ~5% of that for DC operation, in case of the V-OGFET for a 1 MHz switching frequency. This suggests that self-heating would have less impact on the device performance and reliability under such operating conditions.

VI. Conclusion

In this report, OGFETs have been characterized using TTI, an in-situ optical thermography technique. The peak ΔT of a single-cell GaN-on-GaN V-OGFET was shown to be 68% lower than that for a GaN-on-sapphire QV-OGFET, due to the higher thermal conductivity of the GaN substrate and the difference in the current flow pattern. For both devices, majority of Joule-heating is concentrated near the trench and the GaN interlayer. A scaled QV-OGFET cell array was shown to experience a ~30$\times$ higher peak temperature than a single cell OGFET dissipating an identical power per unit cell (100 mW/cell). This is due to the thermal cross-talk between closely packed unit cells. By increasing the inter-cell pitch and the array aspect ratio, the peak temperature of OGFET cell arrays can be significantly reduced.

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