

LETTER

130 mA mm⁻¹ β -Ga₂O₃ metal semiconductor field effect transistor with low-temperature metalorganic vapor phase epitaxy-regrown ohmic contacts

To cite this article: Arkka Bhattacharyya *et al* 2021 *Appl. Phys. Express* **14** 076502

View the [article online](#) for updates and enhancements.

You may also like

- [Frontiers in urethra regeneration: current state and future perspective](#)

Igor Vasyutin, Denis Butnaru, Alexey Lyundup *et al.*

- [GaN-on-silicon transistors with reduced current collapse and improved blocking voltage by means of local substrate removal](#)

Idriss Abid, Eleonora Canato, Matteo Meneghini *et al.*

- [Shear stress induced by fluid flow produces improvements in tissue-engineered cartilage](#)

E Y Salinas, A Aryaei, N Paschos *et al.*



130 mA mm⁻¹ β -Ga₂O₃ metal semiconductor field effect transistor with low-temperature metalorganic vapor phase epitaxy-regrown ohmic contacts

Arkka Bhattacharyya^{1*} , Saurav Roy¹, Praneeth Ranga¹ , Daniel Shoemaker², Yiwen Song², James Spencer Lundh², Sukwon Choi^{2*} , and Sriram Krishnamoorthy^{1*}

¹Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, Utah, 84112, United States of America

²Department of Mechanical Engineering, The Pennsylvania State University, University Park, Pennsylvania, 16802, United States of America

*E-mail: a.bhattacharyya@utah.edu; sukwon.choi@psu.edu; sriram.krishnamoorthy@utah.edu

Received April 21, 2021; revised May 20, 2021; accepted June 3, 2021; published online June 22, 2021

We report on the first demonstration of metalorganic vapor phase epitaxy-regrown (MOVPE) ohmic contacts in an all MOVPE-grown β -Ga₂O₃ metal semiconductor field effect transistor (MESFET). The low-temperature (600 °C) heavy (n⁺) Si-doped regrown layers exhibit extremely high conductivity with a sheet resistance of 73 Ω/◻ and a record low metal/n⁺-Ga₂O₃ contact resistance of 80 mΩ-mm and specific contact resistivity of 8.3 × 10⁻⁷ Ω·cm² were achieved. The fabricated MESFETs exhibit a maximum ON current of 130 mA mm⁻¹ and a high I_{ON}/I_{OFF} ratio of >10¹⁰. Thermal characterization was also performed to assess the device self-heating under the high current and power conditions.

© 2021 The Japan Society of Applied Physics

β -Ga₂O₃, being an ultra-wide bandgap material ($E_g = 4.6\text{--}4.9$ eV), has a projected performance advantage over other predominant wide bandgap semiconductors such as SiC and GaN.^{1,2)} With an added advantage of potentially being cost-effective due to the availability of large-area melt-grown bulk substrates, it has the potential to be the material of choice for next generation solid state power switching applications. Demonstration of β -Ga₂O₃-based field effect transistors with average breakdown fields of up to 5.5 MV cm⁻¹ and breakdown voltages of 8 kV not only strengthens this promise but also demonstrates the rapid progress and breakthroughs achieved in β -Ga₂O₃-based device designs and device processing technologies and high-quality material growth.^{3–9)} Further advancement of material and device engineering and processing is critical to achieving high breakdown voltage and low ON resistance with high ON current simultaneously.

Low resistance ohmic contacts are an essential part of any device, apart from high mobility channel layers, to realize high performance β -Ga₂O₃-based transistors with high current densities and lower conduction losses. To avoid gate-recessing, various techniques such as Si-ion implantation, spin-on-glass, regrown contact layers using molecular-beam epitaxy (MBE) and pulsed-laser deposition have been developed to realize source/drain (S/D) ohmic contacts in Ga₂O₃-based MOSFETs and metal–semiconductor field effect transistors (MESFETs).^{10–14)} While regrown contacts have reportedly provided the lowest contact resistances, the Ga₂O₃ devices in literature which have used regrown S/D contacts have so far mostly relied on the MBE technique to regrow the heavily-doped n⁺ regions.¹³⁾ Metalorganic vapor phase epitaxy (MOVPE) as an epitaxial growth technique has the advantage of growing β -Ga₂O₃ homoepitaxial films with high room-temperature electron mobility values (close to the theoretical limit) and could be promising for fabricating Ga₂O₃ lateral FETs with high current densities.^{15–22)} In this work, we demonstrate for the first time, using selective area epitaxy approach, the realization of low resistance regrown S/D contacts in a fully MOVPE-grown Ga₂O₃ lateral MESFET with high current densities and comparatively high average electric-field (without field plates or passivation).

The epitaxial structure shown in Fig. 1(a) was grown using an Agnitron Agilis MOVPE reactor. A 500 nm thick lightly

Si-doped (1.7×10^{17} cm⁻³) β -Ga₂O₃ channel was grown on a (010) Fe-doped semi-insulating Ga₂O₃ substrate (NCT Japan) at a temperature of 810 °C using triethylgallium, O₂ and silane gases as precursors and Ar as the carrier gas. Prior to loading into the growth reactor, the substrate was dipped in a diluted HF solution for 30 min. From Hall measurements, the channel charge and mobility were measured to be 5.7×10^{12} cm⁻² and 132 cm² V⁻¹ s⁻¹, respectively, giving a channel sheet resistance $R_{sh, ch} = 8.2$ kΩ/◻.

The device mesa isolation was performed using a Ni/SiO₂ hard mask and SF₆/Ar plasma chemistry based ICP-RIE dry etching all the way to the substrate. A selective area MOVPE regrowth process was developed to obtain low-resistance S/D ohmic contacts. First, a sacrificial 500 nm thick SiO₂ layer was blanket-deposited using plasma-enhanced chemical vapor deposition. The S/D contact regions were then defined using a Ni layer patterned by photolithography and lift-off. Using Ni as the hard mask, the SiO₂ in the S/D contact regions was removed by the same SF₆/Ar plasma based directional ICP-RIE dry etching (150 W RF and 600 W ICP). The etching in the contact regions was extended down to the Ga₂O₃ layer with estimated Ga₂O₃ trench depths of 10–20 nm. The Ni mask was then selectively removed by dipping the sample in a diluted aqua regia solution. Next, heavily Si-doped ($\sim 1.8 \times 10^{20}$ cm⁻³) Ga₂O₃ was grown in the open S/D regions using MOVPE at a lowered growth temperature of 600 °C. The ~ 100 nm thick n⁺-Ga₂O₃ growth step was preceded by a heavy Si delta doping at the etched Ga₂O₃ surface in the contact region.^{21,22)} The heavy Si delta doping was done at the etched surface to suppress any epilayer/regrown interface depletion due to any F⁻ ion incorporation caused by the SF₆ dry etching. From Hall measurements on a calibration sample, the volume charge and mobility of the heavily doped n⁺ film were measured to be 1.4×10^{20} cm⁻² and 73 cm² V⁻¹ s⁻¹, respectively, giving a sheet resistance of the n⁺ layer to be 76 Ω/◻. Following the regrowth step, the polycrystalline Ga₂O₃ layer in the regions outside the contact area was removed by dissolving the sacrificial SiO₂ in an HF solution. Ohmic metal stack Ti/Au/Ni (20 nm/100 nm/30 nm) was evaporated on the regrown contact regions by photolithography patterning and lift off followed by a 470 °C anneal in N₂ for

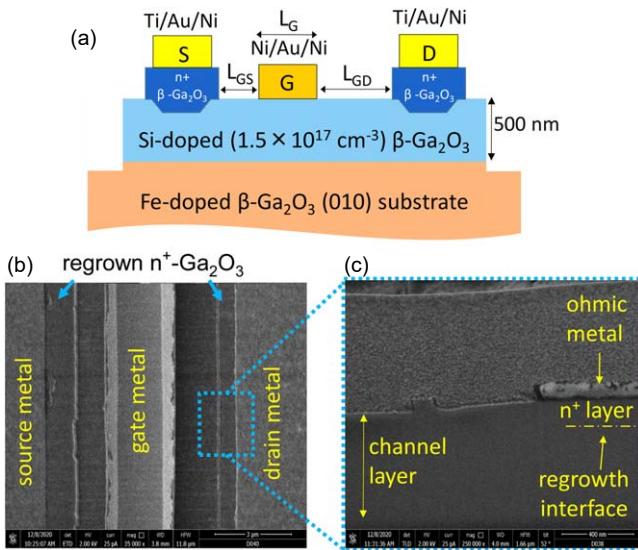


Fig. 1. (Color online) (a) Schematic of the fully MOVPE-grown Ga₂O₃ MESFET with regrown ohmic contacts. (b) Top view SEM image of the MESFET showing the regrown access regions. (c) Cross-sectional SEM of the contact region showing the estimated regrowth interface.

1.5 min. Finally, a Ni/Au/Ni (30 nm/100 nm/30 nm) metal stack was evaporated to form the Schottky gate for the MESFET structure.

Figure 1(b) shows the top-view scanning electron microscope (SEM) image of the MESFET structure. The regrown layers were indistinguishable from the channel region and the surface morphology was similar to that of the channel. From the cross-sectional SEM [Fig. 1(c)] image, no crevices or cracks were visible between the channel and the regrown region. The regrown n⁺-Ga₂O₃/channel interface was very conformal with no visible interface as expected from the MOVPE growth technique.

For a uniformly doped Ga₂O₃ channel with n⁺-Ga₂O₃ contacts, the total contact resistance (R_C) consists of three components: (1) R_{C1} = metal/n⁺ regrown Ga₂O₃ interface contact resistance, (2) R_{n+} = resistance of the regrown n⁺-Ga₂O₃ access region and (3) R_{C2} = n⁺ regrown Ga₂O₃/lightly doped Ga₂O₃ channel interface resistance. Each of these components were extracted from transfer length method (TLM) measurements. From TLM-A (metal contact pads spaced out on the isolated regrown n⁺-Ga₂O₃ slab), sheet resistance of the regrown region ($R_{sh,n+}$) is extracted to be 73 Ω/\square which matched well with the Hall measurement done on the calibration sample mentioned earlier [Fig. 2(a)]. A record low metal/n⁺-Ga₂O₃ interface contact resistance (R_{C1}) of 80 m Ω ·mm and specific contact resistance (ρ_{C1}) of $8.3 \times 10^{-7} \Omega\text{-cm}^2$ were achieved. This shows the low-temperature MOVPE-regrown Ga₂O₃ was of high quality and highly conducting. From TLM-B structure [Fig. 2(b)], $R_{sh,ch}$ and total contact resistance R_C are extracted to be 8.3 k Ω/\square and 12.5 Ω ·mm, respectively. R_{n+} is estimated from the regrown Ga₂O₃ access region dimensions to be 0.2 Ω ·mm²³ giving R_{C2} a value of 12.2 Ω ·mm. This shows the total contact resistance is mainly limited by R_{C2} . As this is a lightly doped channel, this could be due to the etch damage at the regrowth interface caused by the F-based dry etch and could be improved by switching over to a BC_l₃-based dry etching. However, it is to be noted that $R_{sh,ch}$ from TLM after the

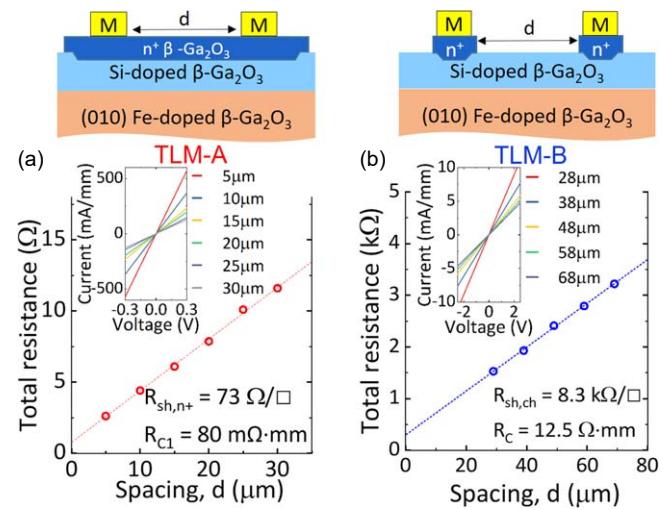


Fig. 2. (Color online) Schematic of TLM structure, corresponding *IV* plots (inset) and total resistance versus contact spacing plots of (a) TLM pads on the MOVPE-regrown n⁺ Ga₂O₃ region and (b) TLM pads with patterned MOVPE-regrown n⁺ ohmic contacts.

regrowth process matches with that of Hall measurements done before the regrowth indicating our low-temperature regrowth process has no detrimental effect on the active region material quality.

Representative DC device output (I_{DS} – V_{DS}) and transfer (I_{DS} – V_{GS}) curves of the fully MOVPE-grown Ga₂O₃ MESFET are shown in Figs. 3(a) and 3(b) with device dimensions of $L_{GS}/L_G/L_{GD} = 1 \mu\text{m}/1.7 \mu\text{m}/1.6 \mu\text{m}$. The maximum normalized drain-to-source current ($I_{DS,MAX}$) was recorded to be 130 mA mm⁻¹ at zero gate bias and a drain bias of 15 V. The device exhibits a subthreshold slope of 122 mV dec⁻¹ and a very large I_{ON}/I_{OFF} ratio of $>10^{10}$ with the OFF-state current mainly limited by the measurement tool detection limit (below noise floor). From the transfer curve, a threshold voltage of -25 V and a max transconductance of 4.8 mS mm⁻¹ (at $V_{GS} = -15$ V) were extracted. It is to be noted that our MESFET exhibits a high ON current

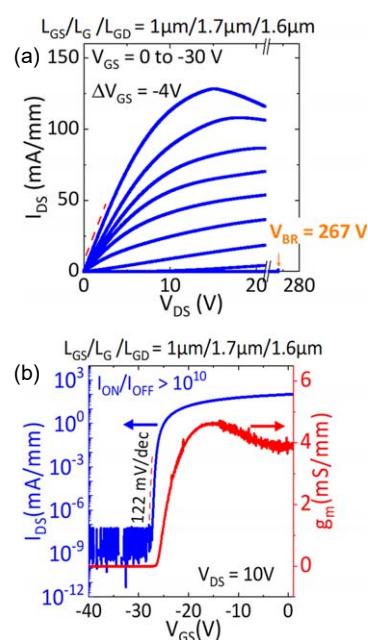


Fig. 3. (Color online) (a) Output characteristics and (b) transfer characteristics of the fully MOVPE-grown beta-Ga₂O₃ MESFET with regrown S/D contacts.

(130 mA mm⁻¹) without even operating at a positive V_{GS} and an extremely low leakage ($<10^{-12}$ A mm⁻¹) simultaneously, thus giving our depletion-mode (D-mode) β -Ga₂O₃ channel MESFET one of the highest I_{ON}/I_{OFF} ratio in its class. This was achieved by the proper substrate preparation to suppress the parasitic channel at the epilayer/substrate interface, maintaining a high-quality of the MOVPE-grown channel layer on the modified substrate and low-temperature device processing (low-temperature MOVPE contact regrowth) that preserved the high-mobility of carriers in the active region. Using TLM and capacitance–voltage (CV) measurements, the effective drift mobility of carriers in the channel region was estimated to be ~ 130 cm² V⁻¹ s⁻¹ for $V_{GS} = 0$ V. Further improvement in the maximum ON currents and device performance can be achieved by realizing an accumulation channel (positive gate bias) by adopting a MOSFET structure and higher channel length to thickness ratio (higher channel aspect ratio) for improved gate control.

Three-terminal OFF state breakdown measurements were performed in Fluorinert solution at V_{GS} of -30 V. A breakdown voltage (V_{BR}) of 267 V was extracted for a device with $L_{GD} = 1.6$ μ m. Using a 2D Sentaurus TCAD simulation of the actual structure, the peak and effective average breakdown fields were estimated to be ~ 7 MV cm⁻¹ and 1.9 MV cm⁻¹, respectively, for this device with $L_{GD} = 1.6$ μ m. With a calculated specific ON resistance ($R_{on,sp}$) of 3.7 m Ω ·cm², the power figure of merit (FOM) is estimated to be 19 MW cm⁻². The $R_{on,sp}$ is the ON resistance normalized to the device active region ($W \times L_{SD}$) after extracting the resistance from the linear part of the output curve at $V_{GS} = 0$ V where W and L_{SD} stands for the width and the source-to-drain length of the transistor. By increasing L_{GD} , the maximum V_{BR} measured is 778 V for $L_{GD} = 20$ μ m. Figure 4(b) shows the $I_{DS,MAX}$ and V_{BR} as a function of L_{GD} in these devices. The maximum power FOM of 25 MW cm⁻² was achieved for a device with $L_{GD} = 5$ μ m. This FOM value is higher than most of the D-mode β -Ga₂O₃ channel MESFETs which do not implement any field-management or passivation techniques.

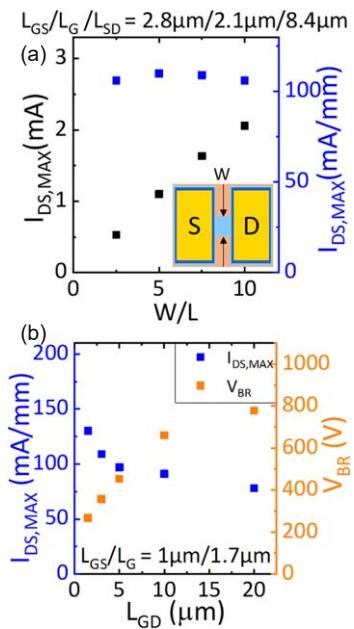


Fig. 4. (Color online) (a) $I_{DS,MAX}$ for devices with different channel width to length ratios (W/L) (b) $I_{DS,MAX}$ and V_{BR} of devices with different L_{GD} .

Absolute $I_{DS,MAX}$ values are measured in devices with smaller channel widths (W) while the channel length (L) was held constant [schematic in Fig. 4(a) inset] that led to devices with different channel width to length ratio (W/L) across the same wafer keeping all other device dimensions ($L_{GS}/L_G/L_{SD} = 2.8$ μ m/2.1 μ m/8.4 μ m) the same. For these long channel devices, the absolute $I_{DS,MAX}$ values scaled linearly with W/L as shown in Fig. 4(a). The normalized $I_{DS,MAX}$ values remain constant throughout the W/L ratio. This indicates the $I_{DS,MAX}$ values in these devices are not limited by the contact resistance of the S/D ohmic contacts. In fact, the $I_{DS,MAX}$ values were limited due to self-heating in these devices evident from the reduction of I_{DS} values at higher V_{DS} values as seen in Fig. 3(a).^{24,25}

To estimate the channel temperature at which self-heating induced current droop occurs in Fig. 3(a) ($V_{GS} = 0$ V, $V_{DS} = 15$ V, $P = 0.96$ W mm⁻¹), the device was characterized via nanoparticle-assisted Raman thermometry using a Horiba LabRAM HR Evolution spectrometer. The temperature was measured by monitoring the E_g mode frequency shift of an anatase TiO₂ nanoparticle deposited near the drain side corner of the gate.²⁶ Experimental results were validated using a three-dimensional finite element thermal model. Details of the thermal modeling procedure can be found in Refs. 26, 27. At the current inflection point in Fig. 3(a) ($P = 0.96$ W mm⁻¹), the estimated channel temperature was 81 °C ($\Delta T \sim 56$ °C). This equates to a thermal resistance of ~ 58.5 mm·°C W⁻¹, which is within the range of values reported in literature.²⁸ To visualize the device self-heating under high power conditions, infrared (IR) thermal microscopy was performed using a QFI medium wavelength infrared InfraScope with a 15 \times objective.²⁹ Results of the thermal analysis are illustrated in Fig. 5(a), while an optical image of the device as well as 2D temperature plots are shown in Fig. 5(b).

In conclusion, we demonstrate the use of MOVPE to realize low-resistance regrown ohmic contacts in a fully MOVPE-grown lateral β -Ga₂O₃ MESFET for the first time. The low-temperature (600 °C) heavy (n⁺) Si-doped regrown layers exhibit extremely high conductivity with sheet resistance of 73 Ω/\square and a record low metal/n⁺-Ga₂O₃ contact resistance of 80 m Ω ·mm and specific contact resistivity of

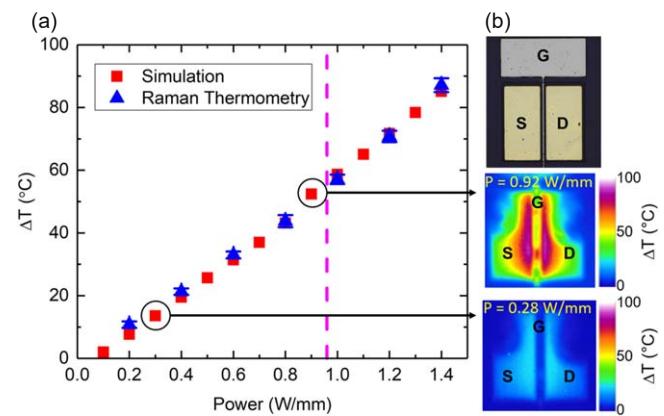


Fig. 5. (Color online) (a) The channel temperature rise determined by Raman thermometry and thermal modeling. The pink dashed line corresponds to the current inflection point shown in Fig. 3(a). (b) Optical image of the device under test and 2D temperature maps generated by IR thermal microscopy corresponding to power densities of 0.92 and 0.28 W mm⁻¹.

$8.3 \times 10^{-7} \Omega \cdot \text{cm}^2$ were achieved. The MESFET shows a maximum current density of 130 mA mm^{-1} at zero gate bias and an extremely low leakage current ($< 10^{-12} \text{ A mm}^{-1}$). Average breakdown field and maximum FOM of 1.9 MV cm^{-1} and 25 MW cm^{-2} , respectively, are achieved even without field-plates or passivation. However, it should be noted that the enabled high current/power capabilities must be supported by effective thermal management solutions [22]. This demonstration of first-generation fully MOVPE-grown $\beta\text{-Ga}_2\text{O}_3$ FETs shows the potential of MOVPE for realizing high ON currents in $\beta\text{-Ga}_2\text{O}_3$ -based devices as well as a promising technique for low-temperature ohmic contact regrowth. Further improvement in device performance can be achieved by implementing field-management techniques in a MOSFET structure along with channel engineering.

Acknowledgments This work was supported by II-VI foundation Block Gift Program. We also thank the Air Force Office of Scientific Research under Award No. FA9550-18-1-0507 (Program Manager: Dr. Ali Sayir) for financial support. Funding for Penn State was provided by the AFOSR Young Investigator Program (Grant No. FA9550-17-1-0141, Program Officers: Dr. Brett Pokines and Dr. Michael Kendra, also monitored by Dr. Kenneth Goretta) and NSF (CBET-1934482, Program Manager: Dr. Ying Sun).

ORCID iDs Arkka Bhattacharyya  <https://orcid.org/0000-0002-7209-5681>
 Praneeth Ranga  <https://orcid.org/0000-0001-9002-1523>
 Sukwon Choi  <https://orcid.org/0000-0002-3664-1542>
 Sriram Krishnamoorthy  <https://orcid.org/0000-0002-4682-1002>

- 1) M. Higashiwaki and G. H. Jessen, *Appl. Phys. Lett.* **112**, 060401 (2018).
- 2) M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, *Appl. Phys. Lett.* **100**, 013504 (2012).
- 3) N. K. Kalarickal, Z. Feng, A. F. M. Anhar Uddin Bhuiyan, Z. Xia, W. Moore, J. F. McGlone, A. R. Arehart, S. A. Ringel, H. Zhao, and S. Rajan, *IEEE Trans. Electron Devices* **68**, 29 (2021).
- 4) S. Sharma, K. Zeng, S. Saha, and U. Singisetti, *IEEE Electron Device Lett.* **41**, 836 (2020).
- 5) A. J. Green et al., *IEEE Electron Device Lett.* **37**, 902 (2016).
- 6) N. K. Kalarickal, Z. Xia, H.-L. Huang, W. Moore, Y. Liu, M. Brenner, J. Hwang, and S. Rajan, *IEEE Electron Device Lett.* **42**, 899 (2021).
- 7) S. Roy, A. Bhattacharyya, and S. Krishnamoorthy, *IEEE Trans. Electron Devices* **67**, 4842 (2020).
- 8) S. Roy, A. Bhattacharyya, P. Ranga, H. Splawn, J. Leach, and S. Krishnamoorthy, arXiv:2105.04413v1.
- 9) S. Roy, A. Bhattacharyya, and S. Krishnamoorthy, arXiv:2008.00280.
- 10) K. Sasaki, M. Higashiwaki, A. Kuramata, T. Masui, and S. Yamakoshi, *Appl. Phys. Express* **6**, 086502 (2013).
- 11) K. Zeng, J. S. Wallace, C. Heimburger, K. Sasaki, A. Kuramata, T. Masui, J. A. Gardella, and U. Singisetti, *IEEE Electron Device Lett.* **38**, 513 (2017).
- 12) K. D. Chabal et al., *Semicond. Sci. Technol.* **35**, 013002 (2019).
- 13) Z. Xia, C. Joishi, S. Krishnamoorthy, S. Bajaj, Y. Zhang, M. Brenner, S. Lodha, and S. Rajan, *IEEE Electron Device Lett.* **39**, 568 (2018).
- 14) M. H. Wong, Y. Nakata, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, *Appl. Phys. Express* **10**, 041101 (2017).
- 15) P. Ranga, A. Bhattacharyya, A. Rishinaramangalam, Y. K. Ooi, M. A. Scarpulla, D. Feezell, and S. Krishnamoorthy, *Appl. Phys. Express* **13**, 045501 (2020).
- 16) P. Ranga, A. Bhattacharyya, A. Chmielewski, S. Roy, R. Sun, M. A. Scarpulla, N. Alem, and S. Krishnamoorthy, *Appl. Phys. Express* **14**, 025501 (2021).
- 17) A. Bhattacharyya, P. Ranga, S. Roy, J. Ogle, L. Whittaker-Brooks, and S. Krishnamoorthy, *Appl. Phys. Lett.* **117**, 142102 (2020).
- 18) Z. Feng, A. F. M. Anhar Uddin Bhuiyan, M. R. Karim, and H. Zhao, *Appl. Phys. Lett.* **114**, 250601 (2019).
- 19) Y. Zhang, F. Alema, A. Mauze, O. S. Koksaldi, R. Miller, A. Osinsky, and J. S. Speck, *APL Mater.* **7**, 022506 (2018).
- 20) G. Seryogin, F. Alema, N. Valente, H. Fu, E. Steinbrunner, A. T. Neal, S. Mou, A. Fine, and A. Osinsky, *Appl. Phys. Lett.* **117**, 262101 (2020).
- 21) P. Ranga, A. Bhattacharyya, A. Rishinaramangalam, Y. K. Ooi, M. A. Scarpulla, D. Feezell, and S. Krishnamoorthy, *Appl. Phys. Express* **12**, 111004 (2019).
- 22) P. Ranga, A. Bhattacharyya, A. Chmielewski, S. Roy, N. Alem, and S. Krishnamoorthy, *Appl. Phys. Lett.* **117**, 172105 (2020).
- 23) J. Guo et al., *IEEE Electron Device Lett.* **33**, 525 (2012).
- 24) M. Higashiwaki, K. Sasaki, T. Kamimura, M. H. Wong, D. Krishnamurthy, A. Kuramata, T. Masui, and S. Yamakoshi, *Appl. Phys. Lett.* **103**, 123511 (2013).
- 25) N. A. Blumenschein et al., *IEEE Trans. Electron Devices* **67**, 204 (2020).
- 26) J. S. Lundh et al., *Appl. Phys. Lett.* **115**, 153503 (2019).
- 27) B. Chatterjee et al., *Appl. Phys. Lett.* **117**, 153501 (2020).
- 28) C. Yuan, Y. Zhang, R. Montgomery, S. Kim, J. Shi, A. Mauze, T. Itoh, J. S. Speck, and S. Graham, *J. Appl. Phys.* **127**, 154502 (2020).
- 29) J. Dallas et al., *Appl. Phys. Lett.* **112**, 073503 (2018).