Diamond-Incorporated Flip-Chip Integration for Thermal Management of GaN and Ultra-Wide Bandgap RF Power Amplifiers

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***Abstract*— GaN radio frequency (RF) power amplifiers offer many benefits including high power density, reduced device footprint, high operating voltage, and excellent gain and power-added efficiency. Accordingly, these parts are enabling next-generation technologies such as fifth-generation (5G) base transceiver stations and defense/aerospace applications such as high-performance radar and communication systems. However, these benefits can be overshadowed by device overheating that compromises the performance and reliability. In response to this, researchers have focused on GaN-on-diamond integration during the past decade. However, manufacturability, scalability, and long-term reliability remain as critical challenges toward the commercialization of the novel device platform. In this work, a diamond-incorporated flip-chip integration scheme is proposed that takes advantage of existing semiconductor device processing and growth techniques. Using an experimentally validated GaN-on-SiC multifinger device model, the theoretical limit of the cooling effectiveness of the device-level thermal management solution has been evaluated. Simulation results show that by employing a ∼2-μm diamond passivation overlayer, gold thermal bumps, and a commercial polycrystalline carrier wafer, the power amplifier's dissipated heat can be effectively routed toward the package, which leads to a junction-to-package thermal resistance lower than GaN-on-diamond high electron mobility transistors (HEMTs). Furthermore, simulation results show that this approach is even more promising for lowering the device thermal resistance of emerging ultra-wide bandgap devices based on β-Ga_2O_3 and AlGaN, below that for today's state-of-the-art GaN-on-diamond HEMTs.**

***Index Terms*— Aluminum gallium nitride, diamond passivation, flip-chip devices, gallium nitride, gallium oxide, radio frequency (RF), Raman scattering, thermal management of electronics, wide bandgap semiconductors.**

I. Introduction

THE GaN high electron mobility transistor (HEMT) architecture offers high voltage/current handling and high-frequency operation capabilities by taking advantage of the material's large critical breakdown field and the two-dimensional electron gas (2DEG) formed via polarization doping [1]. GaN radio frequency (RF) power amplifiers have become key components enabling fifth-generation (5G) cell towers, broadband satellites, high-performance military radar, and electronic warfare systems [2]–[5].

GaN HEMTs have demonstrated RF output power densities of 40 W/mm at S-band [6], 30 W/mm at X-band [7], and 8 W/mm at W-band [8]. However, heat accumulation caused by the extreme energy dissipation in the device channel degrades signal integrity and compromises the component lifetime [9]. Therefore, commercial AlGaN/GaN HEMTs employing silicon carbide (SiC) substrates are typically operated at reduced power levels of 5–8 W/mm to circumvent device self-heating issues.

In order to address the extreme operational heat flux of GaN HEMTs ($q'' > 50$ kW/cm^2) [9], device-level thermal management must precede the application of package- and/or system-level active cooling solutions [10]. For device-level cooling, the main focus has been to replace the SiC substrate of commercial GaN HEMTs with polycrystalline synthetic diamond [11]–[14]. GaN-on-diamond integration has been demonstrated through bonding the GaN epitaxy onto diamond [12], [15]–[19] and direct growth of diamond underneath the GaN buffer [20]–[22]. Enhanced RF performance of 11 W/mm

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output power density at a 40-V drain bias with 51% power-added efficiency (PAE) has been demonstrated [18]. However, the structural rigidity of the GaN/diamond interface under prolonged high power RF operation remains unanswered [23]. The additional fabrication steps associated with the integration process and the limited availability of large diameter of GaN-on-diamond wafers are other roadblocks to the entry into high-volume low-cost manufacturing [24]. Dielectric seeding/adhesive layers are necessary for the integration of GaN and diamond. Therefore, the thermal resistance of these layers must be precisely controlled, in order to maximize the benefit of the GaN-on-diamond technology.

As compared with bottom-side device-level cooling methods (i.e., diamond substrate integration) pursued to date, this work proposes a top-side cooling approach that leverages well-established flip-chip heterointegration processes [25]–[27], augmented by recent breakthroughs in diamond-on-GaN growth [28]–[30]. A 3-D finite element device thermal modeling was created for a commercial multifinger GaN-on-SiC HEMT, which was validated using micro-Raman thermometry. A 480-nm-thick polycrystalline diamond film was deposited on a GaN/sapphire template to measure its thermophysical properties to be used for subsequent modeling of diverse device configurations. Using the experimentally validated device model and the measured thermophysical properties of the diamond film, simulation was performed to quantify the theoretical limit of the cooling effectiveness of a diamond-incorporated flip-chip integration scheme. Furthermore, this device-level thermal management solution was applied to emerging ultra-wide bandgap (UWBG) semiconductor device technologies [31] based on β-Ga_2O_3 and AlGaN, facing overheating as a bottleneck to their commercialization.

II. Sample Description and Experiments

A. Device Thermal Characterization

The channel temperature of a six-finger commercial GaN-on-SiC HEMT, mounted on a CuW package, was characterized using micro-Raman thermography [32]. This device had an identical epitaxial structure described in [33], and the only difference was the reduced number of gate fingers. Details of the Raman measurement setup can be found in [34] and [35]. The center point of the channel closest to the device center was measured at various power levels up to 11.69 W, which corresponds to a linear power density of 5.27 W/mm. The base temperature underneath the CuW package was maintained at 85 °C during the experiments. Measurement and device modeling results (to be discussed in Section III-A) are displayed in Fig. 1.

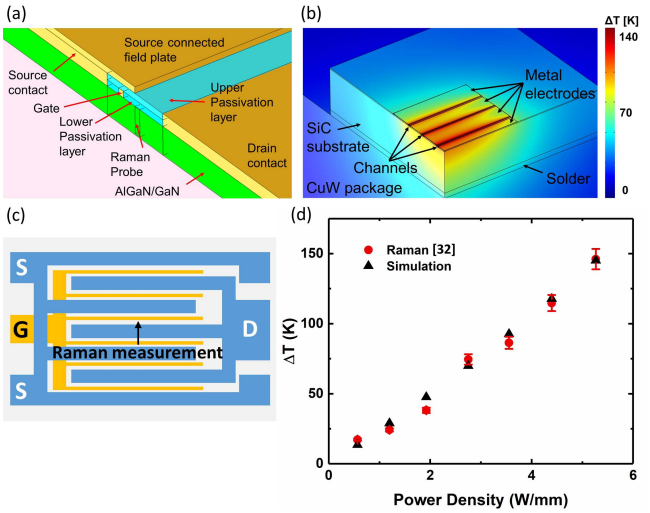

Fig. 1. (a) Cross-sectional view of the channel region of the GaN-on-SiC HEMT model. (b) Quarter-thermal model of the six-finger GaN-on-SiC HEMT operated under a power density of 5.27 W/mm. (c) Planar device layout and measurement location for the Raman thermometry experiments. (d) Measured [32] and simulated channel temperature rise of the six-finger GaN-on-SiC HEMT.

B. Diamond Film Preparation and Thermal Characterization

In order to determine proper diamond thermophysical properties to be used in thermal models with diverse device configurations (to be discussed in Sections III-B and III-C), experiments were performed on a diamond film deposited on GaN. A 480-nm-thick polycrystalline diamond film was grown using a microwave plasma chemical vapor deposition (MPCVD) system (SDS 5000 Seki Diamond Systems) on a Si_3N_4 (20 nm)/GaN (1.17 μm)/sapphire (430 μm) template. The GaN layer was grown by metal organic chemical vapor deposition (MOCVD) on a sapphire substrate. Details of the growth process can be found in [29]. The optimized diamond growth process was shown not to negatively impact the device electrical characteristics [28]. The columnar grain structure of the diamond films (with increasing lateral grain size with film thickness) results in a highly anisotropic thermal conductivity (TC) where the in-plane TC (κ_r) is lower than the cross-plane TC (κ_z) [36]. The effective thermal boundary resistance (TBR) at the diamond/GaN interface includes contributions from the phonon mismatch between materials, the thermal resistance of the dielectric layer used for diamond seeding, and the defective nucleation/coalescence region [11], [37], [38].

Time-domain thermoreflectance (TDTR) and frequency-domain thermoreflectance (FDTR) measurements (previously used in [39]) were performed to determine κ_z and TBR, respectively, by taking advantage of the complementary sensitivities of the two techniques [40]. To minimize the number of fitting parameters during postprocessing, a diamond/GaN/sapphire material stack, GaN/sapphire template, and sapphire substrate were individually prepared and characterized. Au (90 nm)/Ti (7 nm) metal transducers were deposited on the samples and their thicknesses were confirmed by profilometry and cross-sectional scanning electron microscopy (SEM) measurements.

Using TDTR, the TCs of the sapphire substrate and GaN layer were determined to be 37.0 $\pm$ 4.6 and 115.08 $\pm$ 20.42 W/mK, respectively. These room temperature values are similar to those reported in [41] and [42]. The thickness variation of the diamond film [445–521 nm; Fig. 2(a)] and uncertainties associated with the thermal properties of the GaN/sapphire material stack resulted in a κ_z with a relatively large uncertainty (137.4 $\pm$ 42.3 W/mK). It should be noted that κ_z represents the through-thickness average of the cross-plane TC, while κ_z actually increases with the diamond thickness [43], [44].

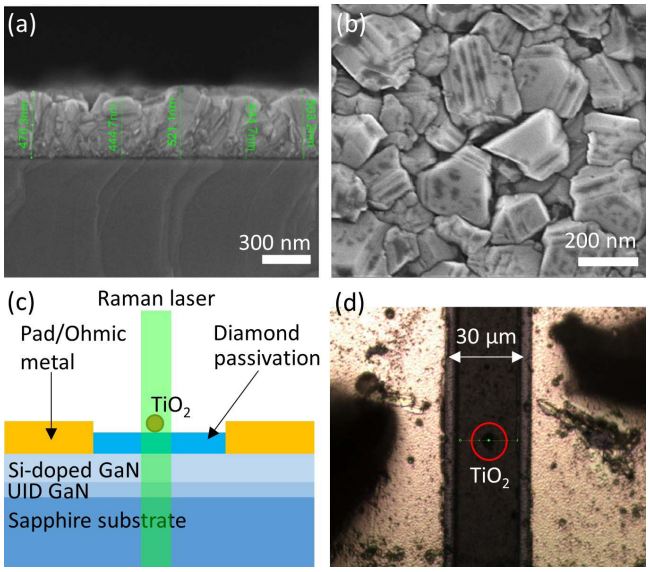

Fig. 2. (a) Cross-sectional and (b) top-side SEM images of the diamond film deposited on a GaN/sapphire material stack. (c) Schematic and (d) optical image of the TLM structure used to estimate κ_r of the diamond layer.

Since both TDTR and FDTR methods did not have the measurement sensitivity to determine κ_r, transmission line measurement (TLM) devices (equivalent to ungated GaN HEMTs) with and without diamond passivation were fabricated. The base material stack consisted of 480-nm diamond/10-nm MOCVD SiN_x/320-nm Si-doped (1×10^{18} cm^{-3}) GaN/120-nm unintentionally doped (UID) GaN/430-μm sapphire substrate and Ti/Al/Ni/Au ohmic contacts, as shown in Fig. 2(c). The channel was 30 μm long and 200 μm wide. Under various power dissipation levels at room temperature, the GaN layer and diamond surface temperature at the center point of each device were measured, using standard [32] and nanoparticle-assisted Raman thermometry [35], [45]. A 3-D finite-element thermal model (COMSOL Multiphysics) was constructed with the mean value of the measured κ_z (137.4 W/mK) employed as a model input parameter. Temperature-dependent TCs for the GaN layers and the sapphire substrate were adopted from [41] and [42]. A constant temperature boundary condition of 25 °C was applied underneath the wafer die (which is consistent with the experimental setup) and a natural convection boundary condition (heat transfer coefficient, $h = 5$ W/mK) was applied to all other surfaces. A parametric sweep was performed to estimate κ_r (~95 W/mK), based on a diamond/GaN TBR of 21.9 ± 3.3 m^{2}K/GW, which was determined from FDTR experiments, that also assumed the mean value of κ_z (137.4 W/mK). It should be noted that the TLM devices had to be operated up to 500 mW to clearly discern the subtle difference in the GaN channel and surface temperature of the TLM devices. At this power condition, the GaN channel (diamond surface) temperature rise for devices with and without the diamond capping layer was 72.6 ± 9.6 K (84.4 ± 1.8 K) and 81.9 ± 12.7 K (87.9 ± 1.9 K), respectively. Despite the fact that this multimethod approach does not rigorously account for the temperature dependence of the diamond thermophysical properties, the derived κ_r, κ_z, and TBR values (Table I) are reasonable when compared with previous reports in literature, also accounting for the relatively large average lateral grain size [~344 nm; Fig. 2(b)] of the tested diamond films [36], [46] and the thickness of the SiN_x (heretofore referred to simply as SiN) dielectric adhesion layer [37], [47]–[49].

TABLE I
MEASURED/ESTIMATED DIAMOND THERMOPHYSICAL PROPERTIES

Thermo-physical property	Value (measurement technique)
Diamond in-plane TC, κ_r	95 W/mK (TLM, Raman, modeling)
Diamond cross-plane TC, κ_z	137.4±42.3 W/mK (TDTR)
Diamond/GaN TBR	21.9±3.3 m^{2}K/GW (FDTR)

III. THERMAL MODELING

A. Conventional Upright Configuration

The 3-D finite-element thermal modeling of a six-finger GaN-on-SiC HEMT was performed using COMSOL Multiphysics. This device has an identical epitaxial structure described in [33], and the only difference is the reduced number of gate fingers. Taking advantage of the fourfold symmetry of the device, a quarter-model was built with an accurate solid geometry that would represent the real device [Fig. 1(b)]. Temperature-dependent TC of constituent materials for the HEMT structure (SiN passivation, AlGaN, GaN, and SiC substrate) and CuW package as well as the GaN/SiC TBR were adopted from [32], [33], and [39]. The die attach material (AuSn solder) TC was 57 W/mK (according to the vendor specifications) and the metal electrodes were assumed to be Au. Since the device was operated under fully open channel conditions ($V_{GS} = 2.5$ V), the Joule heating was assumed to occur uniformly across the channel [50]. A constant temperature boundary condition of 85 °C was applied underneath the CuW package (which is consistent with the experimental setup) and a natural convection boundary condition ($h = 5$ W/mK) was applied to all other surfaces. This conventional device configuration is illustrated in Fig. 3(a). The HEMT structure employs a source connected field plate (SCFP) with physical dimensions similar to that in [51] [Fig. 1(a)]. As shown in Fig. 1, the thermal response of the real device is successfully reproduced by the thermal model.

The SiC substrate of the simulated device was then replaced by polycrystalline diamond to form a GaN-on-diamond HEMT model. The temperature-dependent/anisotropic TC of the synthetic diamond substrate was adopted from [22]. The GaN/diamond substrate TBR was assumed to be the measured value in Table I (21.9 m^{2}K/GW), which is similar to GaN/diamond effective TBRs reported in [52]. Fig. 4 shows the reduction in channel temperature by replacing the SiC substrate into diamond. The thermal resistance of this hypothetical GaN-on-diamond HEMT will serve as a benchmark to assess the cooling performance of the proposed diamond-incorporated flip-chip configuration [Fig. 3(c)].

B. Diamond Passivation

While most near-junction cooling efforts for GaN HEMTs have focused on GaN-on-diamond integration, a smaller

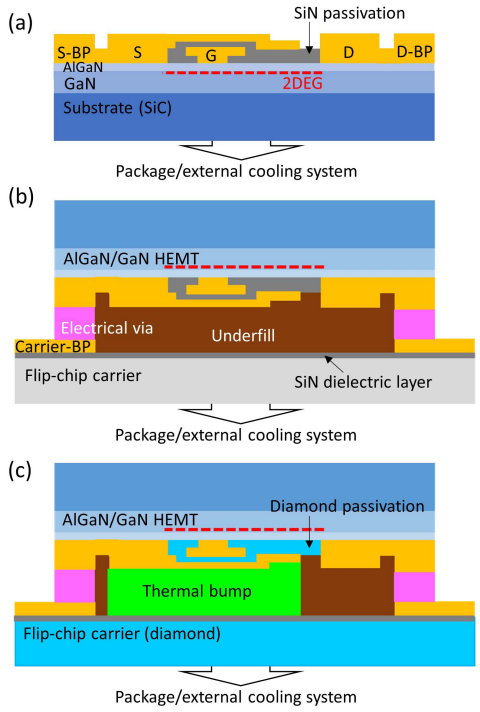

Fig. 3. (a) Conventional upright configuration. (b) Flip-chip integration of the GaN-on-SiC HEMT on a carrier wafer, without consideration of top-side heat extraction. (c) Thermally optimized diamond-incorporated flip-ship configuration. In (a) and (b), BP stands for bond pad.

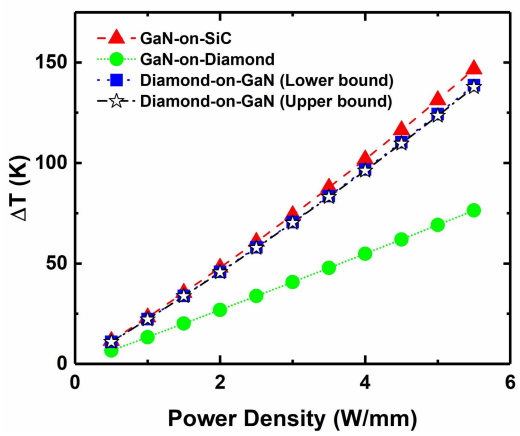

Fig. 4. Channel temperature rise as a function of power density for GaN-on-SiC devices with and without diamond passivation, and a GaN-on-diamond HEMT.

number of efforts have pursued device cooling through nanocrystalline diamond (NCD) coating on SiN-passivated GaN-on-SiC HEMTs [53]–[55]. While these studies demonstrate the resulting improvement in the device direct current (dc) and RF performance, the cooling effectiveness has not been accurately quantified.

The SiN passivation layer of the GaN-on-SiC HEMT model was replaced by a 980-nm-thick diamond passivation layer. While thicker diamond passivation layers will exhibit better cooling performance, the practical diamond thickness is less than ~2 μm in order to prevent degradation of the 2DEG characteristics caused by undesired residual stress effects [28].

TABLE II
ASSUMED DIAMOND THERMOPHYSICAL PROPERTIES FOR CASE STUDIES

Case	Property	Value	References
Lower bound	Thickness	980 nm	
	κ_r (first 490 nm)	46 W/mK	[36]
	κ_r (Second 490 nm)	77 W/mK	[36]
	κ_z (first 490 nm)	89 W/mK	[36]
	κ_z (Second 490 nm)	210 W/mK	[36]
	TBR	24.3 m^{2}K/GW	
Upper bound	Thickness	1960 nm	
	κ_r (first 490 nm)	85 W/mK	[62]
	κ_r (Second 490 nm)	175 W/mK	[62]
	κ_r (third 980 nm)	309 W/mK	[63]
	κ_z (first 490 nm)	142 W/mK	[61]
	κ_z (Second 490 nm)	310 W/mK	[61]
	κ_z (third 980 nm)	510 W/mK	[63]
	TBR	7.3 m^{2}K/GW	

As shown in Fig. 1(a), the diamond passivation layer in the model was split into multiple domains to account for the increase in κ_r and κ_z with the diamond thickness [43], [44]. Two cases of diamond-passivated GaN-on-SiC HEMTs have been simulated, representing the lower bound and upper bound of diamond film thermophysical properties reported in literature (which represent two different diamond layer thicknesses as well as different diamond layer and interface quality).

For the lower bound case, the effective TBR between the 2DEG region (GaN surface) and the diamond passivation layer was assumed to be represented by an effective TBR that lumps the equivalent TBR arising from the 21-nm-thick AlGaN barrier ($\kappa = 8.77$ W/mK [39]) and the measured diamond/GaN TBR of 21.9 m^{2}K/GW in Table I. This calculation results in an effective TBR of 24.3 m^{2}K/GW. The diamond film thickness was assumed to be ~1 μm (980 nm). For the upper bound case, the thermal resistance between the GaN surface and the diamond passivation is represented by a situation where the thickness of the SiN diamond seeding layer is reduced from 20 nm (lower bound case) to 2 nm [28]. Based on the SiN TC of ~1.06 W/mK [56], [57], an 18-nm reduction of the SiN thickness correlates to a reduction of the lumped/effective TBR by ~17 m^{2}K/GW. Therefore, the upper bound effective TBR between the GaN surface and diamond passivation was set to be ~7.3 m^{2}K/GW. The theoretical limit for the effective TBR between GaN and diamond was shown to be 3 m^{2}K/GW, assuming no SiN seeding layer is implemented and only the diffusive mismatch between diamond and GaN contributes to the TBR [58], [59]. By adding the resistive contributions from the 21-nm AlGaN barrier (~2.4 m^{2}K/GW) and the 2-nm SiN seeding layer (~1.9 m^{2}K/GW) to this theoretical value, an identical effective TBR of ~7.3 m^{2}K/GW is derived. These lower/upper bound case TBR values are listed in Table II. It should be noted that the diamond film thickness for this upper bound case was assumed to be ~2 μm (1960 nm) instead of the ~1 μm (980 nm) used for the lower bound. All of the assumptions used to derive the TBR values align with experimental findings reported in [19] and [60]. For instance, Yates *et al.* [60] show a diamond/GaN TBR of 9.5 m^{2}K/GW for a sample with a 5-nm-thick SiN interlayer.

For the lower bound case, the κ_r and κ_z values for the bottom and top 490-nm domains of the diamond passivation layer [Fig. 1(a)] were based on top- and bottom-side TDTR measurements of a 1-μm-thick diamond film reported in [36]. For the upper bound case, the κ_r and κ_z values for the bottom and middle 490-nm domains of the diamond passivation layer were chosen from [61] and [62]. For the top 980-nm domain, κ_r and κ_z were adopted from [63], within the error bar range of the measured values. These references were carefully chosen based on a comparison between the bottom-layer κ_r and κ_z values listed in Table II and those of the diamond film characterized in this work (Table I). It should be noted that the thickness of characterized film is comparable with the bottom-layer passivation layers in Table II. On the other hand, the lateral grain size of the diamond film grown in this work is larger than those in these references (see [36], [61], [62]). This aligns with the fact that κ_z of the characterized film lies between the lower and upper bound cases in Table II, while κ_r is larger than that of the upper bound case.

As shown in Fig. 4, the cooling benefit provided by diamond passivation is minute, regardless of adopting a higher quality diamond layer (upper bound case). This is because the diamond layer is exposed to a natural convection thermal boundary condition. The amount of heat spreading through this layer is much less than the heat dissipated through the substrate and package, i.e., the bottom side is the preferred pathway for heat flow due to the lower thermal resistance. Furthermore, it should be noted that the model assumes κ_r and κ_z of the diamond passivation layer are temperature invariant. For real devices, the cooling effectiveness of the diamond passivated configuration should be inferior to predictions shown in Fig. 4.

C. Flip-Chip Integration

In the previously discussed conventional/upright device configuration, bond wires are used to interconnect the device to external circuitry. In contrast, in the flip-chip approach [64], the device is flipped over so that its bond pads connect with mirror-imaged matching pads on the carrier wafer using electrical vias [Fig. 3(b)]. However, an ordinary flip-chip configuration is inefficient in terms of heat extraction from the device, mainly because of the low TC of the epoxy underfill material (κ = 1.7 W/mK; EPO-TEC 930-4 [65]). Recently, a thermally optimized flip-chip design locating thermal bump heat sinks between the device metal electrodes and the carrier wafer was shown to effectively lower the junction temperature of GaAs heterojunction bipolar transistors (HBTs) [66].

The key to accomplish high heat transfer performance from a flip-chip configuration is to maximize heat conduction from the heat source (for a GaN HEMT, the Joule heating region in the 2DEG) to the thermal bump, which in turn transfers heat to the carrier wafer. The proposed design scheme employs existing growth, processing, and packaging techniques: 1) a 980-nm diamond passivation layer [28] that promotes heat conduction from the 2DEG to the SCFP; 2) 2-μm-tall Au thermal bumps [25]–[27] that transfer heat from the SCFP to the carrier wafer; and 3) a commercial polycrystalline diamond substrate [14], [43], [49] as the carrier wafer that

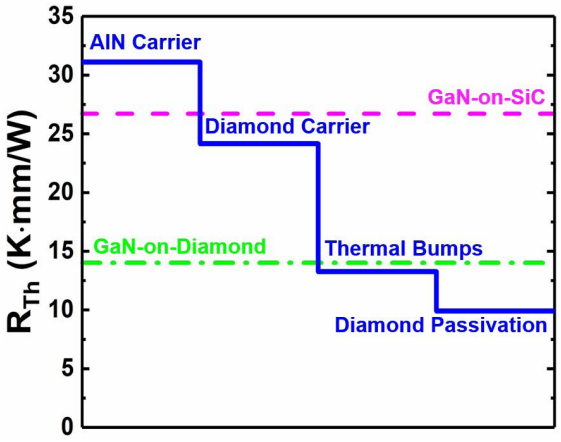

Fig. 5. Thermal optimization process of the flip-chip integration scheme.

spreads/dissipates the heat toward the CuW package. While the SCFP is grounded for most RF power amplifiers, the drain electrode experiences a large RF voltage swing. Therefore, we avoid the use of a thermal bump on the drain electrode that will result in added capacitance that may negatively impact the device RF performance. This diamond-incorporated flip-chip configuration is displayed in Fig. 3(c). In principle, this top-side cooling approach locates the thermal solution in closer proximity to the heat source, as compared with the GaN-on-diamond bottom-side cooling method. In the model, the thickness of the bond pads and interconnects was 2 μm. The carrier wafer length, width, and height were 1600, 1600, and 100 μm, respectively. The 100-nm-thick SiN (κ = 4.5 W/mK) was blanket deposited on the carrier wafer for electrical isolation.

IV. Results and Discussion

To compare the effectiveness of the flip-chip cooling method with the standard cooling methods, various flip-chip configurations were modeled for a GaN-on-SiC HEMT and the results are shown in Fig. 5. The first case was a standard flip-chip configuration with no thermal bumps, SiN passivation, SiC substrate, and an AlN carrier wafer. As expected, this configuration results in an inferior thermal performance as compared with the baseline GaN-on-SiC HEMT. The calculated junction-to-package thermal resistance (Rth) is ~31.1 Kmm/W, which means the channel temperature rise (with respect to the base plate temperature) will be 311 K at 10-W/mm operation. When replacing the AlN carrier wafer with a polycrystalline diamond carrier, the thermal resistance was reduced by 22% (Rth ~ 24.15 Kmm/W). The implementation of thermal bumps is shown to be the most significant factor that further reduces the thermal resistance by 45.1% (Rth ~ 13.25 Kmm/W), making this a more efficient cooling method than the baseline case (GaN-on-SiC HEMT with SiN passivation). However, it should be noted that the simulation results presume perfect bonding (without voids) among the Au bumps and the metallization structures. Finally, replacing the SiN passivation layer with diamond enables to further lower the thermal resistance below that for GaN-on-diamond devices. By implementing the "lower

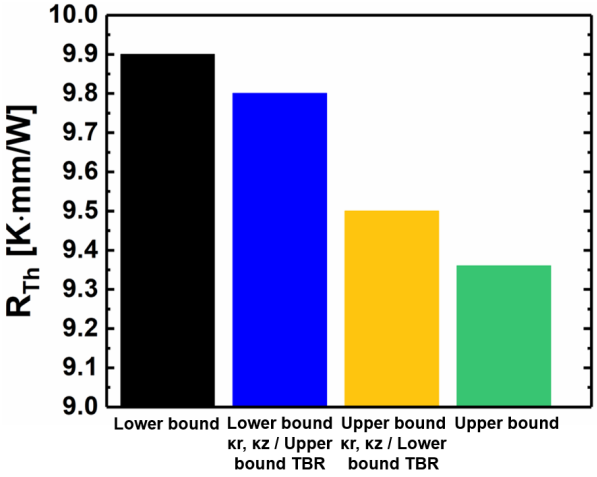

Fig. 6. Reduction in device thermal resistance by improving thermophysical properties of the diamond passivation, for the thermally optimized flip-chip design. All *R*th values were calculated under a power density of 5.5 W/mm.

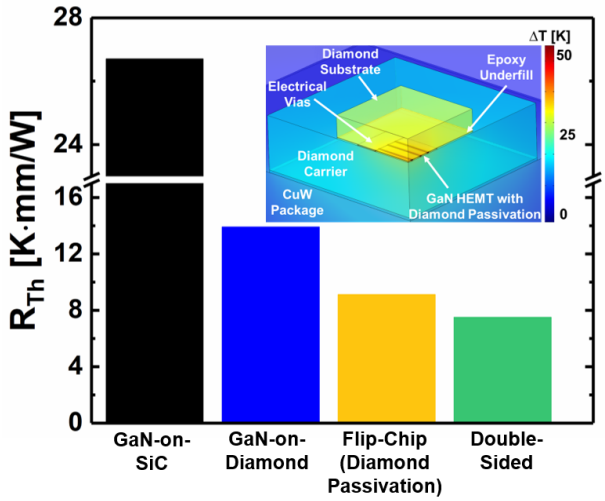

Fig. 7. GaN HEMT ultimate device-level cooling limit (double-sided cooling; Inset: operation under a power density of 5.5 W/mm).

bound" diamond passivation as outlined in Table II, the resulting R_{Th} value reduces to ~9.87 Kmm/W, a further 25% reduction. For the GaN-on-diamond case listed in Fig. 5 (and subsequent Figs. 6–9), the GaN/diamond effective TBR is assumed to be 21.9 m^2K/GW (from Table I; a value that is comparable with the current industry standard [67]) and the TC of the polycrystalline synthetic diamond substrate was adopted from [22] and [68].

One may speculate that ignoring any negative RF performance implications and adding a thermal bump between the drain electrode and diamond carrier wafer would result in a dramatic reduction in R_{Th}. However, the resulting R_{Th} reduction was found to be less than 0.4 Kmm/W (~5%) from the diamond passivation-incorporated flip-chip design. Simulations show that most of the heat generated in the 2DEG conducts through the diamond passivation, SCFP and the thermal bump above it, and toward the diamond carrier wafer. This is the preferred pathway for heat dissipation being that the SCFP overhangs the majority of the channel, while the drain electrode does not. Not including a thermal bump on the drain is the preferred design anyway considering the RF performance and ease of fabrication.

Fig. 6 shows the effect of improving the thermophysical properties of the diamond passivation layer. The "Lower bound" case corresponds to the "Diamond Passivation" case represented in Fig. 5. In this model, the 980-nm diamond passivation is used with the TC and TBR values listed in Table II under "Lower bound." By applying the previously derived upper bound TBR limit of 7.3 m^2K/GW (shown in Table II as the upper bound TBR) between the diamond passivation and the GaN, R_{Th} is reduced by 0.5%. Now, if the 980-nm diamond passivation is replaced with a 1960-nm passivation layer with improved TC values outlined in Table II as "Upper bound" while using the lower bound TBR of 24.3 m^2K/GW, R_{Th} is reduced by 3.8% from the "Lower bound" case. This case is represented in Fig. 6 as "Upper bound κ_r and κ_z/Lower bound TBR." Finally, by employing the upper bound diamond passivation, R_{Th} is reduced by 5.2% from the "Lower bound" case. It should be noted that for real fabricated/integrated structures, the heat sinking performance of the thermal bumps can be inferior to the model predictions. This is due to the imperfect interfaces between the gold bumps, initially applied to both the device and carrier wafer metallization structures, that are eventually joined together via the flip-chip process [66]. Therefore, it is of critical importance to employ diamond layers with best thermophysical properties achievable (e.g., larger lateral grain size and lower dielectric seed layer thickness), within the growth regime (i.e., limitation in the layer thickness and film stress [28]) that prevents degradation of the intrinsic 2DEG electrical performance.

To push the limits of GaN HEMT cooling, the thermally optimized flip-chip design [shown in Fig. 3 (c)] was applied to a GaN-on-diamond device, from here on denoted as the "double-sided" cooling design. By combining both the enhanced top- and bottom-side cooling methods, a thermal resistance of 8.42 Kmm/W was achieved. This value corresponds to a 68% reduction in R_{Th} compared with the conventional upright GaN-on-SiC baseline case and marks the ultimate limit for cooling the tested multifinger GaN HEMT that is achievable using diamond with state-of-the-art thermophysical standards ("upper bound" case in Table II). A comparison of this best-case scenario with the aforementioned baseline (GaN-on-SiC), GaN-on-diamond, and thermally optimized flip-chip cases can be found from Fig. 7.

V. Application to Ultra-Wide Bandgap Devices

The future of RF and power switching lies with the incorporation of UWBG semiconductors such as AlGaN [69]–[71] and β-Ga_2O_3 [72] into the device design. The enhanced critical breakdown fields of these materials give promise to the development of next frontier devices with unmatched improvement in system-level size, weight, and power (SWaP) and efficiency [31].

While these UWBG materials offer substantial advantages in terms of potentially achievable electrical performance, their poor TCs [39], [73], [74] lead to greatly intensified device

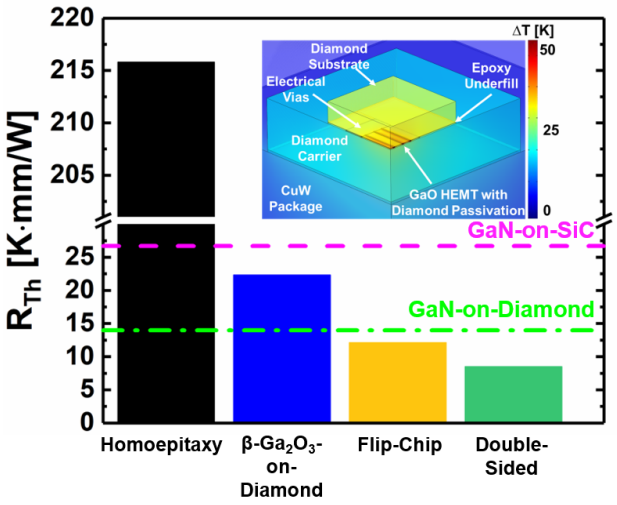

Fig. 8. β-Ga_2O_3 device thermal management. A homoepitaxy baseline case, β-Ga_2O_3-on-diamond, diamond-incorporated flip-chip design, and a double-sided cooling approach are compared (Inset: double-sided cooling case under a power density of 5.5 W/mm).

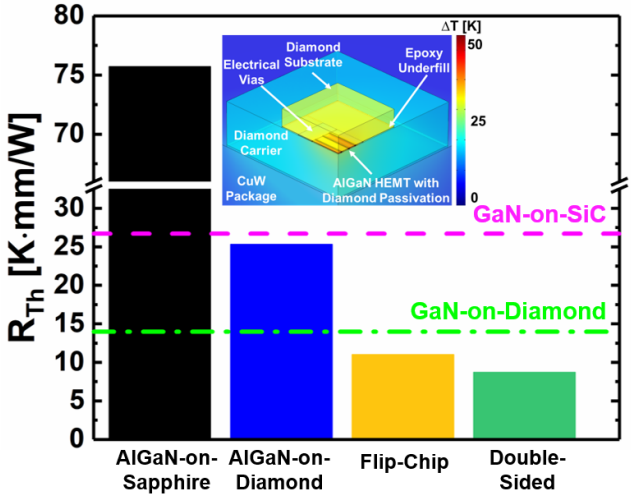

Fig. 9. AlGaN-channel HEMT device-level thermal management. A baseline case where the AlGaN-channel HEMT is fabricated on a sapphire substrate, AlGaN-channel HEMT-on-diamond, diamond-incorporated flip-chip design, and a double-sided cooling approach are compared (Inset: double-sided cooling case under a power density of 5.5 W/mm).

self-heating. For AlGaN-channel HEMTs grown on a sapphire substrate [35], [39] and a homoepitaxial β-Ga_2O_3 modulation-doped field-effect transistor (MODFET) [65], the combined low TCs of the substrate and channel materials greatly reduce the ability for heat to dissipate through the bottom side of the device. Therefore, top-side cooling solutions that allow efficient heat extraction from the device heat generation region are pivotal to the realization of practical UWBG devices. By implementing the flip-chip design augmented by thermal bumps and diamond passivation layers, similar to the designs in Fig. 3(c), simulation results show that it is possible, in principle, to reduce the device thermal resistance to a value even lower than that of the conventional GaN-on-diamond case examined in Figs. 4 and 5. For both cases, the substrate thickness was assumed to be 100 μm and the AlGaN channel/buffer thickness is $\sim$2 μm. It should be noted that the thickness of today's commercial β-Ga_2O_3 and sapphire substrates is on the order of 500–650 μm. Also, it was shown in [75] that for bottom-side substrate integration schemes, reducing the thickness of the low TC β-Ga_2O_3 (and AlGaN) layers is the key to achieve high heat transfer performance; yet this is less of a concern for the flip-chip design. Details of the AlGaN-channel HEMT and β-Ga_2O_3 MODFET modeling procedure (thermal properties) can be found in [39] and [65]. In this work, both devices were assumed to have identical device layouts as the GaN-on-SiC six-finger HEMT studied so far.

Fig. 8 shows the comparison of the cooling effectiveness of a six-finger Ga_2O_3 MODFET operated at a power density of 5.5 W/mm. The following four device configurations were studied: 1) homoepitaxy without additional thermal management; 2) integrating the β-Ga_2O_3 device with a diamond substrate; 3) flip-chipping a homoepitaxial device onto a diamond carrier while employing a diamond passivation layer; and 4) a β-Ga_2O_3-on-diamond MODFET using the diamond-incorporated flip-chip process (i.e., double-sided cooling). For the typical homoepitaxial configuration with no flip-chipping, the poor TC and thus lack of an effective route to dissipate heat lead to R_{Th} of $\sim$216 Kmm/W, which is an order of magnitude higher than that for a typical GaN-on-SiC HEMT. However, if a diamond substrate is introduced, heat dissipation is far more efficient, and the resulting R_{Th} is reduced to $\sim$22.5 Kmm/W. Furthermore, the implementation of the top-side flip-chip cooling method with diamond passivation and thermal bumps [similar to that shown in Fig. 3(c)] further improves R_{Th} to $\sim$12.1 Kmm/W. Finally, by applying the double-sided cooling method to the Ga_2O_3 device, it is possible to improve R_{Th} to $\sim$8.5 Kmm/W, which is lower than that of the GaN-on-diamond configuration.

Similarly, the effectiveness of the diamond substrate and flip-chip methods was studied for an AlGaN channel HEMT with Al concentrations of $x = 0.7$ and $x = 0.85$ for the channel and barrier layer, respectively, similar to the device described in [39] and [71]. For the baseline case [similar to Fig 3(a)] with the AlGaN-channel HEMT fabricated on a sapphire substrate, R_{Th} is about three times higher ($\sim$75.7 Kmm/W) than GaN-on-SiC HEMTs. By replacing the sapphire substrate with diamond, R_{Th} decreased to a level comparable with the GaN-on-SiC HEMT ($R_{Th} \sim 25.3$ Kmm/W). By applying the previously described diamond-incorporated flip-chip method (to an AlGaN-on-sapphire HEMT) as well as the double-sided cooling design, R_{Th} is further reduced to $\sim$11 and $\sim$8.7 Kmm/W, respectively. The diamond flip-chip cases again show that a thermal resistance lower than that of a GaN-on-diamond HEMT is possible to achieve.

VI. Conclusion

In this work, the cooling effectiveness by applying diamond as a substrate, passivation layer, and carrier wafer for various device configurations was evaluated for GaN and UWBG multifinger lateral transistor structures. Due to the decent TC of GaN and SiC, simply adopting a diamond passivation

layer does not result in a significant reduction in the thermal resistance of conventional upright-positioned GaN-on-SiC HEMTs. However, flip-chipping a diamond-passivated GaN HEMT onto a diamond carrier while implementing thermal bumps into the device design significantly reduces the device thermal resistance, below that for current state-of-the-art GaN-on-diamond HEMTs. In addition, this configuration can be applied to UWBG devices such as AlGaN-channel HEMTs and β-Ga_2O_3 MODFETs to reduce the thermal resistance of these devices within the range of current state-of-the-art GaN-on-diamond RF power amplifiers. By implementing the double-sided cooling method, the GaN-on-diamond benchmark can be surpassed for both AlGaN and β-Ga_2O_3 devices, leading to the lowest possible thermal resistances currently achievable for these UWBG devices. In conclusion, the diamond-incorporated flip-chip integration scheme locates the heat extraction mechanism in proximity to (less than several tens of nanometers) the heat source of lateral transistors (that take advantage of a high electron mobility 2DEG, which is essential to build a high-frequency RF power amplifier). Therefore, an outstanding cooling performance can be achieved, regardless of the TC of the device base material system.

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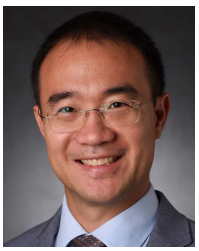

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