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ABSTRACT

Ultra-wide bandgap β-gallium oxide (Ga_2O_3) vertical device technologies are of significant interest in the context of the development of next-generation kV-range power switching devices. In this work, thermal analysis of vertical fin channel-based metal–oxide–semiconductor field-effect transistors (or fin field-effect transistors—FinFETs) was performed using infrared thermal microscopy and coupled electro-thermal modeling. FinFETs with different fin width and channel spacing were characterized to study the thermal design trade-off when attempting to minimize the footprint of multi-fin FinFET arrays. A 50×50 μm^2 scaled FinFET cell array exhibited an $\sim 23\times$ higher temperature rise as compared to a 5-fin device. Devices with different orientations were fabricated and characterized. By rotating the fin channel aligned along the [010] direction by 90°, the channel temperature rise reduced by 30%, due to the anisotropy of the Ga_2O_3 thermal conductivity (κ). Electro-thermal modeling shows that a 20% reduction in the temperature rise is possible by fabricating devices on a (010)-oriented substrate as compared to the tested devices built on a (001) substrate. These results indicate the importance of the electro-thermal co-design process for Ga_2O_3 vertical FinFET cell arrays.

In recent years, β-phase gallium oxide (Ga_2O_3) has emerged as a primary candidate to enable next-generation power electronic devices. The ultra-wide bandgap (4.6–4.9 eV)[1,2] of Ga_2O_3 translates into a large critical electric field (~8 MV/cm) that is more than 2× higher than that of wide bandgap materials GaN and SiC.[3] The potential performance gain by using Ga_2O_3 in power switching applications is apparent from its Baliga's figure of merit (BFOM), which is higher than those of Si (3000×), SiC (10×), and GaN (4×).[4] An advantage of Ga_2O_3 over other ultra-wide bandgap ($Al_xGa_{1-x}N$, diamond, etc.) and wide bandgap semiconductors (GaN, SiC) is that high-quality melt-grown substrates are commercially available.[5–8] However, one major roadblock toward the maturation of the Ga_2O_3 technology is device overheating, which is caused by the low anisotropic thermal conductivity (κ) of the material (11–27 W/m K at 300 K).[9] The emerging device technology will not be able to achieve the superior electrical performance suggested by the BFOM, unless this thermal challenge is overcome by using electro-thermal co-design techniques (i.e., by optimizing the device-layout design and employing thermal management solutions).[10–13]

While significant advancements have been made in the development of Ga_2O_3 lateral devices [e.g., modulation doped $(Al_xGa_{1-x})_2O_3$/Ga_2O_3 heterostructures[14]], vertical devices are preferred for high power and high voltage applications. The vertical configuration allows for scaling the breakdown voltage by controlling the drift layer thickness without increasing the device footprint. Therefore, a higher current level can be achieved than lateral devices for a same chip area. In addition, the device characteristics are less impacted by the surface states. In 2016, a Ga_2O_3 current aperture vertical electron transistor (CAVET) was demonstrated.[15] Early stage development of vertical metal-oxide-semiconductor field-effect transistors (MOSFETs) and FinFETs exhibiting relatively low breakdown voltages often without pinch-off characteristics has also been reported.[16,17] Recently, Hu *et al.*[18] demonstrated kV-range vertical Ga_2O_3 transistors with normally off (E-mode) operation.[19] Among the vertical device architectures, the FinFET configuration provides several benefits, including stronger gate electrostatic control (by double-gating) and minimized resistance between the gate and source electrodes. The relatively low current density of individual devices can be overcome by the design of

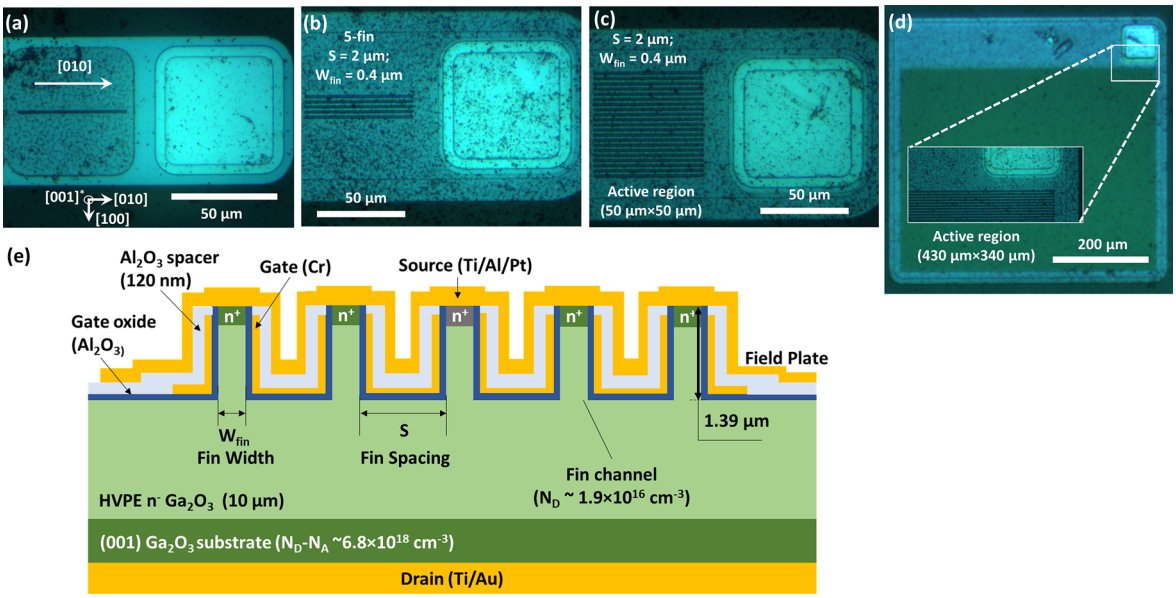

FIG. 1. (a) A single-fin FinFET with a fin width (W_{fin}) of 0.4 μm and fin length of 50 μm. (b) A 5-fin FinFET with W_{fin} of.4 μm and a fin spacing (S) of 2 μm. (c) A 50 × 50 μm^2 multi-fin transistor with $W_{fin} = 0.4$ μm and S = 2 μm. (d) A 430 × 340 μm^2 multi-fin transistor with $W_{fin} = 0.03$ μm and S = 2 μm. (e) The epitaxial structure of a multi-fin Ga_2O_3 FinFET.

multi-fin FinFETs and the use of post-deposition annealing that improves the channel mobility.[20] However, the thermal consequences of scaling multi-fin devices have not been experimentally studied. In this work, the self-heating behavior of FinFETs with different number of fins, fin design parameters, and device orientations was investigated. Optical thermography and electro-thermal device modeling were performed to study the impact of various design variables, including the chip area utilization (i.e., number of fins) and device/substrate orientation on the electrical and thermal performance.

An optical image of a single-fin transistor with a fin width (W_{fin}) of 0.4 μm is shown in Fig. 1(a). Figures 1(b) and 1(c) show a 5-fin device and a scaled multi-fin device with active area of 50 × 50 μm^2, respectively. A larger scaled device with an active area of 430 × 340 μm^2, $W_{fin} = 0.3$ μm and a fin spacing (S) of 2 μm is shown in Fig. 1(d). The FinFETs were fabricated on a (001)-oriented n^+ Ga_2O_3 substrate with a 10 μm n-Ga_2O_3 drift layer grown by halide vapor phase epitaxy [Fig. 1(e)]. For the devices shown here, the default fin length is along the [010] crystallographic direction, while the fin width is along the [100] direction. These lead to a [001]-like direction along the trench height (denoted henceforth as [001]*), i.e., (100)-like trench sidewalls. The scaled multi-fin devices were fabricated by repeating the intermediate fin and trench structure. Details of the fabrication process can be found elsewhere.[17,18,20,21] The various types of devices studied in this work are summarized in Table I. For the 50 × 50 μm^2 multi-fin devices, including that shown in Fig. 1(c), the number of fins was varied based on W_{fin} and S while the active area remains constant.

Current–voltage (I–V) characteristics of various single-fin devices are shown in Fig. 2(a) for W_{fin} of 0.3 and 0.4 μm. The current is normalized with respect to the n^+ doping area (W_{fin} × 50 μm^2). With an increase in W_{fin}, the resistance to the current flow from drain to source reduces, leading to a higher current. However, as seen in Fig. 2(a), the calculated current density reduces with increased W_{fin} due to the normalization scheme used.[20] With an increase in W_{fin}, the threshold voltage (V_{th}) shifts to the left as shown in Fig. 2(b). Figure 2(c) shows the I–V characteristics of a 5-fin FET with $W_{fin} = 0.3$ μm and S = 3 μm obtained from measurements and coupled the electro-thermal simulations.

The surface temperature of the single- and multi-fin FinFETs was measured using a Quantum Focus medium wavelength infrared radiation (MWIR) Infrascope, which has also been used in our previous work on GaN p-i-n diodes and Ga_2O_3 Schottky barrier diodes.[22,23] A 15× objective was used for thermal imaging, and a pixel-by-pixel emissivity correction algorithm was used to increase the accuracy of the measurement. The diffraction limited spatial resolution was ~2.8 μm. The typical size of a measured fin was ~50 × 1.5 μm^2. IR measurements were taken at a base temperature of 50 °C. The emissivity of the fin surface of a typical 5-fin device was ~0.301 ± 0.0034, which is sufficient for quantitative thermal imaging.[19] Further details of the emissivity measurement can be found in the supplemental information. Figure 3(a) shows an IR thermal image of a 5-fin FinFET with

TABLE I. List of FinFET device types and the corresponding design parameters varied in this study.

Device type	W_{fin} variation (μm)	S variation (μm)
Single-fin	0.2;0.3;0.4	N.A.
5-fin	0.3;0.4	1.2;2.0; 3.0;5.0
Multi-fin (50 × 50 μm^2)	0.3;0.4	1.2;2.0;3.0;5.0
Multi-fin (430 × 340 μm^2)	0.3	2.0

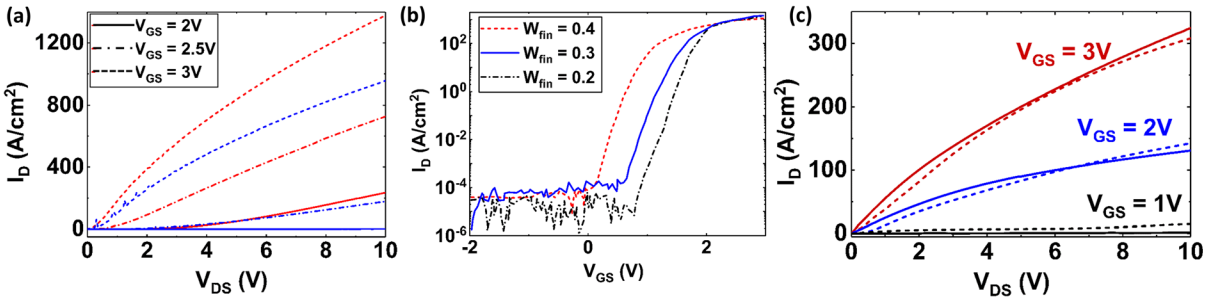

FIG. 2. (a) Electrical output characteristics of a single-fin FinFET with W_{fin} of 0.3 μm (red lines) and 0.4 μm (blue lines). (b) Transfer characteristics of single-fin devices with W_{fin} = 0.2, 0.3, and 0.4 μm, for V_{DS} = 10 V. (c) Output characteristics of 5-fin devices (W_{fin} = 0.3 μm; S = 3 μm) obtained from measurement and simulation results. Solid lines are from measurements and dashed lines represent simulation results. Current density is calculated by normalizing to the n^+ source area.[20]

W_{fin} = 0.4 μm and S = 3 μm [similar to the device structure in Fig. 1(b)] under V_{GS} = 3 V and a power dissipation level of 50 mW, which corresponds to an aerial power density of 7.1 kW/cm^2 (normalized with respect to the total area of the active region).

An electro-thermal FinFET model was constructed that couples a 2D technology computer aided design (TCAD) electrical model (Synopsys Sentaurus) with a 3D finite element thermal model (COMSOL Multiphysics). The motivation behind the coupled model lies in the importance of accurately capturing both the electronic transport processes that dictate the Joule heat generated in the devices, and the thermal transport processes across/through the 3D device structure that determines the internal temperature distribution. Details of this multi-physics modeling scheme can be found in our previous work.[13,24,25] In the electrical model, temperature dependent electronic properties available in the literature (electron mobility, bandgap energy, etc.)[20,26–28] were used as modeling inputs. The Al_2O_3/Ga_2O_3 interface trap density was adjusted to calibrate the simulated I-V characteristics. Temperature dependent thermal properties from the literature were used in the 3D thermal model.[9,29–31] Further details of the electro-thermal model and the coupling method can be found in the supplementary material.

Electrical output characteristics obtained from the coupled electro-thermal simulation and experiments are in close agreement, as shown in Fig. 2(c). The Joule heat distribution in a 5-fin FinFET (W_{fin} = 0.3 μm and S = 2 μm) under a power density condition of 10.5 kW/cm^2 and V_{GS} = 3 V calculated by the electro-thermal model

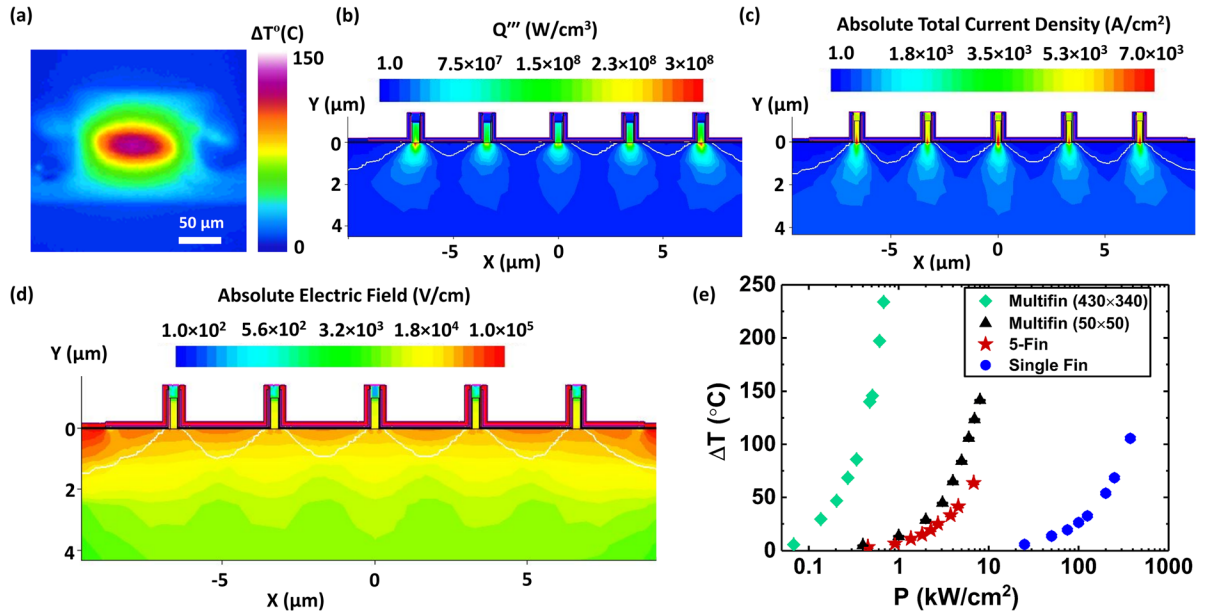

FIG. 3. (a) Top-view infrared (IR) thermal image of a 5-fin device (W_{fin} = 0.4 μm; S = 3 μm). (b) Joule heat distribution of a 5-fin device obtained from electro-thermal simulation. (c) Current density distribution in the 5-fin FinFET. (d) Electric field distribution across the 5-fin FinFET. All simulation results shown here were performed under P = 50 mW, V_{GS} = 3V, with W_{fin} = 0.3 μm and S = 3 μm. (e) The surface temperature rise of single-fin (W_{fin} = 0.4 μm), 5-fin (W_{fin} = 0.4 μm; S = 5 μm), and multi-fin devices with 50 × 50 μm^2 (W_{fin} = 0.4 μm; S = 5 μm) and 430 × 342 μm^2 (W_{fin} = 0.3 μm; S = 2 μm) device area, obtained from IR thermography. The power density for the single and 5-fin devices was calculated by normalizing the power with respect to the n^+ source area. For the multi-fin devices, a total area of 430 × 340 and 50 × 50 μm^2 was used.

is shown in Fig. 3(b). The generated heat was observed to be concentrated near the bottom of the fin channels. The spatial distribution of $Q'''(x,y)$ is determined by the distributions of the current density [Fig. 3(c)] and the electric field within the device active region [Fig. 3(d)].

Converting the current density (Fig. 2) into total current, the current flowing through devices with W_{fin} increases by ~14× when they are converted from a single-fin to a 5-fin device with $S = 3\ \mu m$, and by 37× for a $50 \times 50\ \mu m^2$ scaled device. However, the increase in current comes at the expense of a substantially increased thermal load. For example, Fig. 3(e) compares the IR-measured peak temperature rise (ΔT) of single-fin device, 5-fin device, and multi-fin devices with active areas of 50×50 and $430 \times 342\ \mu m^2$ for varying power dissipation levels. It is to be noted that ΔT measured by IR thermography may underestimate the true peak temperature of the devices due to the limited spatial resolution of the technique. However, the 3D electro-thermal model can be used to confirm the average surface temperature measured by IR and predict the device peak temperature rise. For the large-area scaled devices, the ΔT is ~2× for the $50 \times 50\ \mu m^2$ active area device as compared to the 5-fin FinFET (active area of $\sim 1100\ \mu m^2$). For scaled devices with an active area of $430 \times 342\ \mu m^2$, the ΔT is ~40× as compared to the 5-fin FinFET. This aggravated self-heating effect is caused by the thermal crosstalk among adjacent fins, which impedes the heat flow away from the center of the device, owing to adiabatic boundary conditions forming at the planes of symmetry between the fins. This undesired effect significantly increases the peak temperature of multi-fin devices over single-fin devices under identical power density conditions.

Effects of fin design variables (W_{fin} and S) on the device electrical performance have been discussed in our prior work.[20] While increasing W_{fin} and S reduces the device on-resistance (R_{on}), a larger fin area ratio (W_{fin}/S) results in a lower specific on-resistance ($R_{on\text{-}sp}$).[20] From a thermal perspective (Fig. 4), increasing S and W_{fin} should reduce ΔT. Figures 4(a) and 4(b) show IR thermography images for 5-fin devices ($W_{fin} = 0.4\ \mu m$) with S of 1.2 (hotter) and 5 μm (colder) for a power dissipation level of 50 mW, under $V_{GS} = 3$ V. Figures 4(c) and 4(d) show IR thermography images for scaled devices with an active area of $50 \times 50\ \mu m^2$ ($W_{fin} = 0.4\ \mu m$) with S of 1.2 and 5 μm. Figure 4(e) summarizes the measured ΔT obtained from infrared thermal imaging for 5-fin devices. By increasing S from 1.2 to 5 μm, the device thermal resistance (R_{th}) of FinFETs with $W_{fin} = 0.3$ and 0.4 μm reduces by ~26% and 16%, respectively. For scaled devices with an active area of $50 \times 50\ \mu m^2$, the effect of S (i.e., decrease in ΔT with an increase in S) saturates faster than the 5-fin device case. For example, for the case of $W_{fin} = 0.3\ \mu m$, there is 17% reduction in ΔT for a 5-fin device as the fin spacing increases from 2 to 5 μm, whereas for the $50 \times 50\ \mu m^2$ area device, the corresponding reduction in temperature is only ~3%. The 3D coupled electro-thermal model was used to calculate the ΔT of 5-fin devices with intermediate values of S. As shown in Fig. 4(e), for the 5-fin FinFETs, the effect of increasing S diminishes rapidly for $S \geq 4\ \mu m$, which corroborates with the experimental data discussed above.

Due to the strong anisotropy associated with a monoclinic crystal structure,[9] the κ of β-phase Ga_2O_3 can vary from ~10.9 W/m K in the [100] direction to ~27 W/m K in the [010] direction under 300 K temperature conditions.[13] Consequently, the thermal performance of any

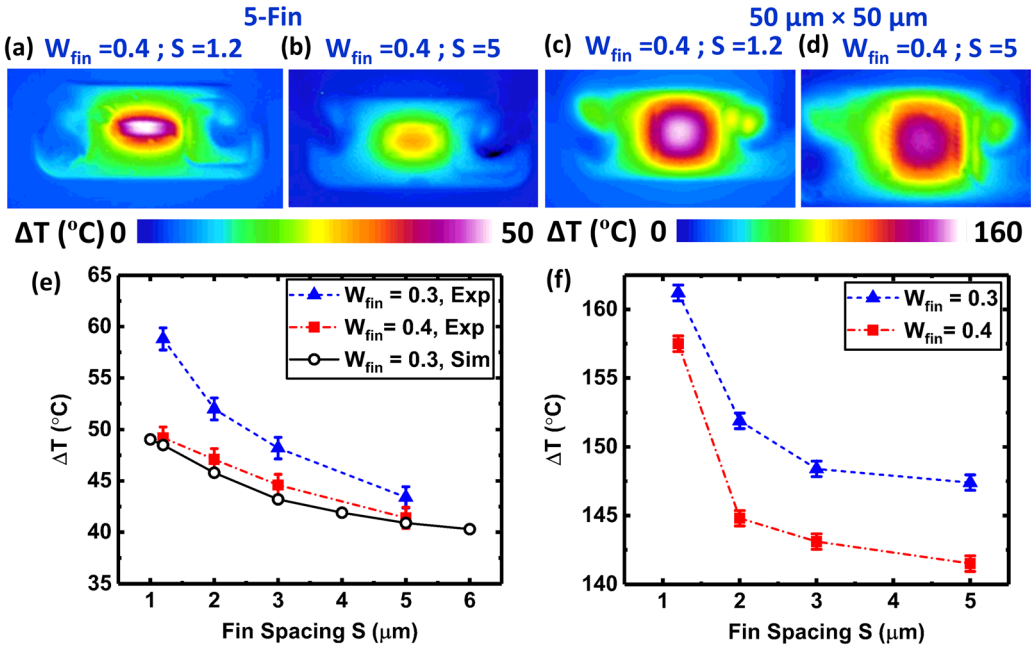

FIG. 4. Infrared (IR) thermal image of (a) 5-fin device with $W_{fin} = 0.4\ \mu m$, $S = 1.2\ \mu m$; (b) 5-fin device with $W_{fin} = 0.4\ \mu m$, $S = 5.0\ \mu m$; (c) $50 \times 50\ \mu m^2$ area device with $W_{fin} = 0.4\ \mu m$, $S = 1.2\ \mu m$ and (d) $50 \times 50\ \mu m$ area device with $W_{fin} = 0.4\ \mu m$, $S = 5.0\ \mu m$. (e) Effect of fin spacing ($S = 1.2$, 2.0, 3.0, and 5.0 μm) and fin width ($W_{fin} = 0.3$ and 0.4 μm) on device ΔT from IR thermal imaging 5-fin FinFETs. Spatially averaged temperature rise determined from 3D electro-thermal simulation is also shown in the figure. (f) Variation of ΔT for a $50 \times 50\ \mu m^2$ area devices with $S = 1.2$, 2.0, 3.0, and 5.0 μm and $W_{fin} = 0.3$ and 0.4 μm, acquired by IR thermal imaging. All results shown here were obtained at the power dissipation level of 50 mW and $V_{GS} = 3$ V.

Ga_2O_3 based electronic device is affected by the substrate orientation. The impact of crystal orientation on the heat dissipation and maximum forward current in Ga_2O_3 vertical rectifiers has been recently reported by Xian *et al.*[32] To study the effect of the anisotropic κ and the orientation of the device layout on the FinFET thermal performance, single-fin devices were fabricated where the fin channels were rotated at different angles with respect to the baseline configuration. Figure 5(a) shows exemplar devices, and they were characterized using IR thermography [Fig. 5(b)]. Here, θ denotes the angle between the direction along the fin channel length and [010] [Figs. 1(e) and 5(a)]. ΔT obtained from IR thermography for all the measured devices is summarized in Fig. 5(c). ΔT in the FinFET devices was measured to be the lowest for the orientation with $\theta = 90°$. There was a 30% reduction in ΔT for the design with $\theta = 90°$ as compared to the baseline design of $\theta = 0°$. This is because for $\theta = 90°$, the fin width is along the [010] direction [$\kappa(300\,K) = 27$ W/m K], thereby facilitating efficient heat transfer from the fin channels because of its higher κ as compared to the [100] orientation of the baseline case ($\theta = 0°$) [$\kappa(300\,K) = 10.9$ W/m K].[13] However, the change in the fin alignment impacts both V_{th} and the saturated drain current (^{I}D,Sat), as shown in our previous work.[20] For the $\theta = 90°$ design, the V_{th} was observed to be the highest and $I_{D,Sat}$ was lowest among the tested devices with different fin orientation. The lowest V_{th} and highest $I_{D,Sat}$ were observed for the device with $\theta = 0°$.

Finally, the overall R_{th} of the device can be reduced by employing a substrate with a higher cross-plane κ.[13] The electro-thermal model was used to compare the ΔT of the tested devices employing a (001)-oriented substrate as well as hypothetical devices fabricated on a (010)-oriented substrate. The ΔT measured via IR thermography and those predicted by the electro-thermal model show excellent agreement as shown in Fig. 5(d). This model was then used to predict the effect of substrate orientation on 5-fin FETs with various S values, as shown in the blue curve of Fig. 5(d). It should be noted that for all case studies involving different S, the R_{th} of devices fabricated on a (010) substrate was lower than that for devices fabricated on a (001) substrate by 19% (for $W_{fin} = 0.3\,\mu m$) and 25% (for $W_{fin} = 0.4\,\mu m$, shown in the supplementary material).

An experimental study was performed on homoepitaxial Ga_2O_3 FinFETs fabricated on a (001)-oriented substrate to identify key design parameters that impact the device thermal performance. For single-fin devices, increasing the fin width (W_{fin}) reduces the device R_{on}, which in turn negatively shifts the V_{th} and reduces the temperature rise (ΔT). While increasing the fin spacing (S) increases the device $R_{on\text{-}sp}$ and footprint, it reduces the ΔT. For the 5-fin and the scaled multi-fin devices, it was found that increasing S results in a remarkable reduction in ΔT (up to $S = 3\,\mu m$). As FinFETs are expanded to larger area scaled devices (50×50, $430 \times 340\,\mu m^2$), ΔT can increase by $\sim 2\times$ and $\sim 40\times$, respectively, as compared to 5-fin devices operating at an identical areal power density. To understand the effect of the anisotropic κ of Ga_2O_3 on the self-heating behavior of FinFETs, devices with different fin channel orientations were fabricated and characterized via IR thermography. It was observed that for an orientation where the fin channel is rotated by 90° with respect to a baseline configuration (where the fin channel is oriented along the [010] orientation), the ΔT reduces by ~30%. 3D electro-thermal simulation also showed that the device R_{th} can be reduced by ~20% if FinFETs are fabricated on a

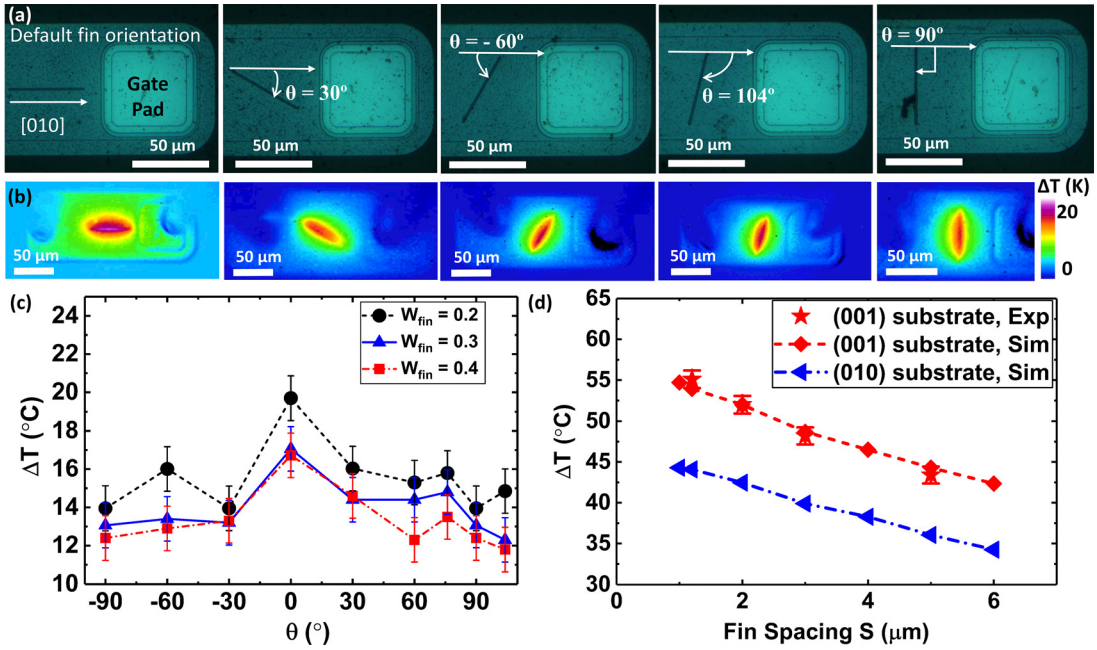

FIG. 5. (a) Plan-view optical image of single-fin devices with $\theta = 0°$, $\theta = 30°$, $\theta = -60°$, and $\theta = 90°$. (b) IR thermal image of each of these devices cooperating under a power dissipation level of 50 mW, $V_{GS} = 5$ V. (c) Summary of the effect of device orientation for single-fin FETs for various W_{fin} FinFETs on a 001-oriented substrate. IR measurements were done under a power dissipation level of 50 mW and $V_{GS} = 5$ V. (d) Effect of substrate orientation on device ΔT demonstrated by electro-thermal modeling of 5-fin FinFETs, with varying S, for $W_{fin} = 0.3\,\mu m$ and a fin orientation of $\theta = 0°$. All simulations were performed at a power dissipation level of 50 mW for $V_{GS} = 3$ V. IR thermography results are shown for the baseline configuration of the (001) substrate.

(010)-oriented Ga_2O_3 substrate instead of a (001) substrate on which test structures were built. Along with the thermally aware device layout design, device-level thermal management solutions will be necessary to further reduce R_{th} to a manageable level. For vertically configured devices, top-side cooling solutions, such as flip-chip integration on a high thermal conductivity carrier wafer, will be preferred over bottom-side heat extraction methods, such as integration with a high κ substrate.[10,11,13,33,34]

See the supplementary material for more detailed discussions on the electro-thermal modeling, infrared thermography experiments, and the substrate orientation effect on the device self-heating for $W_{fin} = 0.4\ \mu m$.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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