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ABSTRACT

In this report, the thermal performance of a hydrogen (H)-terminated diamond field-effect transistor (FET) is investigated using Raman spectroscopy and electrothermal device modeling. First, the thermal conductivity ($\kappa_{diamond}$) of the active diamond channel was determined by measuring the temperature rise of transmission line measurement structures under various heat flux conditions using nanoparticle-assisted Raman thermometry. Using this approach, $\kappa_{diamond}$ was estimated to be 1860 W/m K with a 95% confidence interval ranging from 1610 to 2120 W/m K. In conjunction with measured electrical output characteristics, this κ was used as an input parameter for an electrothermal device model of an H-terminated diamond FET. The simulated thermal response showed good agreement with surface temperature measurements acquired using nanoparticle-assisted Raman thermometry. These diamond-based structures were highly efficient at dissipating heat from the active device channel with measured device thermal resistances as low as ~1 mm K/W. Using the calibrated electrothermal device model, the diamond FET was able to operate at a very high power density of 40 W/mm with a simulated temperature rise of ~33 K. Finally, the thermal resistance of these lateral diamond FETs was compared to lateral transistor structures based on other ultrawide bandgap materials ($Al_{0.70}Ga_{0.30}N$, β-Ga_2O_3) and wide bandgap GaN for benchmarking. These results indicate that the thermal resistance of diamond-based lateral transistors can be up to ~10× lower than GaN-based devices and ~50× lower than other UWBG devices.

With increasing demands for high power and high frequency applications, conventional semiconductors (Si, GaAs) are being replaced by wide bandgap (WBG) semiconductors (SiC, GaN). As the theoretical performance limits of these WBG semiconductors are being reached, researchers are actively investigating ultrawide bandgap (UWBG) semiconductors with a bandgap energy (E_G) higher than 4 eV. Currently, the UWBG semiconductors of greatest interest are $Al_xGa_{1-x}N$, β-Ga_2O_3, and diamond. The ultrawide bandgap of these materials makes them promising candidates for radio frequency (RF) applications because of their high breakdown field strength. The Johnson figure of merit (JFOM) can be used to assess these UWBG material systems for high power RF applications,[1]

$$JFOM = V_B f_T = \frac{E_c v_{sat}}{2\pi}, \quad (1)$$

where V_B is breakdown voltage, f_T is cutoff frequency, E_c is critical electric field, and v_{sat} is the carrier saturation velocity. In the supplementary material, Table I, the JFOM and related material properties for conventional, WBG, and UWBG semiconductors (diamond,[2–4] $Al_{0.70}Ga_{0.30}N$,[5–9] β-Ga_2O_3[10–13]) are given and normalized with respect to Si. The JFOM increases from conventional to UWBG semiconductors, and among the UWBG semiconductors, the JFOM is relatively similar.

While the JFOM is useful for identifying promising materials for high frequency applications from an electrical standpoint, it does not provide any indication regarding the potential thermal performance of the material. The higher power operation required of UWBG-based microelectronics increases the demand for efficient dissipation of heat from the active region as increased temperatures degrade performance and reliability.[14] By incorporating the thermal conductivity (κ) of the material system, the Keyes figure of merit

(KFOM) captures the potential high frequency performance from a thermal point of view,[15]

$$KFOM = \kappa\sqrt{\frac{cv_{sat}}{4\pi\epsilon}}, \quad (2)$$

where c is the speed of light and ϵ is the relative permittivity of the material. When thermal performance is also considered, diamond excels among all materials,[16] especially when KFOM is compared to that of other UWBG semiconductors (supplementary material, Table I). The RF output power of commercial GaN devices is derated to prevent thermal failure, which negates the potential of the technology to reach its theoretical maximum power density.[17] Furthermore, the thermal conductivities of both $Al_xGa_{1-x}N$ and β-Ga_2O_3 are orders of magnitude lower than that of GaN. Therefore, one of the largest roadblocks for realizing the full potential of these UWBG material systems ($Al_xGa_{1-x}N$, β-Ga_2O_3) is poor thermal performance.[14] The ultrahigh thermal conductivity of diamond offers a solution to this thermal obstacle. While low thermal resistance is to be expected of diamond-based electronics, there has yet to be any quantitative experimental reports on the thermal performance of diamond transistors. This is because device fabrication has been a challenge due to the difficulty working with diamond. For example, n-type doping of diamond has remained elusive and p-type doping is typically realized through surface transfer doping as opposed to traditional substitutional doping. Surface transfer doping was originally accomplished using atmospheric adsorbates;[18] however, this method results in very unstable device performance. Recent studies employing high electron affinity capping layers have improved both the surface transfer doping and the stability of the device performance.[19] Accordingly, it is now possible to study the thermal performance of diamond-based device technologies.

In this report, the thermal performance of lateral H-terminated diamond field-effect transistors (FETs) is investigated using Raman thermometry and electrothermal device modeling. Transmission line measurement (TLM) structures are utilized to estimate the thermal conductivity of the chemical vapor deposition (CVD)-grown single crystal diamond substrate. Subsequently, the estimated diamond thermal conductivity and measured electrical characteristics are used to create a coupled electrothermal device model of the H-terminated diamond FETs. The simulated thermal response of the diamond FET is then validated by the temperature rise measured experimentally via nanoparticle-assisted Raman thermometry. The model was used to estimate the channel temperature rise of diamond FETs under high power density conditions (up to 40 W/mm). Finally, the experimentally measured thermal performance of a lateral diamond FET is compared with lateral transistor structures based on UWBG $Al_{0.70}Ga_{0.30}N$ and β-Ga_2O_3 materials. In addition, the thermal performance of these three UWBG semiconductors is benchmarked against a GaN-based lateral transistor structure.

H-terminated diamond FETs[19,20] [Fig. 1(a)] were fabricated at the Army Research Laboratory on a 500 μm thick commercial CVD-grown single crystal diamond substrate. Between metal contacts on the H-terminated diamond surface, a 40 nm thick film of V_2O_5 was deposited to provide surface transfer doping.[16,21,22] Subsequently, a 50 nm thick film of SiO_2 was deposited via e-beam evaporation to help to hermetically seal V_2O_5 from atmospheric degradation.[23] The Ohmic contacts are Au, and the Schottky gate contact is Al. An ultrathin (~2 nm) Al_2O_3 layer possibly results at the Al-diamond interface

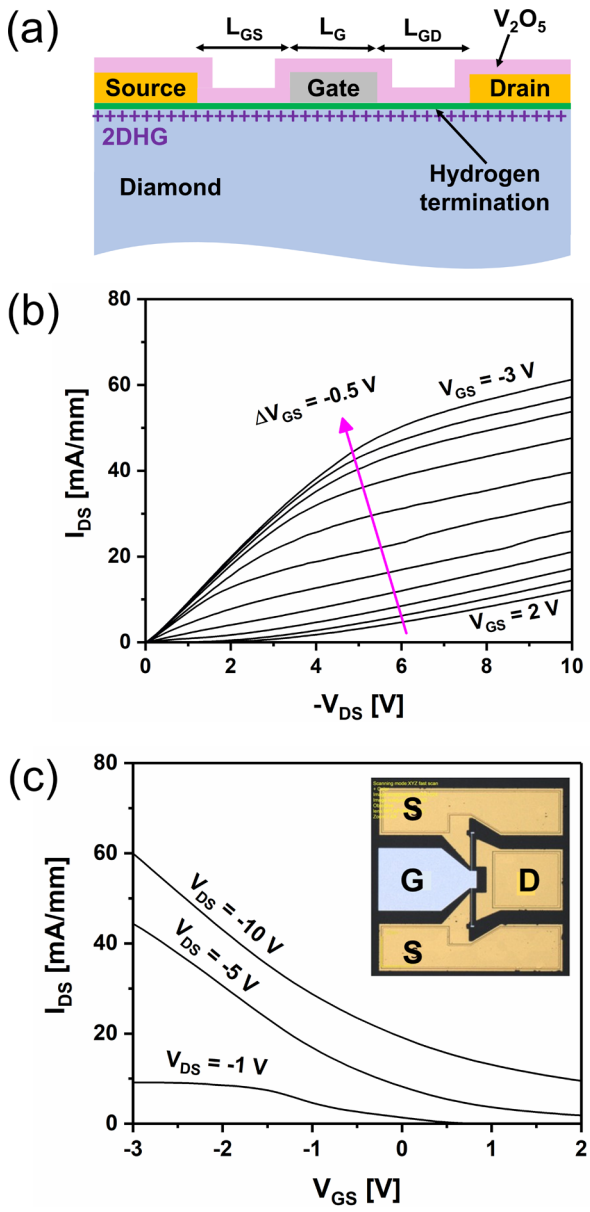

FIG. 1. (a) Cross-sectional schematic of the H-terminated diamond FET. (b) Output and (c) transfer characteristics of a diamond FET. The inset of (c) shows a photomicrograph of the diamond FET.

underneath the gate contact.[24] For all devices tested, the designed channel width (W_{ch}) was 50 μm [25 μm for each finger, inset of Fig. 1(c)], the source-gate spacing (L_{GS}) was 1 μm, the gate length (L_G) was 50 nm, and the drain-gate spacing (L_{GD}) was either 1 or 3 μm. A top-view photomicrograph and cross-sectional schematic of the H-terminated diamond FETs are shown in Fig. 1 along with measured output [Fig. 1(b)] and transfer [Fig. 1(c)] characteristics ($W_{ch} = 22.5$ μm; $L_G = 50$ nm; $L_{GD} = L_{GS} = 1$ μm).

Nanoparticle-assisted Raman thermometry[25–28] was used to measure the surface temperature rise in the active channel region for

both TLM and transistor structures. Using this technique, anatase TiO_2 nanoparticles (99.98% purity) are first deposited onto the surface of the device. During device operation, Raman spectroscopy is used to measure the peak shift of the E_g mode of the TiO_2 nanoparticles due to an increase in temperature. Since the nanoparticle is free-standing on the device surface, it is assumed that the nanoparticle undergoes stress-free thermal expansion. Therefore, while both temperature and stress typically affect the Raman peak position, it is assumed in this case that stress effects are negligible and the measured peak shift is only temperature dependent. TiO_2 nanoparticles were selected for nanoparticle-assisted Raman thermometry due to a high signal-to-noise ratio and good temperature sensitivity of the E_g mode in the Raman spectra.[25] Raman spectroscopy (532 nm) was performed using a Horiba LabRAM HR Evolution spectrometer in a 180° backscattering configuration [$Z(XX)\bar{Z}$] with an 1800 g/mm grating and a 50× long working distance objective (NA = 0.50). The spatial resolution of the measurement was defined by the size of the nanoparticle agglomerates measured (~1 μm). Typically, the best achievable temperature resolution possible using Raman thermometry is approximately ± 1 K;[29] however, this is for small temperature rises. As the measured temperature rise increases, the uncertainty in the measurement can increase up to approximately ± 10 K.[30] A low laser power of ~0.5 mW was used to avoid laser heating of the TiO_2 nanoparticles during thermal measurements. In order to correct for systematic errors, a reference mercury emission line (~546 nm) was monitored during all measurements.

A fully coupled electrothermal device model[31] of the H-terminated diamond FETs was constructed to estimate the device temperature rise under high power density conditions. First, a 2D technology computer aided design (TCAD) model of the diamond FET is built using Synopsys Sentaurus. Briefly, this model solves for the Poisson's and drift diffusion equations to reproduce the device current–voltage characteristics and accurately predict the heat generation distribution in the diamond FET as a function of bias. The heat flux distribution is extracted from the results of the 2D TCAD model, which is extended along the device channel width. This 3D heat flux profile is imported into a 3D COMSOL model, and the device internal temperature field is determined by solving the heat diffusion equation. More details of the 2D TCAD modeling and 2D–3D coupling processes can be found in our previous work on a H-terminated diamond FET,[32] β-Ga_2O_3 modulation-doped FET (MODFET),[33] and GaN high electron mobility transistor (HEMT).[34] As described and investigated in several reports,[16,22,35,36] hydrogen termination of the diamond surface results in surface transfer doping and a resultant two-dimensional hole gas (2DHG) within a few nanometers of the diamond surface. The formation of the 2DHG is a result of the negative electron affinity (NEA) at the diamond surface, which results in emission of electrons from diamond to the surface acceptor. To create the 2DHG in the device model, an electron affinity of –1.3 eV was used at the diamond surface. Device electrical properties, including sheet resistivity (R_S), contact resistivity (R_C), carrier density (n), and Hall mobility (μ_{Hall}), were determined via TLM and Hall measurements and used to calibrate the device model. Respectively, these electrical properties were measured to be $R_S = 7.5\ k\Omega/sq$, $R_C = 1\ \Omega\,mm$, $n = 2 \times 10^{13}\ cm^{-2}$, and $\mu_{Hall} = 150\ cm^2/V\,s$. Using nanoparticle-assisted Raman thermometry and device modeling, the thermal conductivity of the diamond substrate was estimated to be 1860 W/m K with a 95% confidence interval ranging from 1610 to 2120 W/m K. Details on the determination of this thermal conductivity will be discussed subsequently. The temperature dependence of the thermal conductivity of diamond was incorporated into the device model by exponential fitting of the experimental data reported by Inyushkin *et al.*[37] The temperature dependence of the diamond thermal conductivity (κ) used is given by the exponential function

$$\kappa = Ae^{-\alpha(T-T_0)}, \tag{3}$$

where T is temperature in units of K, T_0 is 298 K, and A and α are constants equal to 1860 W/m K and $4.25 \times 10^{-3}\ K^{-1}$, respectively.

The thermal conductivity of diamond reported in literature ranges from 1000 to 3000 W/m K.[38–40] These reported values vary based on the isotopic purity, impurity concentration, and crystal quality of the diamond samples studied. To increase the accuracy of the electrothermal device model in this study, the thermal conductivity of the CVD-grown diamond substrate ($\kappa_{diamond}$) was estimated after device fabrication by repurposing TLM structures. Since TLM gaps essentially function as resistors, the power dissipated in the diamond channel during biasing can be modeled as a constant heat flux. This allows the TLM structure to be used as an electrical pump while the Raman laser is used as an optical probe to measure the temperature rise of the TiO_2 nanoparticle on the device surface [Fig. 2(a)]. While both the Ohmic contact resistance (R_C) and the semiconductor channel resistance (R_{ch}) contribute to the total resistance of the TLM structure, R_{ch} is much greater than R_C.[41] Accordingly, power dissipation due to the Ohmic contacts is assumed to be negligible and all device power dissipation is assumed to occur in the diamond channel when performing thermal modeling for estimation of the thermal conductivity.

$\kappa_{diamond}$ can be determined using (i) an analytical model for thermal spreading resistance in a rectangular heat flux channel[42–44] or (ii) a numerical model based on finite element analysis (FEA). In this study, a finite element model (COMSOL Multiphysics) was used to determine $\kappa_{diamond}$. First, the temperature rise at the center of the TLM gaps was measured using nanoparticle-assisted Raman thermometry. The temperature rise [$\Delta T = T_{surface} - T_{baseplate}$; Fig. 2(a)] as a function of power dissipation (P_{diss}) was measured for several TLM structures with different contact spacings [L_{TLM}; Fig. 2(a)]. Dividing P_{diss} by the active area of the TLM channel ($L_{TLM} \times W_{TLM}$), the heat flux (q″) is determined. The dependence of ΔT on q″ for the diamond TLM structures is shown in Fig. 2(b). Subsequently, these calculated heat fluxes were applied to the active area of the TLM structure in the thermal model. The bottom of the diamond substrate was maintained at room temperature (298 K) for both experiments and modeling. Other surfaces were subject to a natural convection thermal boundary condition. $\kappa_{diamond}$ was then adjusted to match the simulated temperature rise with the experimentally measured temperature rise in the diamond channel. Based on the experimental setup and data provided in Fig. 2, $\kappa_{diamond}$ was estimated to be 1860 W/m K. Using the 95% upper and lower confidence limits for the slope of the linear fit of the data, the 95% confidence interval for the thermal conductivity ranges from 1610 to 2120 W/m·K. It should be noted that the thermal conductivity of the diamond substrate was assumed to be isotropic in this analysis. While diamond thin films have exhibited anisotropic thermal conductivity closer to the nucleation interface due to grain boundary size effects,[45] the large thickness (500 μm) of the diamond substrate should

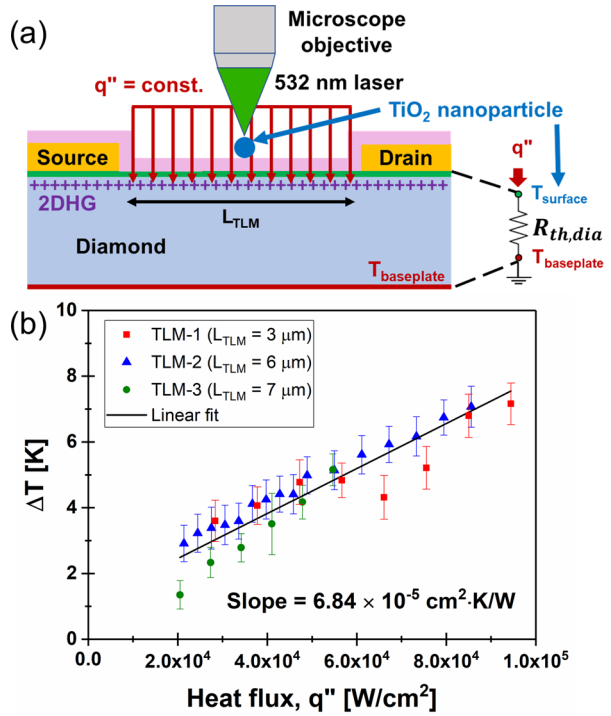

FIG. 2. (a) Schematic diagram of the experimental procedure used to estimate the thermal conductivity of the diamond substrate, including a simplified thermal resistance network. (b) Measured temperature rise of three TLMs as a function of heat flux. The slope of the linear trendline is shown, which is used to calculate the thermal conductivity.

be representative of bulk diamond. Since the transistors in this study were on single-crystal diamond, anisotropic thermal conductivity observed in polycrystalline diamond, attributed to increased phonon-grain boundary scattering as a result of columnar growth,[46] should not be a concern for the single-crystal diamond. This reasoning is also supported by previous experiments[47] where the thermal conductivity of homoepitaxially grown single-crystal diamond was measured to be isotropic.

Having estimated $\kappa_{diamond}$, nanoparticle-assisted Raman thermometry was used to perform thermal characterization on the H-terminated diamond FETs (Fig. 3). Two diamond FETs were used for thermal testing: (FET-1) $L_G = 50$ nm, $L_{GD} = 1\ \mu$m; (FET-2) $L_G = 50$ nm, $L_{GD} = 3\ \mu$m. For both diamond FETs measured, $L_{GS} = 1\ \mu$m. Measured and simulated output characteristics for FET-1 are shown in Fig. 3(a). A schematic diagram of the nanoparticle-assisted Raman measurements is shown in Fig. 3(c). All thermal measurements were performed on nanoparticles in the diamond active channel near the gate electrode. The temperature rise in the diamond channel at the drain-side edge of the gate for FET-1 was measured and plotted as a function of power density in Fig. 3(b). It should be noted that both FET-1 and FET-2 were observed to have temperature rises that agreed within the uncertainty in the measurement. Due to the high thermal conductivity of the CVD-grown single-crystal diamond substrate, the FETs demonstrated very high thermal performance by handling high power densities (~4 W/mm) with very minimal temperature rise (~4 K). The simulated temperature rise from the calibrated electrothermal device model is also plotted in Fig. 3(b) as a function of power density, extrapolated up to a power density of 40 W/mm. The simulated thermal response incorporates the thermal conductivity of the diamond substrate determined previously. In addition, the temperature dependence of the thermal conductivity of diamond (reported elsewhere[37]) was included in the model since there will be a finite reduction in thermal conductivity with an increase in temperature as a result of increased phonon scattering. Again, because of the high thermal conductivity of the diamond, the peak simulated temperature rise of the diamond FET at 40 W/mm is only $\Delta T = 33$ K. Based on the results shown in Fig. 3, the thermal resistance of the H-terminated diamond FET is ~1 mm·K/W in the channel near the drain-side of the gate.

To compare the thermal performance of the diamond FET with other UWBG semiconductors, the thermal resistance of lateral transistor structures based on $Al_{0.70}Ga_{0.30}N$[8] and β-Ga_2O_3[14,33] was also experimentally determined in this study using nanoparticle-assisted Raman thermometry. In addition to these UWBG semiconductors,

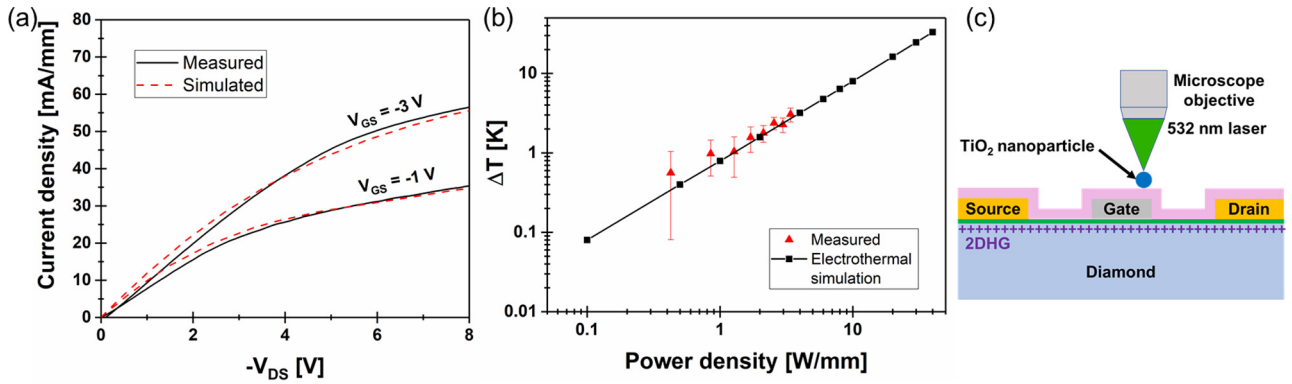

FIG. 3. (a) Measured and simulated output characteristics of the diamond FET ($L_G = 50$ nm and $L_{GD} = L_{GS} = 1\ \mu$m) used for thermal analysis. (b) Measured and simulated channel temperature rise of the diamond FET as a function of power density. (c) A schematic representation of nanoparticle-assisted Raman thermometry on the diamond FET.

the thermal performance of a WBG GaN-based device[26] was also investigated for benchmarking purposes. Details of these lateral device structures are reported elsewhere.[8,14,26,33] For all devices, nanoparticle-assisted Raman thermometry was used to measure the temperature rise on the gate electrode on the drain-side. Since the device geometries are not exactly the same (Table I), there is a possibility that the peak temperature rise on the gate electrode may be slightly underestimated for some device structures due to the location of the nanoparticle with respect to the location of peak temperature rise. To help mitigate this potential source of error, all measurements were performed under open channel conditions at various direct current (DC) power densities [Fig. 4(a)]. Open channel conditions are defined as device biasing such that the drain–source current (I_{DS}) approaches the maximum drain–source current ($I_{DS,max}$) as determined from the transfer characteristics of the device. In other words, devices were tested under open channel conditions, where $I_{DS}/I_{DS,max} \sim 1$. Open channel conditions were used because under pinched-off channel conditions ($I_{DS}/I_{DS,max} \ll 1$), high electric field concentration can lead to very localized heat generation in the transistor channel.[48] Under open channel conditions, this heat generation becomes more distributed; therefore, it should provide the basis for a more unbiased comparison.

The thermal resistances of these UWBG and WBG lateral transistor structures were determined by measuring the temperature rise at the drain-side edge of the gate and dividing ΔT by a given power density (1 W/mm). A comparison of thermal resistances for devices based on next generation UWBG semiconductors experimentally determined in this study at a power density of 1 W/mm is shown in Fig. 4(b). It is immediately evident that the other UWBG semiconductors ($Al_{0.70}Ga_{0.30}N$, β-Ga_2O_3) greatly suffer from a thermal perspective. The thermal resistances of the lateral transistors based on these UWBG semiconductors are up to ∼50× greater than that of the diamond-based lateral transistor. These results are also consistent with previous reports for devices based on UWBG semiconductors. For example, Pomeroy *et al.* reported a thermal resistance of 88 mm·K/W close to the drain-side edge of the gate of a β-Ga_2O_3 MOSFET.[27] While the WBG GaN lateral transistor demonstrates much greater thermal performance than UWBG $Al_{0.70}Ga_{0.30}N$ and β-Ga_2O_3, it still has a thermal resistance of 12.3 mm K/W. This is ∼10× greater than the thermal resistance of the H-terminated diamond FET.

TABLE I. Details of the lateral transistor structures based on β-Ga_2O_3, $Al_{0.70}Ga_{0.30}N$, GaN, and diamond measured in this study (see Fig. 4).

Device architecture	Channel dimension $L_{GS}/L_G/L_{GD}$	Epitaxial structure
MODFET	2 μm/2 μm/3 μm	β-$(Al_xGa_{1-x})_2O_3$/Ga_2O_3 (500 μm)
HEMT	3 μm/2 μm/5 μm	$Al_{0.85}Ga_{0.15}N$/$Al_{0.70}Ga_{0.30}N$ (450 nm) AlN (1.6 μm) Sapphire (1.3 mm)
HEMT	2 μm/1.5 μm/3.5 μm	AlGaN/GaN (4 μm) AlN (50 nm) SiC (470 μm)
FET	1 μm/100 nm/3 μm	Diamond (500 μm)

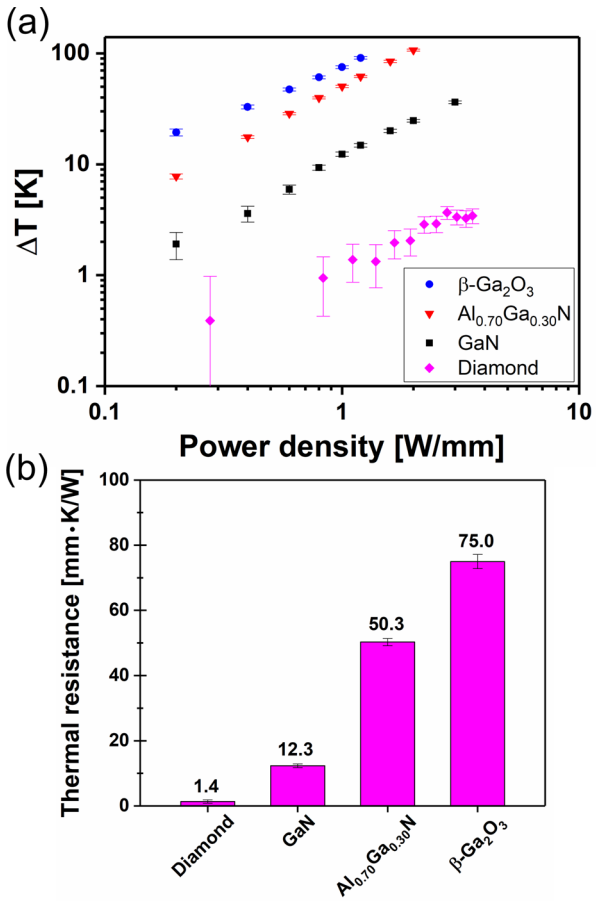

FIG. 4. (a) Temperature rise as a function of power density and (b) thermal resistance at 1 W/mm of lateral transistor structures with diamond, GaN, $Al_{0.70}Ga_{0.30}N$, and β-Ga_2O_3 channels.

Furthermore, lateral devices based on diamond do not need additional thermal management to handle higher power dissipation. Chatterjee *et al.* showed that even with ideal augmented thermal management (double-sided cooling, 1 μm thick nanocrystalline diamond passivation, polycrystalline diamond carrier), the thermal resistance of a lateral β-Ga_2O_3 MODFET was still ∼17 mm·K/W.[33] Presented as a limiting case for maximum thermal performance, the thermal resistance of the UWBG β-Ga_2O_3 lateral transistor with optimal thermal management is still an order of magnitude greater than that for the H-terminated lateral diamond FET of this study, which incorporates no additional thermal management. This strongly indicates that the diamond material system inherently possesses the thermal properties required to meet the heat dissipation demands of next generation devices for higher power RF applications.

In conclusion, the thermal performance of an H-terminated diamond FET has been assessed using nanoparticle-assisted Raman thermometry and an electrothermal device model. Assuming isotropic thermal conductivity, $\kappa_{diamond}$ was estimated to be 1860 W/m K with a 95% confidence interval ranging from 1610 to 2120 W/m K. Using $\kappa_{diamond}$ and measured electrical properties, an electrothermal device

model of the H-terminated diamond FET was created. The simulated temperature field showed good agreement with experimental thermal characterization using nanoparticle-assisted Raman thermometry. From the thermal measurements and device model, the thermal resistance of the diamond FET was found to be ∼1 mm K/W in the diamond channel. The thermal performance of the diamond FET was subsequently compared with GaN, $Al_{0.70}Ga_{0.30}N$, and β-Ga_2O_3 lateral transistor structures by determining the thermal resistance of the various devices at a power density of 1 W/mm. It was shown that the diamond-based transistor exhibits up to 10× improvement in thermal resistance when compared to WBG GaN and up to 50× improvement when compared to the other UWBG semiconductors. In addition to the estimation of thermal conductivity from the as-fabricated TLM gaps using an electrical pump/optical probe experimental procedure, this report quantifies the superior thermal performance of diamond compared to other UWBG semiconductors. These findings demonstrate that diamond is capable of handling the higher power densities expected of UWBG-based microelectronics and provides an avenue for overcoming current thermal obstacles to realize the full potential of UWBG semiconductors.

See the supplementary material for material properties and figures of merit (JFOM, KFOM) of conventional, wide bandgap, and ultrawide bandgap semiconductors and for more details on the estimation of the thermal conductivity of diamond using the thermal model.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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