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Solution-Based, Additive Fabrication of Flush Metal Conductors in Plastic Substrates by Printing and Plating in Two-Level Capillary Channels

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Abstract

A strategy to control the structure of electroless copper deposition in confined features was developed for applications in printed electronic devices and interconnects. This work builds on and refines a previous process of additively manufacturing metal conductors using a combined imprint, print, and plate strategy. A two-level imprinted channel geometry, consisting of inner, parallel capillary channels running along the base surface of a main channel, was designed to control electroless copper deposition. The inner capillary channels contain and precisely position the silver ink seed layer, and the main channel confines the electroless copper as it deposits from the seed layer, resulting in flat copper surfaces that are flush with the surface of the substrate or at a controlled depth. This process produces metal conductors with aspect ratios (height/width) up to ≈ 2 and low edge roughnesses as defined by the imprinting process. The resistance of the final conductors varies linearly with the length and width of the main channel, suggesting high uniformity throughout. Conductive lines with a width of 40 μm and depth of 10 μm had low resistance per unit length (≈ 1 Ω/cm) and retained their performance with repeated mechanical flexing. The methods described here to confine the growth of electroless plated copper are adaptable to form conductors for numerous applications in flexible electronics.

Introduction

Printing and other additive manufacturing processes have tremendous potential for fabricating low-cost and high-performance electronic devices. Printed electronic devices have been demonstrated for a wide variety of applications including display components,[1,2] sensors,[3–5] photovoltaics,[6,7] circuits,[8] wearable electronics,[9–11] and discrete devices[12,13] among others. In these applications, electrically conductive interconnects are required to join discrete devices together into complex circuits.

Optimal properties for interconnects include low resistance per unit length for low power loss and high current carrying capacity, significant mechanical flexibility for wearable and bendable applications, and high precision for accurate placement and connection of devices. Low resistance is achieved by both using a highly conductive material to form the interconnect and a large cross sectional area perpendicular to current flow. To also minimize the amount of surface area used for a printed device and improve device density, high aspect ratio (conductor height / conductor width) designs are essential. Flexibility is achieved by forming the conductor from a ductile and durable material that is not prone to fracture. Avoiding impurity inclusions, specifically hydrogen, has been shown to be key for improving the ductility of electroless plated copper.[14–17] Finally, highly precise metal conductors are formed by carefully controlling all aspects of the materials deposition process. While strategies do exist to target some of these properties, there is a strong need for a single processing strategy that simultaneously addresses all of these. For example, high aspect ratio conductors have been demonstrated by utilizing patterned plastic substrates that control the deposition location of functional conductive materials deposited by doctor blade coating over the patterned substrate.[18] Sometimes this coating is followed by electroplating and consequently polishing is necessary to achieve embedded conductors with flat top surfaces.[19] While these techniques do produce low resistance, additive metal conductors, the use of doctor blade coating of the conductive material means conductive material would be deposited in all molded features of the substrate, preventing the subsequent deposition of other electrically functional materials into other patterned features. Thus, additional patterned features on the substrate could not be utilized to precisely position subsequent layers of other inks, such as semiconductors, required to build complex electronic devices, which limits the applicability of these strategies.

Previously, high aspect ratio, low resistance metal conductors formed by a combined UV imprint, inkjet print, and electroless plate strategy[14] based on the SCALE (Self-aligned, Capillarity-Assisted Lithography for Electronics) process were demonstrated. In SCALE, micro-scale UV imprinting is used to precisely form a network of capillary microchannels, device cavities and ink receiving reservoirs onto a plastic substrate.[20–25] Separate reservoirs and capillary channels are molded in a single micro imprinting step for each layer of functional material in the final device. The simultaneous imprinting of all these structures is critical to achieving the precise alignment of the final layers of functional material. Subsequent ink deposition into the ink receiving reservoirs and flow along the connected capillary channels then deposits multiple layers of printed electronic inks with high lateral accuracy. Fabricating conductors using the SCALE process involves first imprinting reservoirs and capillary channels into a plastic substrate, then printing an ink that deposits a thin silver seed layer on the interior surfaces of these channels, and finally submerging the substrate in an electroless copper plating solution to grow a thick layer of copper from the seed layer as is outlined in Figure 1a. Since conductors are only formed in the capillary channels receiving the silver seed ink during inkjet printing, additional imprinted channels can be left empty for the sequential high-precision deposition of other electrically functional inks to build multi-layer electronic devices. The conductors made by this process demonstrate excellent electrical performance with very low resistance per unit length (as low as 1 Ω/cm) and high durability under bending operations.[14] However, the isotropic growth of electroless copper from the seed layer coating the capillary channel results in a conductor with an irregular profile that typically does not completely fill the channel and has overgrowth from the channel that results in an irregular, bumpy top surface. This complicates the integration of the conductors into functional devices, such as thin film transistors, that require multiple stacked layers

of electrically functional materials[24,26] and prevents close spacing of conductive lines. Deposition of uniform layers of ink on topographically irregular surfaces is challenging due to the gravity and capillarity driven flow and the subsequent coated layer can have thin spots and pinhole defects that lead to device failure.[27]

In this paper, we develop a strategy to confine the electroless copper growth in the capillary channel, leading to metal deposits with a flat top surface, and precisely defined feature edges. The strategy is based on a two-level channel that better defines the seed silver layer deposits and prevents overgrowth of the electroless copper to the substrate surface. The resulting conductors can be tailored to create high current carrying, precisely defined interconnects with predictable electrical performance as well as smooth topped conductors suitable for closely spaced electrodes in multilayer integrated devices.

Experimental

Master Pattern Fabrication

The process for forming a two-level SCALE conductor is outlined in Figure 1. The first step is the fabrication of a master silicon wafer pattern. To fabricate the capillary channels used in this work, multiple photolithography steps were used. The inner capillary channels were fabricated first. To begin, 500 μm thick silicon wafers were dehydration baked on a hot plate at 150 °C for 5 min. The wafers were then placed in an atmosphere of hexamethyldisilazane (HMDS) vapor for 3 min to improve photoresist adhesion. Photoresist (AZ 1512, EMD Performance Materials Corp.) was then spin coated on the wafer at 3000 rpm for 30 s. The wafer was then soft baked at 100 °C for 1 min. The pattern for the inner capillary channel and lower level of the ink receiving reservoir were directly exposed onto the photoresist with a Heidelberg Laserwriter DWL200 using a 5 mm write head. The exposed photoresist was then developed in 1:4 AZ340

developer (EMD Performance Materials Corp): deionized water for 30 s and rinsed with deionized water. The wafer was then hard baked at 100 °C for 1 min. Reactive ion etching was used to etch the developed features into the silicon wafers. First an oxygen plasma clean was performed for 15 s at 100 mTorr pressure, 100 W RF power, and 99 sccm O_2 in an STS Etcher (Model 320) etcher. Then, an etching process based on the work of Legtenberg, *et al.*[28] was used to achieve as rectangular inner capillary channels as possible in the same etcher. Recipe parameters included 100 mTorr pressure, 100 W RF power, and gas flow rates of 30 sccm SF_6, 12 sccm CHF_3, and 10 sccm O_2.[28] The etching rate was ≈ 2 μm/min to reach the desired inner capillary channel depth. The photoresist was then removed using subsequent rinses in acetone, methanol, isopropanol, and deionized water and the wafer was dried with nitrogen gas.

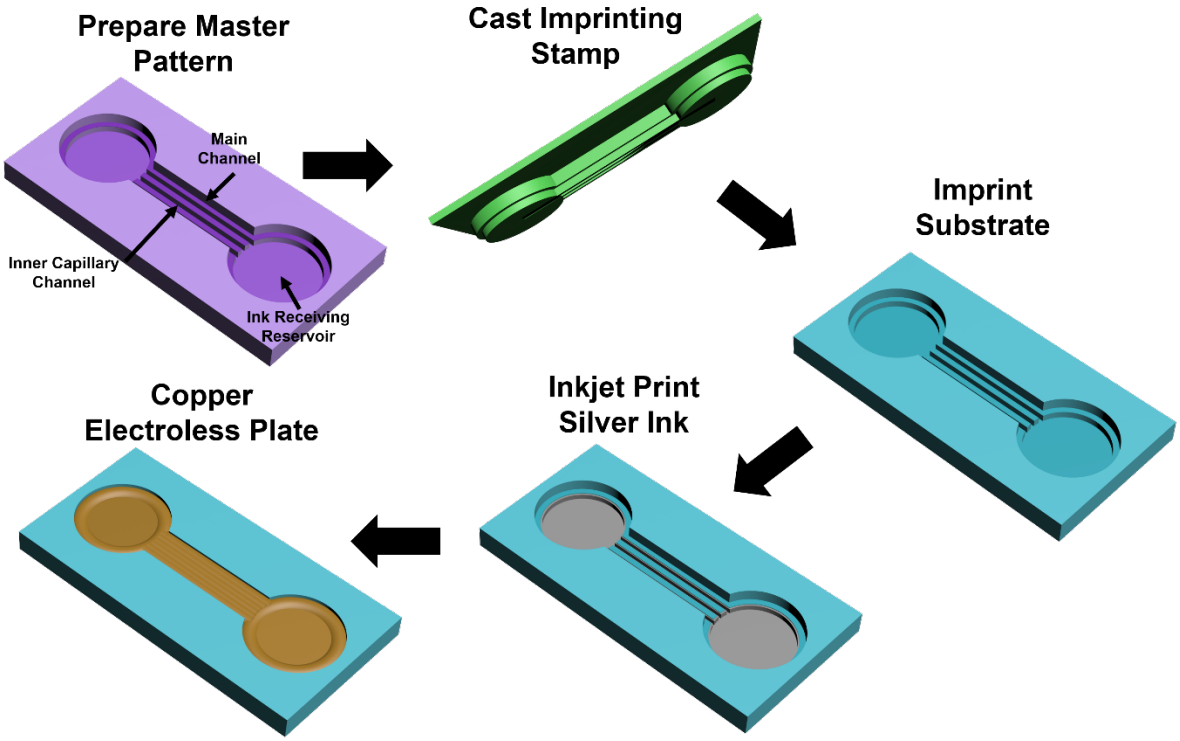

Figure 1: Overview of the process to fabricate a SCALE conductor in a two-level capillary channel.

The main channel and the upper level of the ink receiving reservoir were then formed from SU8 photoresist. First, the wafer was cleaned in a barrel oxygen plasma etcher with an oxygen flow rate of 200 sccm, 200 W RF power, and ≈ 1.4 torr pressure for 10 min. Then MicroChem SU8-2010 negative tone photoresist was coated to a thickness of about 10 μm by spin coating (500 rpm for 5 s, acceleration 100 rpm/s, followed by 2800 rpm for 30 s, acceleration 300 rpm/s) or about 20 μm by spin coating (500 rpm for 5 s, acceleration 100 rpm/s, followed by 900 rpm for 30 s, acceleration 300 rpm/s). Edge bead removal was performed using MicroChem EBRPG. The wafer was then soft baked at 95 °C for 2.5 min (10 μm) or 3.75 min (20 μm). Exposure was performed through a photomask on a Karl Suss MA6 aligner at 12 mW/cm^2 for 10 s (10 μm) or 12.5 s (20 μm) followed by a post exposure bake at 95 °C for 3.5 min (10 μm) or 4.5 min (20 μm). The resist was then developed in propylene glycol methyl ether acetate (Sigma Aldrich) until the features were fully formed, then rinsed with more propylene glycol methyl ether acetate followed by isopropanol and dried with nitrogen gas. Finally, the wafer was hard baked at 150 °C for 30 min. A non-stick monolayer was then deposited on the wafer by placing the wafer in a chamber of 1H,1H,2H,2H perfluorooctyl trichloro silane vapor (Sigma Aldrich) at reduced pressure overnight.

Batch Substrate Fabrication

To fabricate substrates for copper electroless plating thickness measurements, a batch process was used. First, an imprinting stamp was prepared from the silicon master pattern. Sylgard 184 polydimethylsiloxane (PDMS) was prepared at a 10:1 by mass ratio (base: curing agent) and vacuum degassed. Then the PDMS was poured over the silicon wafer master pattern, which was

secured in the bottom of a petri dish. The PDMS was cured at 75 °C for 2 h, and then delaminated from the silicon wafer. The PDMS was then further cured for 2 h at 120 °C, and then 2 h at 205 °C to increase its modulus and durability.

To prepared the patterned substrate, a piece of 127 μm thick polyethylene terephthalate (PET) (Dupont Teijin Melinex ST505) was cleaned in an oxygen plasma cleaner (Harrick Plasma PDC-32G) for 1 min at 1 torr of pressure and 18 W of power to improve resin adhesion. Then UV-curable Norland Optical Adhesive NOA-61 was drop cast on the PET film, the PDMS stamp was pressed into the UV-curable resin, and then the PET, UV-curable resin, and stamp stack was placed into a UV curing system (Honle LED Cube 100, 365 nm powered by a Honle LED Powerdrive 40) for 90 s at ~ 100 mW/cm^2 UV intensity and illuminated through the PDMS stamp. This fully solidified the resin and the PDMS stamp was able to be delaminated without any damage to the cured resin. The cured resin adhered to the PET backing was then post-cured at ~ 100 mW/cm^2 for 180 s from the top side.

Roll-to-Roll Imprinting of Substrates

To fabricate large numbers of substrates for electrical measurements, a roll-to-roll micro imprinting process was used as described in Jochem, *et al.*[14,20] on a commercial roll-to-roll UV micro imprinting machine (Carpe Diem Technologies) at a web speed of 10.2 cm/min, a web tension of 8.9 N, and with additional imprinting pressure from an air knife. This process involves the continuous reverse gravure coating of NOA-61 UV-curable adhesive on the same PET web used in the batch experiments followed by imprinting with a drum-based PDMS imprinting stamp to mold the SCALE features and curing by a high intensity arc lamp UV light source (≈ 4.7 J/cm^2) and a UV post cure after demolding (≈ 7.1 J/cm^2).

Inkjet Printing

The micro imprinted substrates were aged for at least 72 h after imprinting and prior to printing. Inkjet printing was performed based on the procedure described in Jochem, *et al*.[14] using a custom inkjet printer based on a MicroFab Jet Drive III printer controller and a drop-on-demand piezoelectric MicroFab MJ-AT-01-080 80 μm orifice inkjet nozzle. While a variety of materials can be used to catalyze electroless copper deposition including palladium,[29] copper,[30] and polydopamine inks,[31] among others, Electroninks EI-011 reactive silver ink was chosen due to its ease of printing and previously demonstrated excellent capillary flow properties. This ink was printed into the lower level of the ink receiving reservoir at each end of the sets of inner capillary channels. Sufficient ink was deposited to fully fill the reservoir and maintain sufficient liquid in the reservoir throughout the capillary flow process. Capillary flow transported the ink along all of the inner capillary channels for 1-2 min before the substrate was placed on a hot plate heated to 100 °C for 2-3 min to dry the ink. Ink printing and flow was performed in a humidity-controlled enclosure maintained at 50 ± 5 % relative humidity.

Copper Electroless Plating

Copper electroless plating was performed as described in Jochem, *et al.*[14] including the incorporation of a small amount of polyethylene glycol (PEG, Dow Carbowax) in the plating formulation. The PEG was shown in past work to significantly improve the performance of the plated copper in bending.[14] Substrates were suspended in place in the plating solution for the desired plating time and rinsed with distilled water afterwards before being allowed to dry completely.

Conductor Characterization

Specimens for cross-sectional scanning electron microscope (SEM) studies were prepared by first embedding the substrates with conductors in Epon/Polybed 812 resin cured at 63 °C for 48 h. Then a Leica UC7 microtome with glass microtome knife blade was used to cut a flat face across the embedded conductor. A thin conductive gold layer was deposited via sputter coating on the samples to reduce charging in the SEM and a JEOL JSM-6010Plus/LA SEM was used to image the samples in backscattered electron Z-contrast mode and in energy dispersive spectroscopy (EDS) mode. Optical images were collected using a Hirox KH-7700 digital microscope.

Electrical resistance was measured using the two-point probe method with a Keithley 2400 source meter. The reported resistance values are for the full path through the measurement probes, the sections of conductor between the ink receiving reservoirs and main channel, and the length of conductor in the main channel. Substrate bending tests were performed by bending the metal conductor around a glass vial of known radius and then measuring resistance both in the bent and unbent states with a Keithley 2400 source meter.

Results and Discussion

Controlling Conductor Width and Morphology

Precisely controlling the structure of additively manufactured metal conductors is beneficial for improving the conductor performance and functionality. Figure 2 compares the original SCALE conductor fabrication process with the new two-level channel process developed in this work. As shown in Figure 2a, the traditional SCALE process begins with a substrate

containing an imprinted single-level capillary channel.[14,20,32] Then a reactive silver ink[33] is inkjet printed into the ink receiving reservoirs and allowed to flow along the capillary channels. Printing and drying conditions, including relative humidity and flow time, must be very controlled during this process to ensure the ink deposits a uniform film of metallic silver.[14] The imprinted capillary channels confine the silver ink during flow forming narrow, precisely positioned channels with all interior surfaces coated with metallic silver. The substrates are then submerged in an electroless copper plating solution to grow a layer of copper on the printed silver seed layer. While the localized silver in capillary channels defines the location of copper growth, isotopic growth from the seed layer results in considerable copper overgrowth due to the silver at the top of the side walls. The result is an irregular top surface, as shown in Figure 2a, after plating. This irregular, bumpy top surface significantly complicates the deposition of subsequent layers of ink onto the top of the metal conductor, as noted in the introduction.

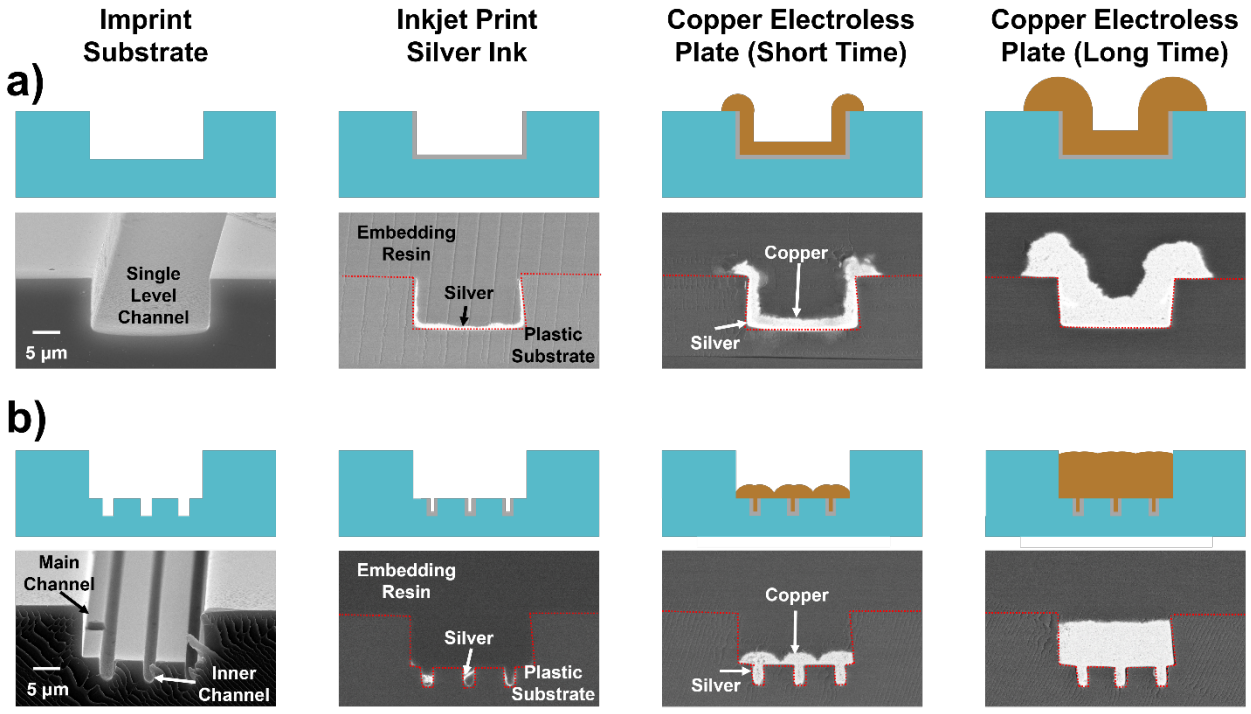

Figure 2: Cross-sectional schematics and SEM images of SCALE conductors prepared with a) the traditional single-level channel method and b) the two-level channel method. Cross sections of

empty channels were imaged in SEM secondary electron mode and cross sections of filled capillary channels were collected after embedding the conductors in epoxy resin and imaged in SEM backscattered Z-contrast imaging mode. The red dashed lines show the interface between the imprint material and the resin used for embedding. SEM images in part a) of this figure are adapted from Jochem, *et al.*[14] and are adapted with permission from Jochem, K. S.; Kolliopoulos, P.; Zare Bidoky, F.; Wang, Y.; Kumar, S.; Frisbie, C. D.; Francis, L. F. Self-Aligned Capillarity-Assisted Printing of High Aspect Ratio Flexible Metal Conductors : Optimizing Ink Flow, Plating, and Mechanical Adhesion. *Ind. Eng. Chem. Res.* **2020**, *59*, 22107–22122. Copyright 2020 American Chemical Society.

To improve surface smoothness and plating control, we developed a new two-level strategy with inner, smaller capillary channels running parallel on the bottom of the main channel, as shown in Figure 2b. These smaller inner channels, rather than the larger main channel, are connected to the ink receiving reservoirs where the silver ink is deposited. Thus, after printing and flow of the silver ink, the walls and bottom of the inner capillary channels are fully coated with the silver seed layer while the walls of the main channel remain free of the seed material. During electroless plating, these smaller, inner capillary channels behave like the single capillary channel of the original process with isotropic growth from all the coated surfaces. As described more in the next section, the overgrowth from these closely spaced inner channels merges to form an even coating of copper across the bottom of the main channel and then the copper grows vertically in the main channel, resulting in a more rectangular copper profile with a flat top, as shown in Figure 2b. These improvements to the profile of the metal conductors formed are achieved entirely by changing the geometry of the capillary channel, not with any changes to the copper electroless plating formulation developed in previous work.[14]

The new two-level process can be tailored to produce metal conductors with a wide range of line widths and highly rectangular cross section profiles. Figure 3 shows cross-sectional SEM micrographs, EDS maps, and top view optical micrographs for conductors with line widths ranging from ≈ 10 μm to ≈ 40 μm. The cross-sectional SEM images confirm the deposited metal is well

adhered to the plastic substrate and that both the inner and outer channels retain their shape during electroless plating. The deposited metal appears solid with no internal voids. EDS maps demonstrate the confinement of the silver seed material to the inner channels, and the uniform width and smooth edges of the conductors are apparent in the top view optical images. The EDS maps also confirm the silver seed layer (identified in green) has only deposited on the surfaces of the inner capillary channels while the deposit in the main channel is copper only (identified in red).

The 10 μm wide conductor (Figure 3a-c) represents the narrowest conductor we have made with this process. In this case, the single inner capillary channel is ≈ 5 μm wide, which is near the limit of the optical photolithography and reactive ion etching we used to create the master pattern. With higher resolution photolithography and etching methods, narrower lines are possible.[34] For example, we have made ≈ 2 μm wide channels with careful control of microfabrication. The main channel width is also set by the need to maintain a gap of ≈ 2 μm between the outer edge of the inner capillary channels and the inner edge of the main channel. This width of side gap space is necessary to ensure the silver seed ink stays in the inner capillary channel and does not flow into the main channel. The precision of this conductor fabrication process relies on the silver seed layer staying confined to the inner capillary channels. The depth of the inner channel is also important to achieve efficient capillary flow and uniform silver deposition.[14] For the channels in Figure 3, the inner channel depth is 5 μm, which is the minimum needed for reliable silver deposition. To increase the conductor width, additional inner channels are included in the design (e.g., two inner channels were used to create an 18 μm wide conductor, Figure 3d-f). The widest conductors formed in this work are ≈ 40 μm wide (Figure 3g-i), but there is no practical limit to conductor width. Achieving a flat top surface on conductors in wider channels also requires attention to the spacing between the narrow inner channels, as discussed later.

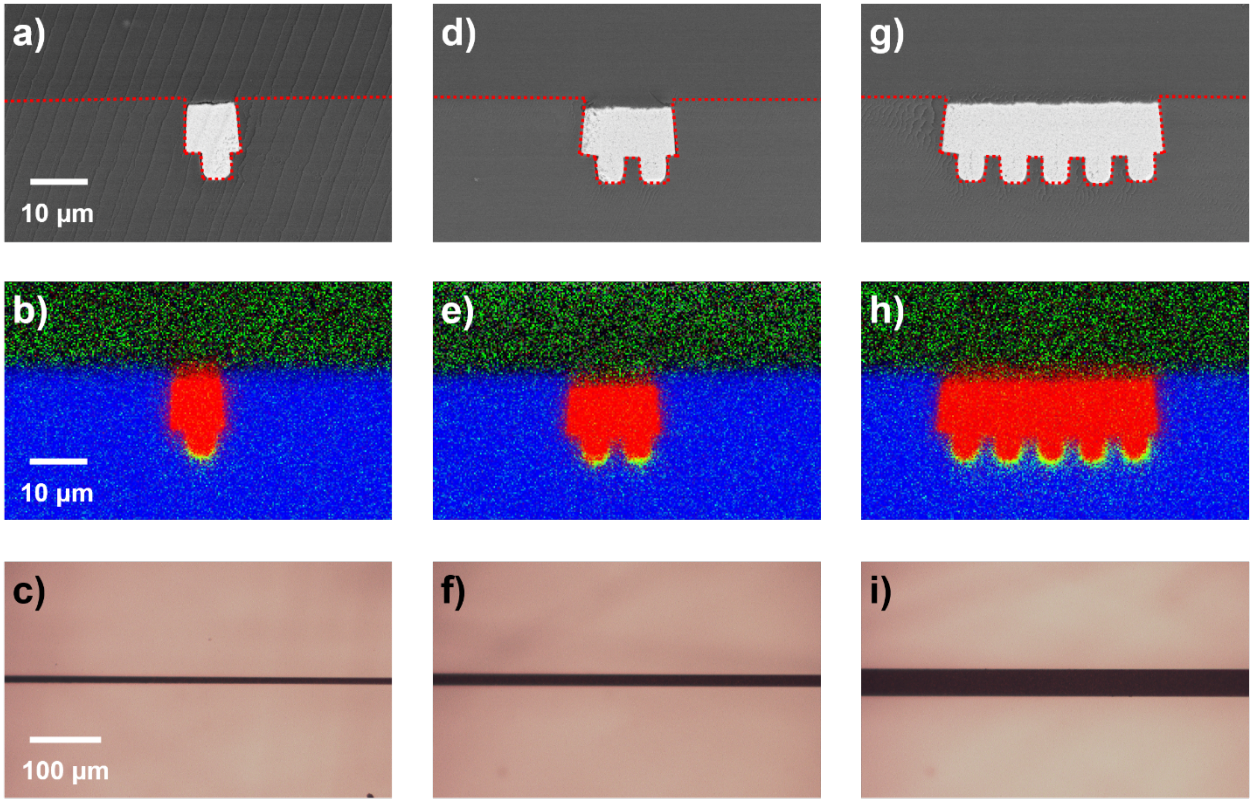

Figure 3: Two-level SCALE conductors of varying width prepared from 5 µm wide and 5 µm deep inner capillary channels: a) – c) show a cross-sectional Z-contrast backscattered SEM image, a cross-sectional EDS map showing the plastic substrate in blue, the silver seed layer in green, and the copper in red, and a top view optical image of a ≈ 10 µm wide conductor, respectively. d) – f) show the same sequence of images for a ≈ 18 µm wide conductor. g) – i) show the same sequence of images for a ≈ 40 µm wide conductor.

The 10 µm wide conductor in Figure 3 is an excellent example of the high aspect ratio (depth/width) achievable with this process. Ignoring the narrow inner channel, the aspect ratio is roughly 1. This value greatly exceeds the typical values achieved using traditional printing methods, such as inkjet printing, gravure printing, screen printing, and aerosol jet printing.[35–38] Even higher aspect ratios can be achieved with this new process by increasing the depth of the main channel. The electroless plating process is stable and able to fill main capillary channels 20 µm deep in a single plating step. By making the main channel ≈ 10 µm wide and ≈ 20 µm deep, conductors with aspect ratio ≈ 2 were produced as shown in Figure 4.

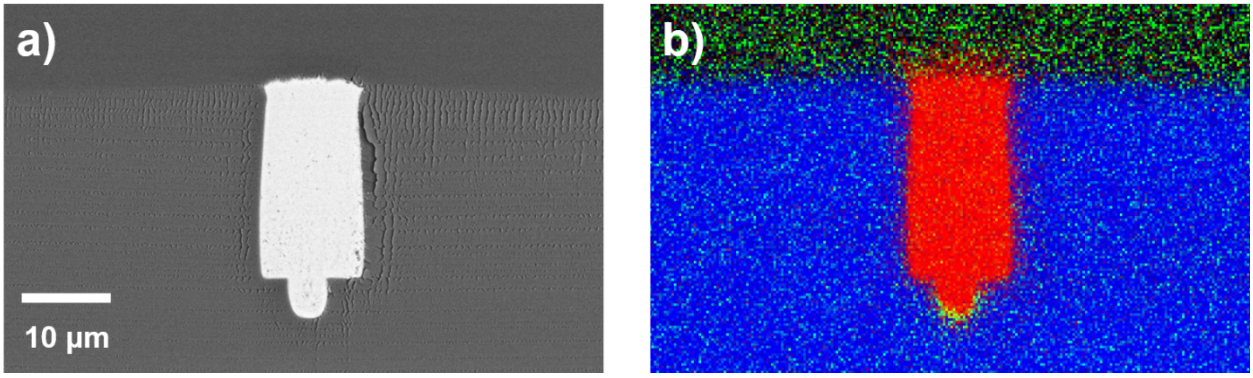

Figure 4: High aspect ratio two-level SCALE conductor: a) cross-sectional Z-contrast backscattered SEM image and b) cross-sectional EDS map showing the plastic substrate in blue, the silver seed layer in green, and the copper in red. The main channel is ≈ 10 µm wide and ≈ 20 µm deep. A 10 h copper plating time was used.

The edges of conductors fabricated with the two-level process are much smoother than those of the original, single level SCALE conductors (see comparison in Supplementary Figure S1[14]), because irregular copper overgrowth from the main channel can be prevented by selecting the appropriate plating time. For the ≈ 10 µm deep main channels shown in Figure 3, a plating time of 4.5 h was selected to fully fill the main to just below the top surface to achieve the desired rectangular conductor profile with well-defined uniform edges and flat top surface for a variety of different conductor widths.

Copper Plating Rate

Cross-sectional SEM images showing the effect of plating time on the development of two-level conductors are shown in Figure 5 for two conductor widths. Images of the silver seed layer alone indicate that the seed layer thickness is somewhat thicker in the bottom of the inner channels. This is likely due to the rounded bottom corners of the inner capillary channel produced during the photolithography fabrication of the master pattern and the wetting behavior of the silver ink in

these capillary channels. After 0.5 h of electroless plating, a thin layer of copper has formed on all surfaces of the silver seed layer, and after 1 h, thickening of the copper in the inner channel is clear along with some overgrowth of copper into the main channel. With continued plating, the copper fills in the inner channel and the overgrowth extends into the main channel eventually merging (i.e., after 2 h of plating). Once a copper layer covers the bottom of the main channel, continued plating results in a thickening of this layer until the thickness just reaches the plane of the imprinted substrate (i.e., after 4.5 h of plating). The side walls of the outer channel keep the copper growth confined as the main channel fills with copper from the bottom to the top. If the plating is allowed to continue, then overgrowth from the main channel is observed (i.e., after 5h of plating).

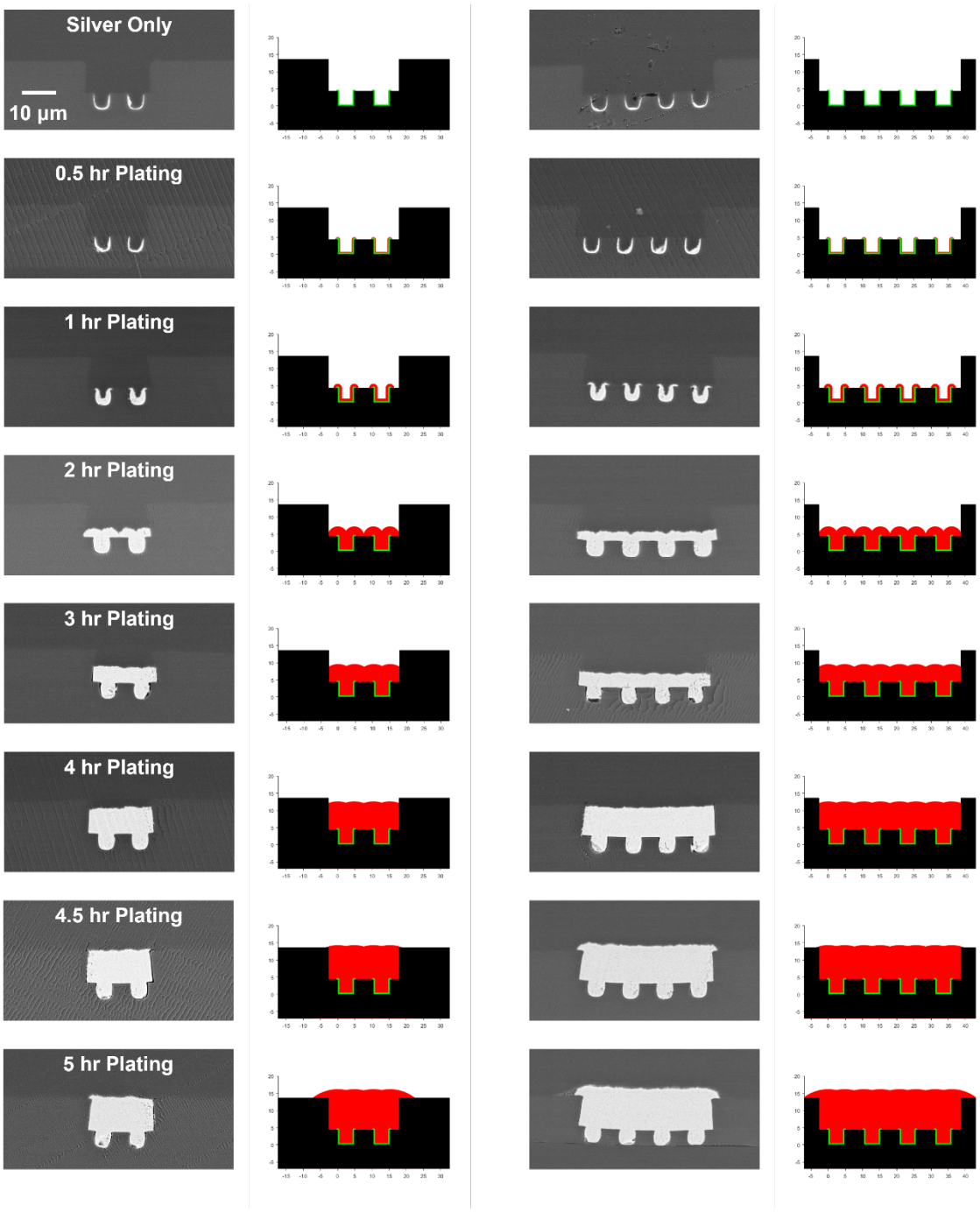

Figure 5: Cross-sectional Z-contrast backscattered SEM images (left) and empirical model predictions (right) of the copper electroless deposition as a function of time for two different capillary channel geometries, ≈ 18 µm wide and ≈ 40 µm wide, both have channel depths of ≈ 4.5 and ≈ 10 µm for inner and main channels, respectively. Plating times are labeled. Dashed lines are not shown in these images to distinguish the plastic substrate from the embedding resin, but they would be located in the same place as seen in the previous figures. In the empirical predictions, the copper is shown in red, the silver seed layer in green, and the plastic substrate in black.

The time progression in Figure 5 shows that copper grows outward from all surfaces of the inner channel coated with the seed layer. The thickness of the copper deposited in the channel can be measured using the assumption of isotropic growth from all coated surfaces. To avoid the complications, such as discerning the plated copper from silver at the bottom of the channel, the copper thickness was measured from the top corners of the inner capillary channel, as described in the Supplementary Information (see Supplementary Figure S2). Additionally, growth from the corner point is of practical interest as it defines the height of the copper in the main channel, and as soon as the inner capillary channels fill in with copper, the growth initiated from the side walls of this channel stops. For each substrate, three measurements were performed, and the average copper thickness was calculated.

Figure 6 shows the total metal (copper and silver seed layer) thickness as a function of plating time for copper grown in two- level channels with main channel depths of ≈10 μm (see Fig. 3) and ≈ 20 μm, as well as on a flat surface coated with silver. Cross-sectional SEMs of the electroless copper growth in the 20 μm deep main channels and the electroless copper growth on the flat surface are shown in the Supplementary Information (Supplementary Figures S3 and S4). Instantaneous copper deposition rates calculated from this data are shown in Supplementary Figure S5. There is noise in the measured metal thickness data because of the relatively small sample size. This data is representative, but we have noticed that batch to batch measured metal thickness may vary by as much as 10%, especially at longer plating times. Further optimization of the electroless plating chemistry could help reduce this variation, but the level of control demonstrated here produces conductors of controlled thickness and properties and is a significant improvement on past work.[14,20]

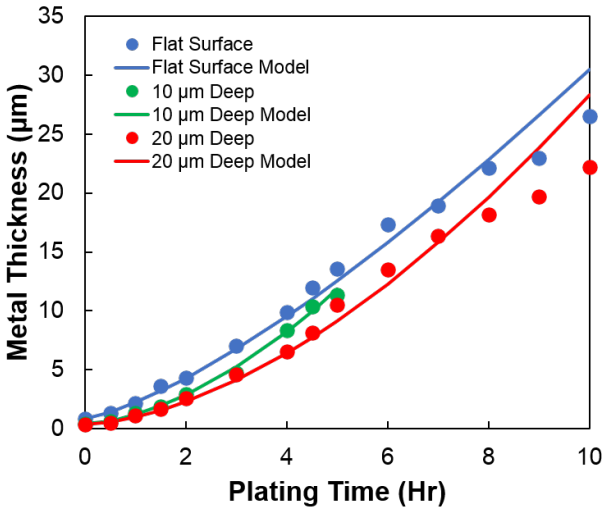

Figure 6: Measured total metal thickness as a function of plating time for three different geometries: two-level channels with ≈ 10 µm deep main channel and ≈ 20 µm deep capillary channel each with silver seed layer coated inner channel(s), and a flat surface coated with a silver seed layer. Growth in the 10 µm deep capillary channel was terminated after 5 h because the channel was filled. Solid lines show the total metal thickness based on a power law fit of the data.

As shown in Figure 6, the deposition rates in both the 10 µm and 20 µm deep main channels are very similar, certainly within the range of measurement error. Past about 2-3 h of plating in either of these channels, the copper growth rate stabilizes at approximately the same rate as that observed on the flat surface (shown by their similar slopes) and maintains this value for the rest of the plating time. The exact reason for the lower plating rate in the two-level channels at earlier times is not known. Generally, a constant plating rate is expected for electroless plating if the reactant concentrations and plating bath temperature are kept constant. To encourage a uniform composition in the plating bath, the bath is stirred and one reactant, formaldehyde, is added periodically; however, the reactant concentrations are not constant, which likely affects the plating rate.[39–43] Additionally, the well-mixed condition may not extend to inside the channel geometry and some initial suppression of plating rate may occur due to local depletion of reactants. Diffusion limitations on copper electroless plating rate have been shown to affect deposition rate

inside narrow vias and tubes due to reactant depletion at the bottom surface of the device.[40,43,44] The transition to a nearly constant plating rate occurs roughly at the time when the inner channels are filled (≈ 1.5 – 2 h).

Empirical equations for the copper thickness as a function of plating time were found from the data in Figure 6, as described in the Supporting Information (Supplementary Figure S6). Using these empirical models, the copper thickness profiles in these two-level channels were predicted and are shown in Figure 5 with the plastic substrate shown in black, the silver seed layer in green, and the deposited copper in red. While there is experimental variation in copper deposition thickness from batch to batch as discussed above, the empirical models accurately capture the copper deposition profile over the full plating time in the 10 μm deep main channels and only show noticeable deviation at the longest plating times in the 20 μm deep channels and on the flat surfaces. The predicted total metal thickness based on the empirical model is represented by the solid lines in Figure 6. The slower deposition during the first ≈ 2 h of the plating experiments is clearly seen for the deposition inside the 10 and 20 μm deep capillary channels.

Effects of Inner Channel Geometry on Copper Profile

The effects of geometry and spacing of the inner capillary channels are shown in Figure 7 for 2 h of plating (about at the point of merging of the inner features) and Figure 8 for 4.5 h of plating (about at the point of fully filling the main channels). Results from the 2 h plating time show that a smoother top copper surface is formed with closer spaced inner capillary channels. Narrower inner capillary channels also provide a small advantage for achieving a flatter top copper surface. Both closer spacing and narrower inner capillary channels increase the number of inner capillary channels, and hence increases locations for initiation of copper growth into the main

channels. Since the growth from the top corners of each inner capillary channel defines the top copper surface, as explained in Supplementary Figure S2, more closely spaced seed locations reduce the amount of growth necessary before adjacent growth fronts merge, leading to a flatter top surface profile. To explore reproducibility, a similar series of experiments was performed with the same inner capillary channel geometry and plating time, but with a slightly wider main channel; results are shown in Supplementary Figure S6. Similar deposition behavior is observed in this second set of samples since the growth profile of the electroless copper primarily depends on the placement of the inner seed capillary channels.

We have found limitations in the implementation of narrow inner capillary channels, specifically the ≈ 2 μm wide inner capillary channels used in Figure 7 and Figure 8. First, the narrow, and especially narrow and tall, features of the imprinting stamps that mold these channels are more likely to deform and buckle during imprinting.[20] Second, achieving a uniform silver seed layer in narrow capillary channels is difficult due to the tendency for defects and incomplete capillary wall coverage that results from flow and drying behavior of the particle-free silver ink in channels of this geometry.[14] The inconsistent coating of these narrow capillary channels with the silver ink leads to inconsistent measured copper deposition thickness. Therefore, we have chosen inner capillary channels with a minimum width of approximately 5 μm, where these issues are not observed, for the remainder of this work.

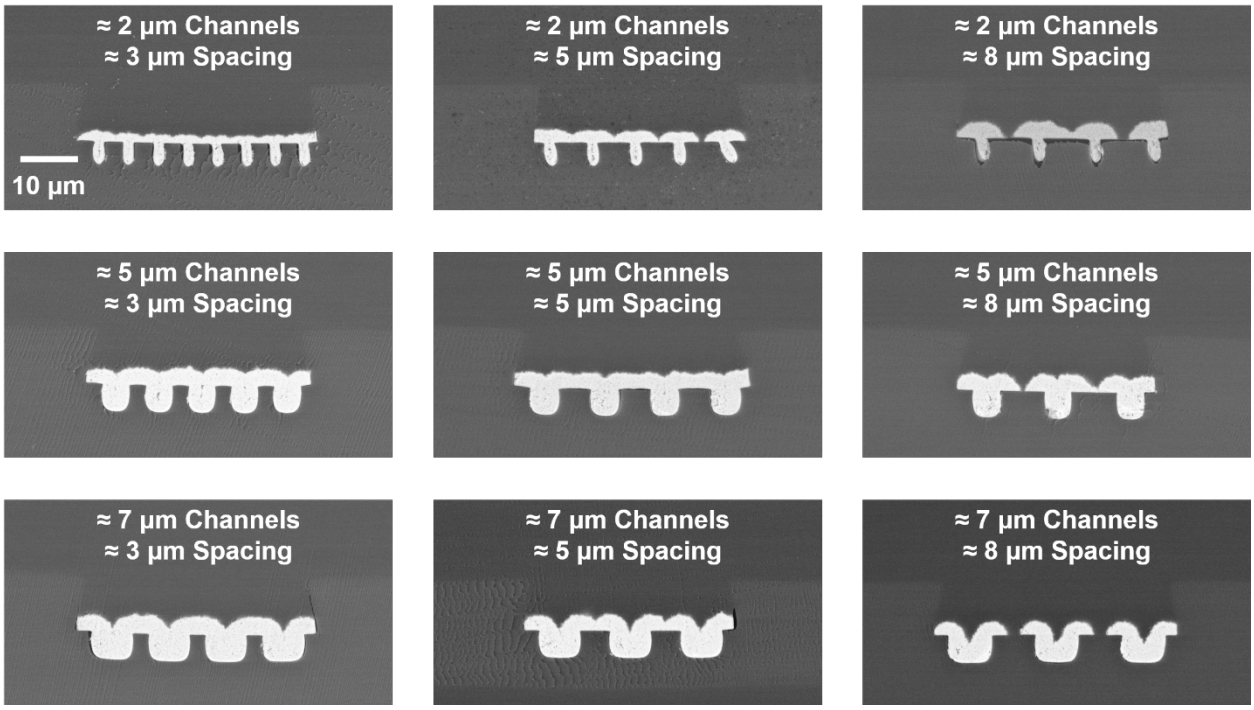

Figure 7: Cross section Z-contrast backscattered SEM images of conductors prepared in ≈ 40 µm wide and ≈ 10 µm deep main channels with a variety of inner capillary channel geometries and plated for 2 h. All channels have ≈ 2.5 µm of space between the outer edge of the inner channels and the wall of the outer channel. Each figure is labeled with the capillary width / capillary spacing.

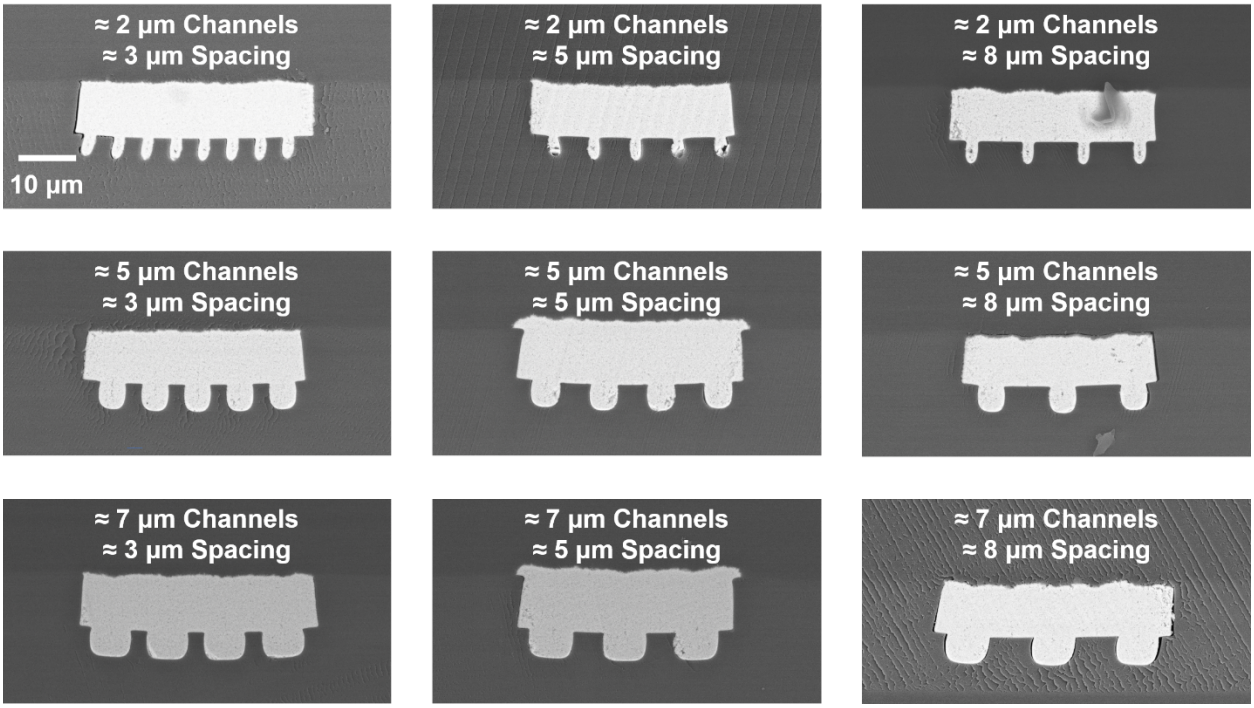

Figure 8: Cross section Z-contrast backscattered SEM images of conductors prepared in ≈ 40 µm wide and ≈ 10 µm deep main channels with a variety of inner capillary channel geometries and plated for 4.5 h. All channels have ≈ 2.5 µm of space between the outer edge of the inner channels and the wall of the outer channel. Each figure is labeled with the capillary width / capillary spacing.

With longer plating times, the surface flatness becomes less dependent on the inner capillary channel structure as shown in Figure 8. Closer spaced and narrower capillary channels demonstrate a slightly flatter top surface as expected, but all inner capillary channel structures tested gave a relatively flat top surface after 4.5 h of plating. The smoother top surface at longer plating times is expected due to the isotropic growth of the copper, as illustrated in Supplemental Figure S2; the radii of the circles defining the top surface increases with increasing plating time, and hence their surface curvature, decreases. The smoothing tendency with plating time is shown in the model predictions in Figure 5 and the diagrams in Supplementary Figure S2. Thus, for all but the largest inner capillary channel spacings, a very smooth top surface is achieved by the time the metal reaches the top of the main channel.

Conductor Resistance and Durability

The electrical resistances of a variety of two-level conductors are shown in Figure 9 using the two-point probe resistance measurement method. Samples were prepared with two inner channel depths (≈ 5 and ≈ 10 μm), three main channel widths (≈ 10, ≈ 20 and ≈ 40 μm), two plating times (2 h and 4.5 h) and a range of main channel conductor lengths. All inner capillary channels were ≈ 5 μm wide and spaced ≈ 5 μm apart. The details of the sample geometry are shown in Figure 1 and cross section SEM images of the ≈ 40 μm wide conductors used in the measurements are shown in the inset images on Figure 9. For conductors prepared with ≈ 5 μm deep inner capillary channels (Figure 9a and Figure 9c), resistances were measured with samples having main channel lengths of 2 and 4 mm. Longer conductor lengths (up to 8mm) were obtained with deeper inner capillary channels (≈ 10 μm deep) (Figure 9b and Figure 9d) compared to the shallower inner channels due to the increased flow and longer evaporation times of the liquid ink. This conductor length represents the maximum length which can be achieved between two reservoirs with the geometry of channels used in this work. The achievable useful flow distance of the silver seed ink used to pattern these conductors in open capillary channels in the presence of evaporation has been discussed in detail in previous work.[14] Briefly, the use of deeper capillary channels significantly reduces the influence evaporation has on the pinning of the forward ink meniscus during capillary flow due to the larger volume of liquid ink present in the channel for a given channel width. Thus, increasing the inner capillary channel depth significantly increases the length of useful flow of the silver seed ink, allowing the formation of longer conductors. For each channel geometry and plating time, the resistance increases linearly with main channel length, indicating a uniform structure along the conductor. The reported resistance values include the contact resistance from the portion of the conductor connecting the main channel to the ink receiving reservoir contact

points (0.75 mm on each end) and the internal measurement system resistance, and hence there is a non-zero y-intercept. For the conductors prepared with 4.5 h of plating, these contact resistance values ranged from 0.35 to 0.5 Ω, a significant fraction of the measured resistance values.

To check the reproducibility of the two-level channel conductor fabrication process, a second set of conductors were fabricated using inner capillary channels spaced ≈ 3 μm apart instead of ≈ 5 μm and the resistances of these conductors are shown in Supplementary Figure S7. These conductors demonstrated very similar electrical resistance to the conductors with inner capillary channels spaced ≈ 5 μm apart, suggesting good reproducibility.

The resistance also predictably changes with plating time and main channel width. For any given geometry, longer plating times result in thicker copper deposits and lower resistance. Low resistances, ideal for interconnects and electrodes, are achieved both for thinner copper that partially fills the main channels (2 h of plating; Figure 9a and Figure 9b) and thicker copper that completely fills the main channels (4.5 h of plating; Figure 9c and Figure 9d). Notably, 8 mm long conductors with resistances of only ≈ 1 Ω (including contact resistance) were prepared in 40 μm wide capillary channels plated for 4.5 h. Likewise, the resistance drops predictably with the main channel width. For example, the resistance of a 40 μm wide conductor is roughly half of that of a 20 μm wide conductor with all other variables kept constant. The average resistance per unit length for the conductors prepared with 4.5 h of plating and the two different spacings of 10 μm deep inner channels is 0.9 Ω/cm (40 μm wide main channel), 1.9 Ω/cm (20 μm wide main channel) and 3.7 Ω/cm (10 μm wide main channel), further confirming the linear scaling of resistance with main channel width. By comparison, the copper overgrowth in single-level SCALE conductors interferes with linear scaling of resistance with channel width. The improved scaling of resistance with conductor width is due primarily to the rectangular cross section of the conductors formed

from the two-level channel geometry. This linear scaling of resistance with conductor width is beneficial for conductor design as the performance of conductors can easily be predicted.

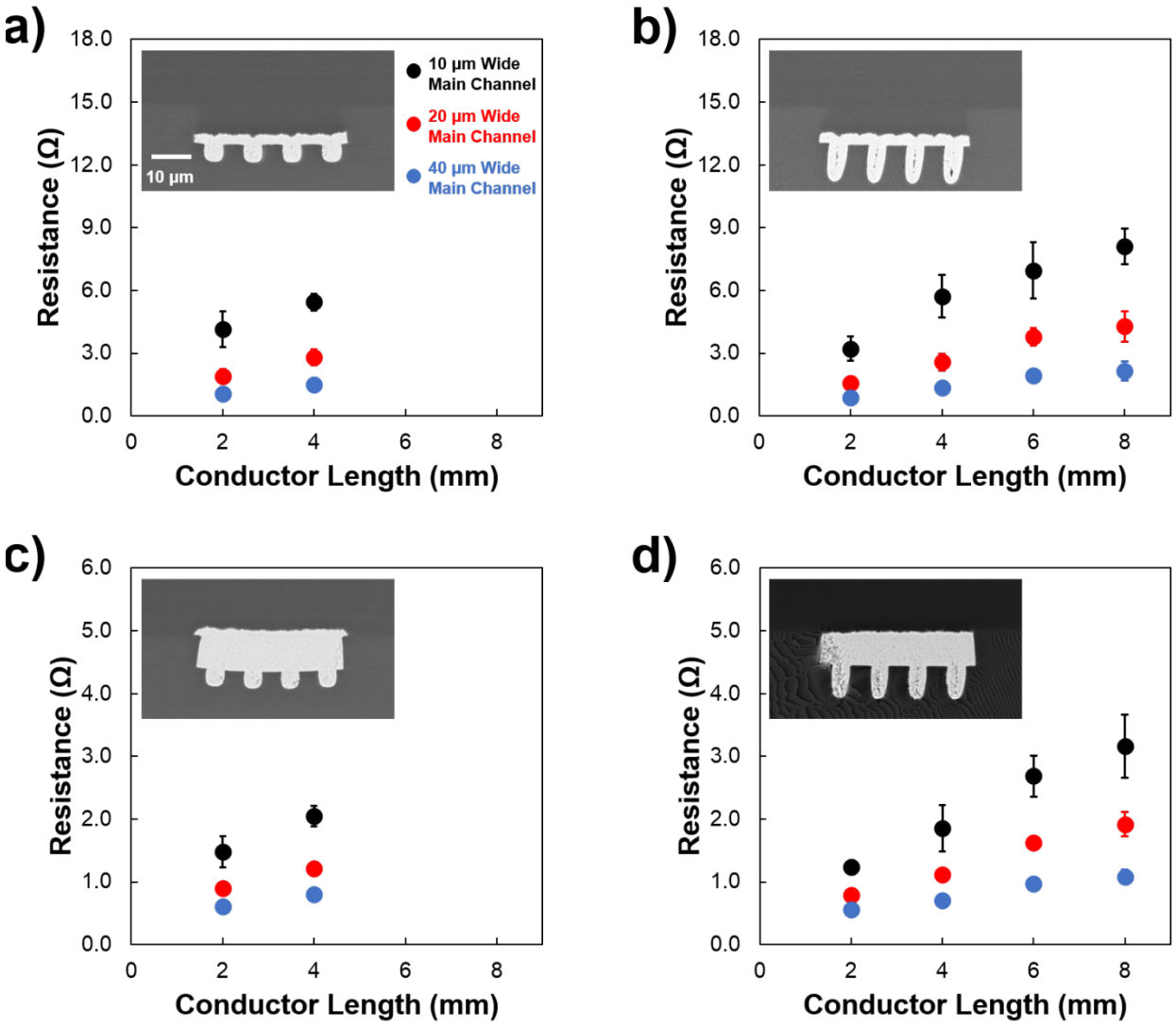

Figure 9: Measured resistance for conductors fabricated in a variety of two-level channel geometries (widths ≈ 10, ≈ 20, and ≈ 40 µm wide) with ≈ 5 µm wide inner capillary channels. a) Conductors with ≈ 5 µm deep inner channels and plated for 2 h. b) Conductors with ≈ 10 µm deep inner channels and plated for 2 h. c) Conductors with ≈ 5 µm deep inner channels and plated for 4.5 h. d) Conductors with ≈ 10 µm deep inner channels and plated for 4.5 h.

To determine the uniformity and consistency between conductors of varied length prepared with the two-level conductor fabrication strategy, resistance per length was calculated for the conductors prepared with ≈ 10 µm deep and ≈ 5 µm wide inner capillary channels spaced ≈ 5 µm apart and plated for 2 h (Figure 10a) and plated for 4.5 h (Figure 10b). Zero-length contact resistance was subtracted from the data shown in Figure 9b and Figure 9d and then the values were divided by the conductor length to obtain these results. See Supplementary Figure S8 for the linear fits used to calculate contact resistance. This removes the resistance from the portion of the conductor outside both ends of the two-level channel and contact resistance from the measurement system. The calculated resistance per length values are quite consistent as a function of conductor length, especially for the ≈ 20 µm wide and ≈ 40 µm wide main channels, indicating consistent performance across the tested range of two-level conductor lengths.

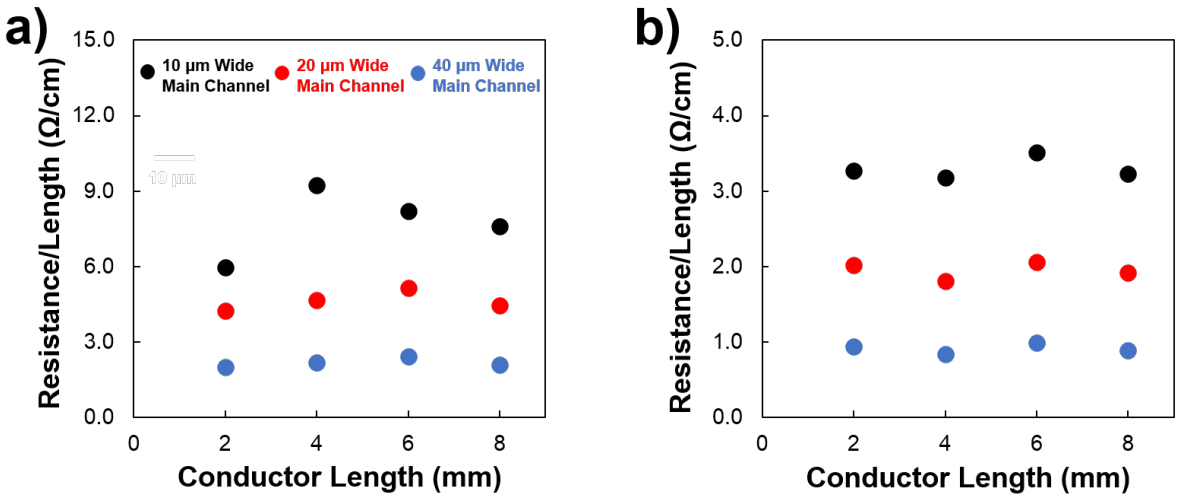

Figure 10: Calculated resistance per length of the two-level conductors prepared with ≈ 10 µm deep and ≈ 5 µm wide inner capillary channels spaced ≈ 5 µm apart found by subtracting off zero-length contact resistance and then dividing this corrected resistance by the length of the conductor for a) 2 h copper electroless plating and b) 4.5 h copper electroless plating.

Conductors formed in the new, two-level, capillary channel demonstrate significant durability during bending as shown in Figure 11. Results are shown for low resistance conductors

prepared with 40 μm main channel widths, 4 mm lengths and either partial filling (2 h plating time; see inset in Supplementary Figure S7b) or complete filling (4.5 h plating time; see inset in Supplementary Figure S7d) with resistances per length of ≈ 1.3 Ω/cm and ≈ 0.6 Ω/cm, respectively. These conductors used inner capillary channels 5 μm wide and 10 μm deep spaced 3 μm apart. Testing was carried out by bending around either a 13.5 mm radius vial from thinner conductors, resulting ≈ 0.63 % tensile strain, or a 26.5 mm radius vial for thicker conductors, resulting in a ≈ 0.32 % tensile strain assuming a plane of zero stress through the middle height of the layered substrate. These radii of curvature represent the minimum radii where the conductors reliably survived 1000 bending cycles. Conductors were bent alone their length (longitudinally) with the metal conductor facing outward to place the conductors in tension along their lengths as this orientation has been previously observed to most easily damage the printed and plated SCALE conductors in comparison to bending in the transverse direction. Equivalent resistances per length in the bent and unbent state demonstrate that the conductor did not experience cracking during the bending action, suggesting the metal deposits likely demonstrate significant ductility. As shown in past work, the addition of PEG to the plating bath prevents embrittlement of the copper.[14] The conductors prepared in two-level channels and plated for two hours tolerate 1000 bending cycles with approximately the same radius of curvature as traditional single level channel SCALE conductors plated for one hour while demonstrating similar linear resistance, suggesting the use of a two-level capillary channel does not harm the flexibility of these devices.[14] Moreover, no delamination occurred in bending, indicating excellent adhesion between the conductor and the plastic substrate. This level of performance should be sufficient for wearable electronics applications and processing on roll-to-roll manufacturing equipment.

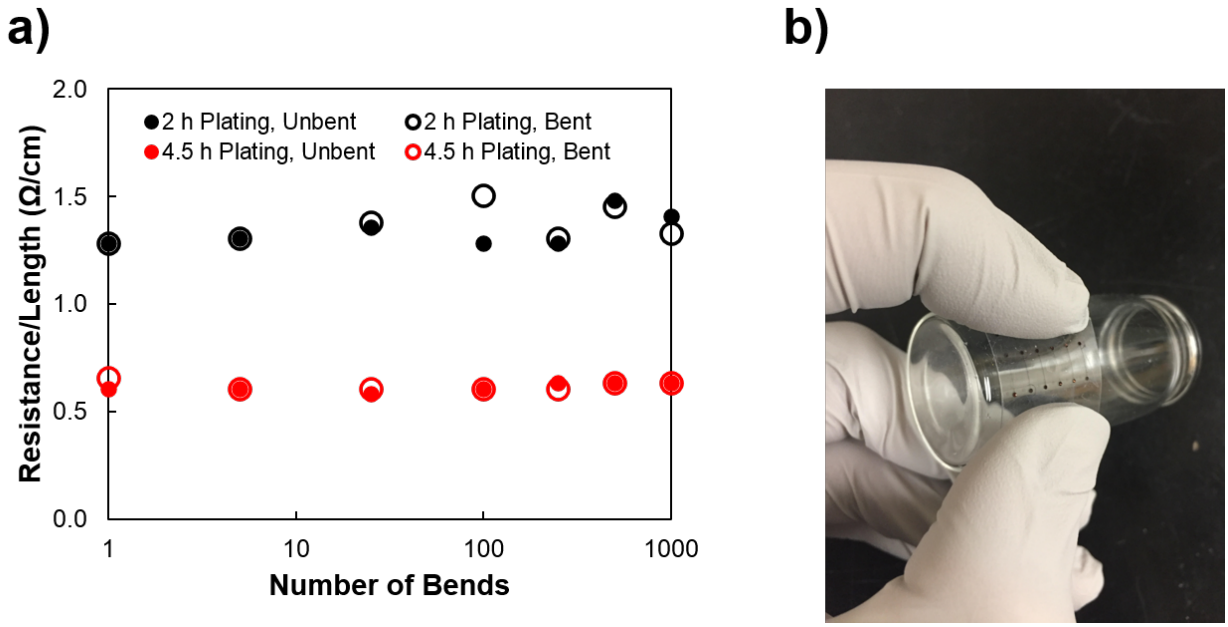

Figure 11: a) Measured resistance per length for 4 mm long and ≈ 40 μm wide two-level channel conductors (≈ 5 μm wide and ≈ 10 μm deep inner capillary channels spaced ≈ 3 μm apart) for 2 h of plating time and bent with 13.5 mm radius of curvature (0.63 % strain) and for 4.5 h of plating time and bent with 26.5 mm radius of curvature (0.32 % strain). Closed circles are for measurements taken with the conductor in an unbent state and open circles are for conductors measured in the bent state. b) Photo of a two-level channel conductor substrate while being bent around the 13.5 mm radius vial.

Conclusions

Thorough this work, we have developed a technique for additively manufacturing high precision metal conductors. By creating a two-level channel to confine copper electroless plating, more rectangular and uniform metal cross sections are prepared compared to conductors formed from a single-level capillary channel. The silver seed layer deposition in the inner capillary channels serves as a nucleation site for electroless copper growth and the copper growth from the inner capillary channels merges to create a flat layer of metal at the bottom of main channel. The copper then continues to grow vertically in the main channel, filling it in. The sidewalls of the main channel confine the metal growth, leading to flat-sided metal conductors. The plating is

reproducible, allowing for the level of metal filling in the capillary channel to be predicted with a simple empirical model. This allows us to make conductors that are flush with the substrate surface or recessed without metal on the side walls of the channel and prevent copper overgrowth. Narrow and deep conductors with aspect ratios greater than one and without overgrowth of metal onto the surrounding substrate with precisely defined edges were prepared. These metal conductors also have very low resistance and are flexible. The control afforded by the two-level channels results in precisely fabricated metal conductors for integration into printed electronic devices.

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