An Autonomous, Optically-Powered, Direct-to-Digital Sun-Angle Recorder for Honey Bee Flight Tracking

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***Abstract*—An autonomous sensor for insect flight tracking that captures and stores solar angle-of-incidence without the use of a conventional ADC is presented. The chip uses pairs of Angle-Sensitive Pixels as differential 1-bit ADCs, and an array of these sensors provides a many-bit encoding of angle-of-incidence. Digitization occurs immediately within the pixel by use of a novel in-pixel comparator, thus enabling ultra-low-power, direct-to-digital capture of angle-of-incidence. These measurements are stored in an on-chip memory throughout the flight and can be uploaded to a base station via magnetic backscatter at the end of the flight. To permit full autonomy, the system is powered by on-chip photovoltaics, providing open-circuit voltages in the range of 0.40 – 0.50 V in natural sunlight, the intensity of which can vary throughout a flight. The system consumes a simulated 630nW at nominal supply voltage of 0.45 V, and circuit topologies amenable to photovoltaic power conditions are presented. The chip is envisioned as a flight recorder to be mounted on honey bees to track their trajectories, and bee flights were emulated by carrying the chip along a 226 m outdoor trajectory and downloading the recorded flight data from the chip at a base station in the field. Across 18 trials of the same trajectory, which emulates a small sample of tagged bees visiting known feeding sites and returning to their hive, the average reconstructed final position is 9.6 m away from the true final position, an error less than 5% of the total trajectory length.**

***Index Terms*—Autonomous ICs, smart dust, angle-sensitive pixels, integrated photovoltaics, direct-to-digital sensing, insect tracking.**

I. Introduction

WHILE the concept of 'smart dust' has been in the literature for almost two decades [1], chip-scale autonomous sensor systems have only recently emerged, and often involve multi-chip assembly [2], [3], [4]. Autonomous sensors aim to integrate most or all functionality on a single low-cost CMOS die, including signal detection, memory, data processing, communication circuitry, and power harvesting. The small size and capacity for untethered operation of autonomous ICs makes them well-suited to serve as tracking tags for monitoring insects. Many bee tag designs have been reported in the literature, with an emphasis on producing smaller, less burdensome tags with increasing levels of functionality. On the small end, commercial integrated RFID tags measuring 0.5-2.5 mm on a side and weighing 0.9-5.4 mg [5], [6] have been successfully deployed on honey bees. While the small size helps with deployment, these tags can only detect the passage of tagged bees past RFID readers, generally positioned at the hive and at feeder stations, and cannot track bees while in transit or when visiting non-instrumented sites. In contrast, a larger research prototype tag has been reported [7] that offers continuous tracking of position via RF localization. Built from discrete components on an aggressively miniaturized PCB, this tag measures 6.1 mm x 6.4 mm, weighs 102 mg, and has been successfully deployed on bumble bees, which can tolerate the larger size and weight.

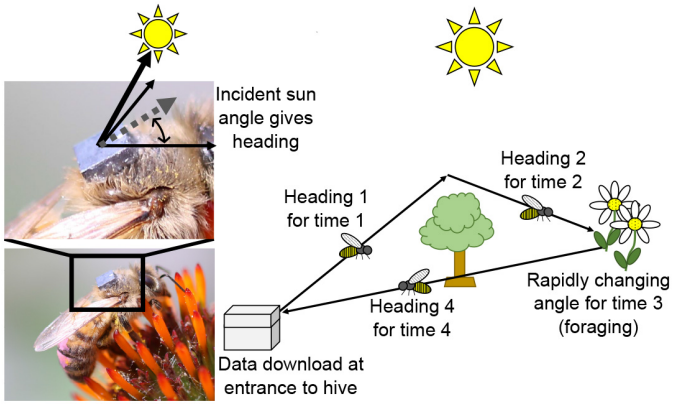

Fig. 1. Concept of integrated flight path recorder mounted on honey bee, showcased with dummy silicon.

In an effort to achieve continuous tracking at smaller scale, we present a 2.25 x 2.4 mm^2 autonomous IC for recording the flight patterns of honey bees (Fig. 1). Since honey bees tend to travel in straight paths at a constant, known speed [8], heading measurements are sufficient to reconstruct flight paths. The presented IC tracks heading by measuring solar angle-of-incidence (AOI) at fixed sampling rate using a novel, direct-to-digital method that is well-tailored to the unique power regime imposed by the on-chip photovoltaics (PVs). This AOI data is stored in an on-chip memory and is

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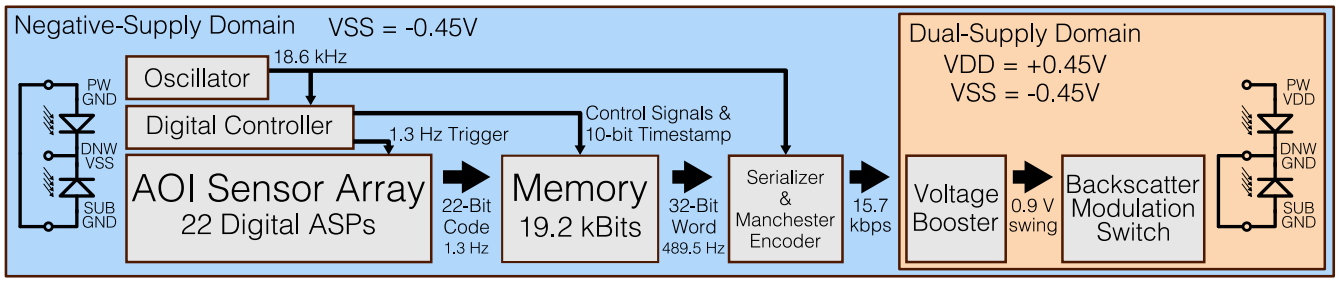

Fig. 2. Top-level system diagram with triple-well diode connections used to generate each supply level. Separate triple wells allow dual supplies.

uploaded via inductive backscatter to a base station upon reentry to the hive, and is then processed off-chip to reconstruct the flight path. The presented chip integrates almost all functions needed to perform bee flight tracking; the backscatter coil and resonant capacitor are the only off-chip components. A system block diagram is shown in Fig. 2.

II. System Description

A. Integrated Photovoltaics

Bee tracking tags must be very small and lightweight. In order to minimize form factor and permit continuous, autonomous power harvesting, integrated PV cells are used as the system power supply in place of a more conventional off-chip PV cell or battery. At the testing location of Ithaca, NY, insolation can range from 20 W/m^2 in shaded environments, such as in the woods or in the shadow of buildings, up to 1100 W/m^2 in unobstructed, midday sunlight. The power available from the integrated PV cells can thus vary widely throughout the course of a measured flight, especially if the honey bee passes under trees or if there is periodic cloud cover. The circuitry must tolerate this large range of operating conditions without losing stored data or significantly changing AOI sampling rate, specifically supply voltages in the range of 0.40-0.50 V and short-circuit currents of 3-200 μA for the 1.47 mm^2 core PV cell in use. To prevent disruptive supply droops, system average current consumption must always be kept below the minimum-insolation current of 3 μA.

Two PV cells are used in order to generate two supply domains. These PV cells are made from the two diodes present in the standard triple-well structure, which features a p-well (PW) enclosed by a deep n-well (DNW) that is buried in the p-type substrate (SUB). These diodes can be configured to bias above or below the grounded substrate when illuminated. The core PV cell is configured to provide a VSS through connection of the triple well as shown on the left side of Fig. 2. A secondary PV cell providing a VDD, shown on the right side of Fig. 2, is used to generate a dual-supply domain, which allows the voltage booster to increase voltage drive of the backscatter modulation switch.

B. Direct-to-Digital Detection of Solar AOI

When a low, unreliable supply voltage is used, analog circuitry should be minimized and digitization should occur as early as possible to avoid corruption of data by supply fluctuations. Integrated AOI sensors have been demonstrated previously [9], [10], but these designs require pixels with conventional analog readout chains and ADCs, which are difficult to implement under the power budget and voltage headroom available from an integrated PV cell.

To circumvent difficult low-voltage analog and mixed-signal design, we demonstrate a direct-to-digital AOI sensor that digitizes in-pixel. The sensor is based on Angle-Sensitive Pixels (ASPs, [10]), which exhibit a sinusoidal sensitivity to changes in AOI along the sensitivity axis of the pixel. This sinusoidal sensitivity provides an opportunity to exchange pixel count for a simplified digitization path. The output voltage of a single ASP can be digitized immediately through comparison to the output voltage of a second ASP with a complementary angular response (Fig. 3a). A pair of compared ASPs forms a differential 1-bit ADC that we term a Digital ASP (DASP). The sinusoidal angular sensitivity of an ASP is thus converted to the square-wave sensitivity of a DASP.

DASPs allow for reduced transistor count and current load on the PV cell by embedding a comparator inside the pixel structure. This is done by adding cross-coupled pull-down transistors that act as a latch (Fig. 3b). This mixed synchronous-asynchronous comparator resets when prompted by pulling both pixels to VSS, then releases the pixels and allows them to develop a forward bias under illumination. The comparator then asynchronously latches into a decision as soon as sufficient differential voltage has developed between the two complementary ASPs, thus eliminating the need for shutter length control, which is often required to account for variable light intensity in conventional pixel readout chains. Furthermore, while conventional asynchronous comparators can consume significant DC current once settled, the in-pixel comparator current is limited to the maximum current drawn by the pixel photodiodes. This current will necessarily be less than the photocurrent available from the much larger PV photodiode, thus protecting against supply droops.

A 1-bit encoding of AOI alone does not provide enough resolution for flight tracking, but if multiple DASPs are implemented in parallel, each exhibiting a different angular frequency β and/or phase offset α, then a multi-bit encoding of the incidence angle can be constructed (Fig. 4). Through choice of these DASP parameters, various angle encoding schemes can be realized. An efficient and robust encoding can be achieved using a Gray code, in which only one bit switches at a time. An array of $(N-1)$ cosine-based DASPs satisfying

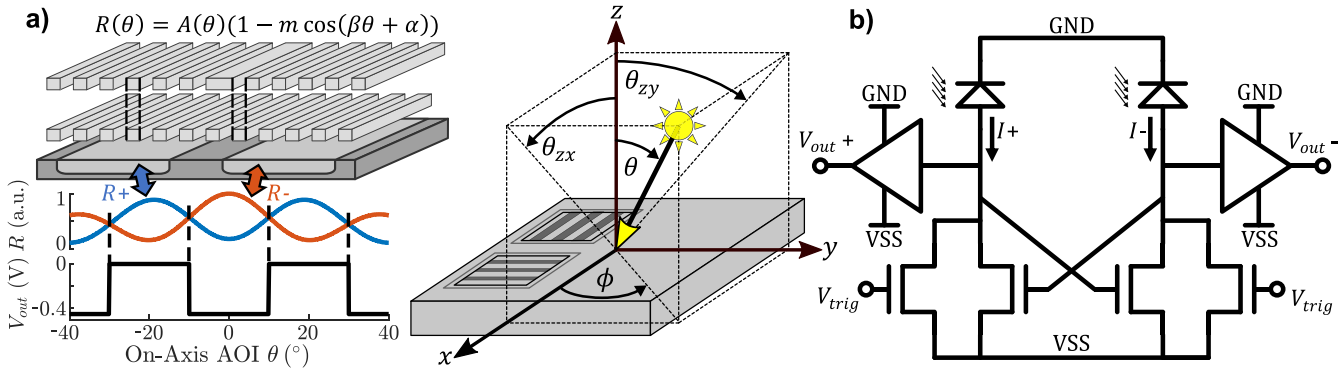

Fig. 3. a) Stacked gratings admit variable light intensity that depends on AOI, producing sinusoidal response as on-axis AOI is swept. The frequency β and phase α can be chosen by changing grating frequency, vertical offset, and phase offset. Comparison of complementary ASP responses produces square-wave DASP response. DASPs can be oriented to give AOI sensitivity along any axis; in this work DASP arrays are oriented to measured angles θ_{zx} and θ_{zy}. b) Schematic of novel in-pixel comparator, in which pixel photocurrents are compared when V_{trig} goes high, giving low-power, direct-to-digital AOI capture.

$\beta_n = \beta_0/2^n$ for $n \in [0, N-2]$, in parallel with a DASP producing a Heaviside response, realizes an N-bit Gray code in which each DASP contributes one bit of AOI encoding.

Two core DASP arrays having $\beta \in \{3.5, 7, 14, 28\}$ and a Heaviside response were implemented with sensitivity axes parallel to the chip x-axis and y-axis, respectively. In addition, redundant DASPs were implemented having $\beta \in \{8, 16\}$ to increase resolution and reduce the chance of repeated codes due to process variation in DASP β-values. The DASPs at $\beta = 28$ and $\beta = 16$ were also implemented at various phase offsets in an effort to increase resolution. A total of 22 DASPs were implemented, with an expected average AOI detection resolution of $1.1° \pm 0.3°$ across the angular operating range of $[-60°, +60°]$, which is determined by the daytime solar elevation range at the latitude of the test location.

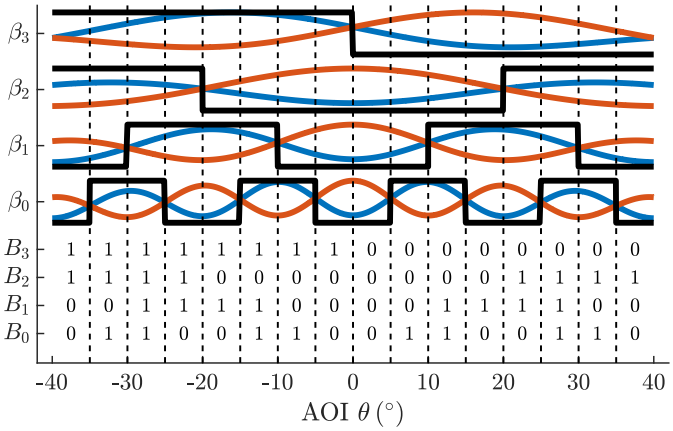

Fig. 4. An array of appropriately-chosen DASPs generates a Gray-encoding of incidence angle, represented as digital code $B = B_3B_2B_1B_0$, where bit B_n is contributed by ASP pair having frequency β_n.

C. Low-Voltage Clock, SRAM, and Wireless Communications

A frequency-stabilized ring oscillator serves as the system clock. Ring oscillators maintain function under aggressively scaled supply voltages, but suffer from increased sensitivity to their supply. To improve frequency stability under expected supply variation, the oscillator is starved by a PTAT current source (Fig. 5a). This current-limiter stabilizes oscillator frequency to 18.6 kHz ± 2.7% across supply variations of 0.45 ± 0.05V and limits jitter to 0.1%, sufficient frequency stability to allow accurate trajectory reconstruction. This clock rate allows complete upload of stored data in 1.2 seconds, enough time to upload from a bee crawling past the reader. The clock is divided down heavily to prompt AOI sampling at 1.3 Hz.

Since data upload cannot occur until the chip returns to the reader, an on-chip memory is required to store recorded angles during flight. Each sample generates a 32-bit word (22b angle encoding + 10b timestamp), and the memory can store 600 words, allowing 7 minutes and 41 seconds of continuous recording. To maximize robustness to supply variation and simplify system control, the memory read and write ports are separated. This separation is enabled by a 9T SRAM cell (Fig. 5b), which adds gated nFET readout buffers to the standard 6T topology [11]. This separation also allows the chip to continuously attempt to upload data, thus ensuring a data upload opportunity is never missed and removing the need for a prompt from the reader, simplifying system design. To ensure bees pass the reader one at a time, a narrow hive-entry tunnel can be used to force the bees to walk single-file past the reader, eliminating potential interference between tags.

For upload, the data is serialized and a 6-bit delimiter is added between each word. The bitstream is fed through a voltage booster (Fig. 5c) to increase the logic high level, then is used to switch a FET acting as a load-modulator to an off-chip PCB coil and resonant capacitor. The voltage booster is necessary to push the logic high level above the threshold voltage of the modulation FET, ensuring high contrast between the two impedance states. The off-chip coil is a 1-turn square loop that measures 3 mm on a side and resonates with a 6.8 pF off-chip capacitor at 775 MHz. The system is readable from 1.5 cm away.

D. Mitigation of Parasitic Light Sensitivity

Many circuit components contain pn-junctions, and if these diodes absorb light, photocurrent is generated and they will attempt to forward bias. With sufficient illumination, this parasitic light sensitivity can disrupt, or fully compromise, intended

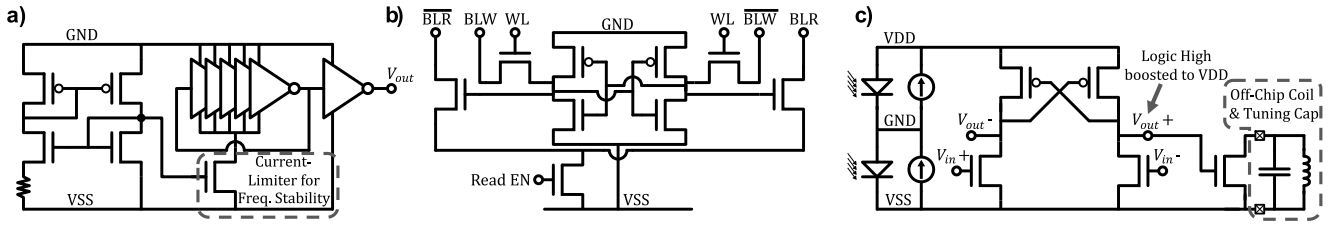

Fig. 5. PV-amenable support circuits. a) Low-voltage ring oscillator with frequency-stabilizing current limiter referenced to a PTAT. b) 9T SRAM cell for enhanced read stability and read/write port separation. c) Voltage booster to translate logic high level from GND to VDD using dual-supply PV cells.

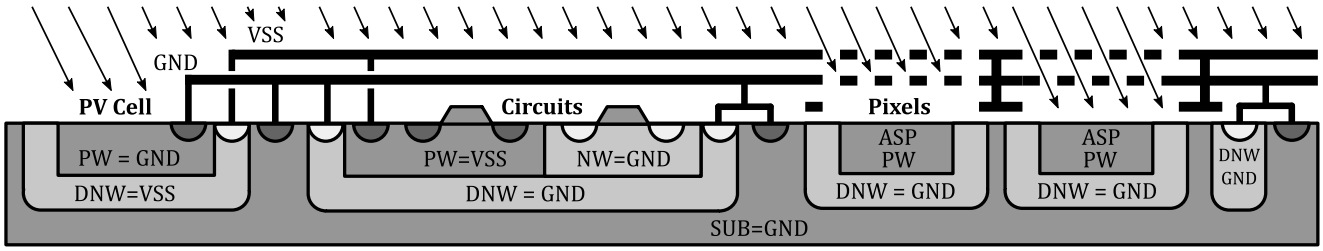

Fig. 6. Diodes and metal-stack light shielding used to protect circuits from light. Metal shielding blocks direct incidence of light on circuitry; backside DNW protects against lateral diffusion of carriers that can be generated in unshielded portions of the substrate. ASPs are intentionally exposed to light through gratings, and the backside shielding protects against laterally-diffused carriers which contain no AOI information and act as interference.

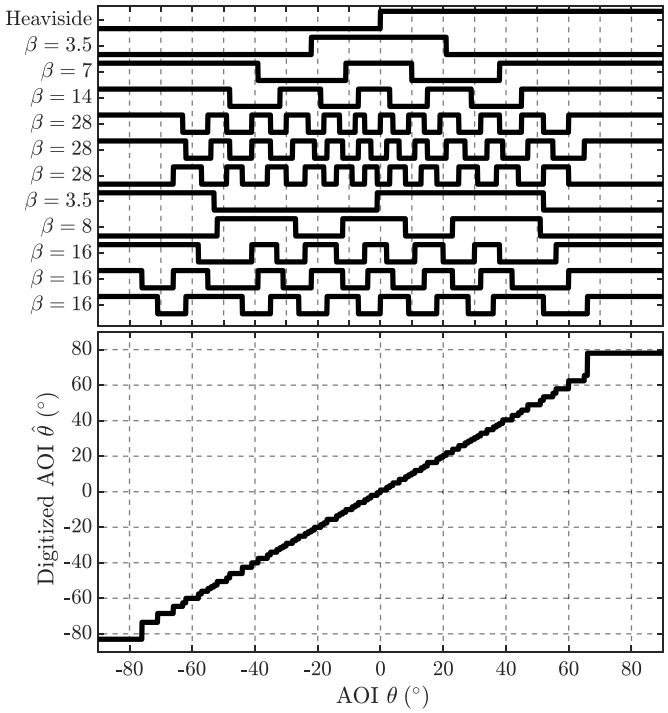

Fig. 7. Top: measured responses of x-axis DASP array. Notated β-values are average frequency across multiple periods. Bottom: AOI reconstruction from shown DASP array waveforms.

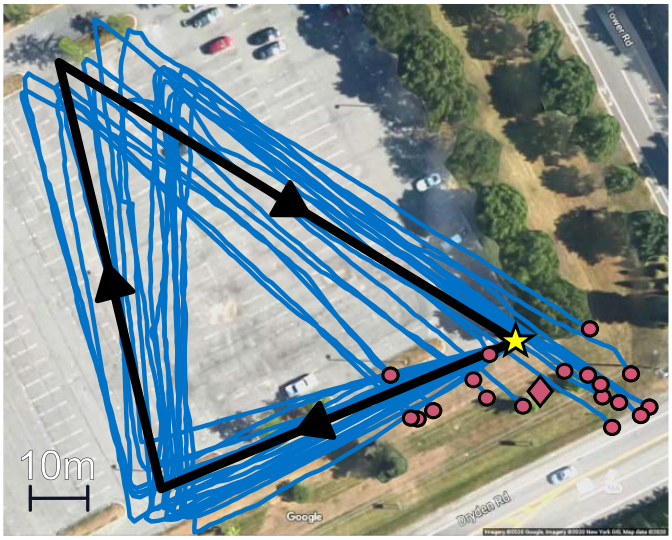

Fig. 8. Set of 18 measured trajectories taken at different times of day. Discretization errors change and tend to cancel out as the sun moves throughout the day. Red diamond indicates average final position, yellow star indicates true start and end position. The average final position is 9.6 m away from the true final position, a positional error 4.25% of the trajectory length.

circuit function [12]. To mitigate this, all non-optoelectronic circuits were placed under sheets of light-shielding metal. Where possible, routing was kept to the lower four metal layers, leaving the top two layers available for shielding. Since fabrication rules often require periodic slotting of large sheets of metal, it is necessary to use a two-layer shield with staggered slotting to fully protect the underlying silicon.

Even when using the above method, it is difficult to guarantee complete shielding of all circuits. Furthermore, light incident on exposed regions of silicon can generate charge carriers that can then diffuse laterally underneath the edge of any adjacent shielding into circuitry. To mitigate this, all circuits were surrounded by a triple-well with the DNW shorted to the substrate and PW biased to VSS (Fig. 6). The shorted outer diode blocks lateral diffusion of photo-generated carriers through the substrate, and additionally the PW provides appropriate nFET bulk biasing for negative supply operation.

III. Measured Results

The measured responses of the DASP array oriented along the chip x-axis are shown in Fig. 7. For AOI swept between

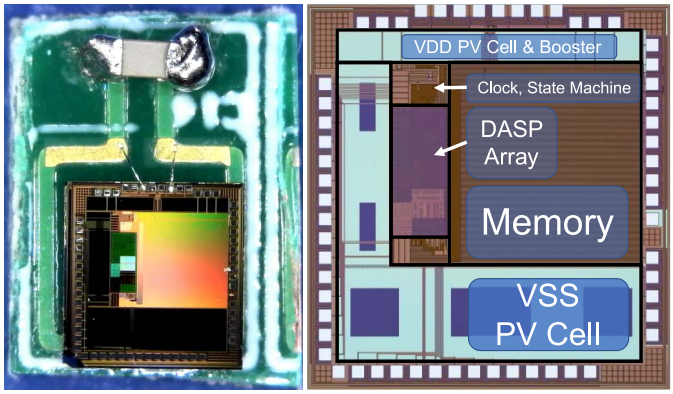

Fig. 9. Die-PCB assembly and Die Photo. The die measures 2.25 mm x 2.4 mm, and the PCB platform measures 4 mm x 5 mm. The complete assembly weighs 26 mg, 80% of which is constituted by the PCB. Downsizing the system is an area of future work.

$-60°$ and $+60°$ along the chip x- and y-axes, average resolution of $1.6° \pm 0.5°$ was measured, corresponding to heading resolution of $2.2° \pm 1.3°$ at solar elevation of 60°.

A hardware simulation of a bee flight was conducted (Fig. 8). The chip was walked in a triangular path around a parking lot at a speed of 1.4 m/s, which is slower than typical honey bee flight [8], but was more practical to achieve in our workspace and allows for an initial proof of concept. This trajectory is 226 m in length and was trialed 18 times across several different dates and times of day. This emulates multiple tagged honey bees from a hive performing routine flights to known food sources and returning to the hive. Solar AOI changes with time of day, and quantization errors thus tend to average out across many trials. Reconstructions were trialed with several subsets of the available sensors to compare performance and relative importance of each sensor. Best performance across all available data was obtained using only the core DASP arrays along each axis, which are constituted by the sensors having $\beta \in \{3.5, 7, 14, 28\}$ and a heaviside DASP; these are the reconstructions shown in this work.

The chip was implemented in bulk 180nm CMOS (Fig. 9). The PVs and circuitry are hard-wired on chip, precluding direct measurement of power consumption; in simulation the isolated circuitry consumes 95pW from a $+0.45$V source and 630nW from a -0.45V source.

IV. Conclusion

An autonomous IC integrating almost all necessary functionality to track bee flights has been demonstrated, and a simulated flight has been shown. A novel, integrated technology for flight tracking via direct-to-digital measurement of solar AOI has been demonstrated, and circuit topologies amenable to PV power have been presented. Finally, light-shielding techniques have been described.

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