

In another work Joseph et al. develop a SWIPT system that transmits using an amplifier and a 915 MHz oscillator [6]. The tag converts the received 915 MHz RF signal into DC with high power conversion efficiency (PCE) and utilizes

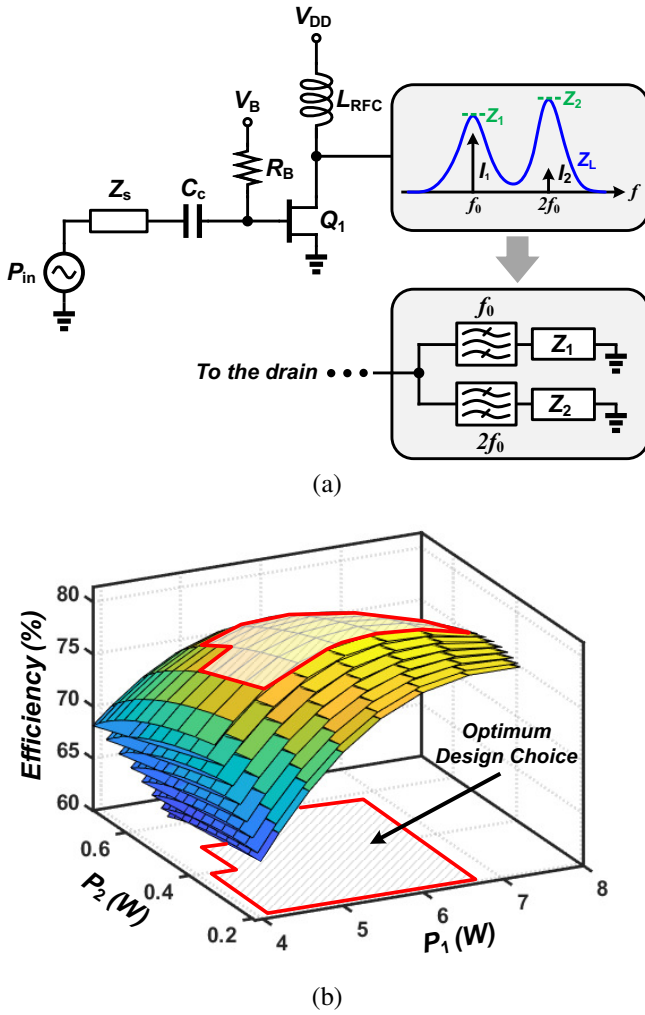


Fig. 3: (a) Conceptual schematic of the LP setup, and (b) the power level trade-off at fundamental and second harmonics.

the second harmonic generated by the rectifier at 1.83 GHz, as the feedback signal. As the tag generates its own carrier signal, it eliminates the need for the WP TX to synthesize and broadcast a separate frequency band to convey information. This lowers the DC power consumption of the transmitter. However, the carrier signal generated at the tag is weak and requires a receiver with high signal to noise ratio (SNR) at the base station. Kuo et al. also used the harmonics generated by a tag's rectifier to relay a signal back to the base station [7]. Their proposed tag receives three different tones at 883 MHz, 898 MHz, and 913 MHz, which are converted to DC and the intermodulation products generated are transmitted back to the base station. By receiving three different RF tones, more power is harvested by the tag. However, the base station contains three distinct frequency synthesizers. This consumes a significant amount of space and power.

To address the shortcomings of these works, this paper proposes a transmitter with a two tone oscillator to synthesize a high power RF signal at 2.4 GHz and at its second harmonic,

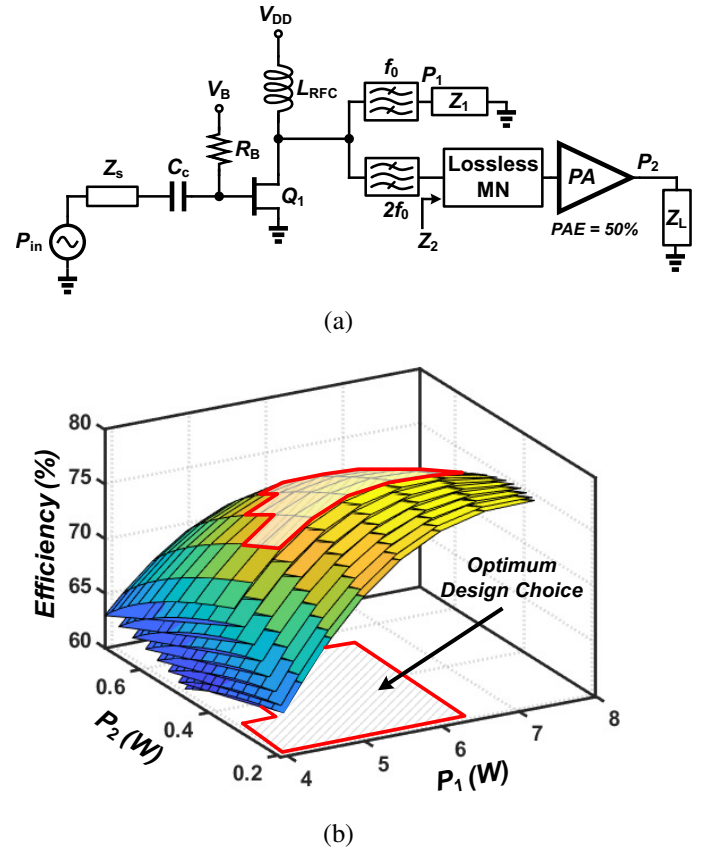


Fig. 4: (a) Conceptual schematic of the LP setup, and (b) the power level trade-off at fundamental and second harmonics, incorporating PA at $2f_0$.

4.8 GHz. Fig. 2 shows the potential application of the proposed transmitter. By transmitting two tones, the WP transmitter is able to provide different amounts of power to the tags, as the tags can be designed to receive a specific frequency. A tag tuned for both frequencies, f_0 and $2f_0$, receives more RF energy and the harmonic and intermodulation products from the tag rectifier can combine to generate a higher power carrier signal at f_{IM} . The high power carrier signal at the tag relaxes the receiver design requirements at the base station.

This paper is organized as follows. Section II explains the preliminaries, describing the theory behind the power transmitter. Section III presents the design methodology, and Section IV shows the simulation results. The paper is concluded in Section V.

II. PRELIMINARIES

Fig. 3 (a) shows the concept of the load-pull (LP) optimization of the gallium nitride (GaN) on silicon carbide (SiC) high electron mobility power transistor (HEMT). The load impedance must be designed to offer high impedance at fundamental (f_0) and second ($2f_0$) harmonics (i.e. Z_1 and Z_2 , respectively), in order to generate adequate amount of power at the two frequency bands. Further, the transistor is biased near the class AB operation region to generate sufficient drain current at $2f_0$ as well as f_0 . The source impedance is

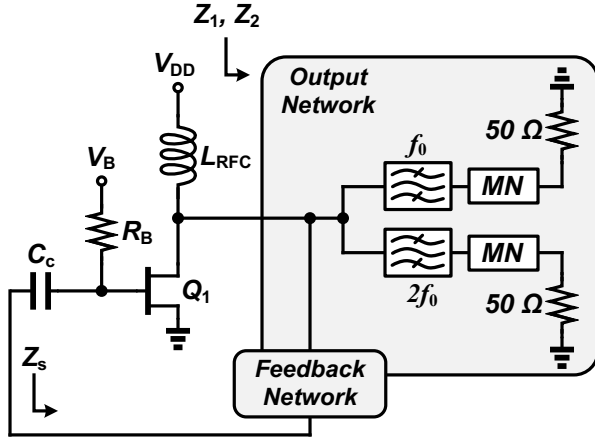


Fig. 5: Preliminary schematic of the proposed power oscillator.

also optimized to deliver maximum power to the gate of the transistor.

Fig. 3 (b) shows the DC to RF power efficiency, η , versus the generated power at fundamental and second harmonic using (1).

$$\eta = 100 \cdot \frac{P_1 + P_2}{P_{DC}} \quad (1)$$

where P_1 and P_2 are the RF power at the drain at f_0 and $2f_0$, respectively, and P_{DC} is the total DC power consumption. It can be seen that the maximum efficiency for a specific P_1 decreases by increasing P_2 . The shaded area on the plot corresponds to the region of maximum power efficiency that maintains sufficient P_1 and P_2 for most applications. Fig. 4 (a) shows a higher P_2 power can be achieved by adopting a power amplifier (PA) at the following stage to amplify P_2 .

Fig. 4 (b) shows the overall efficiency of the transistor incorporating the PA with a power added efficiency (PAE) of 50 %. The matching network and filters are assumed lossless. It can be seen that for a given increase in P_2 , there is a greater decrease in the efficiency for the circuit with a PA, than the one without a PA (see Fig. 3 (b)). This implies that the circuit with a PA has limited design choices toward maximizing the power efficiency, as noticed by comparing the shaded area in Fig. 3 (b) and Fig. 4 (b). Therefore the optimum design is more sensitive to the circuit components and can be affected by process, voltage and temperature (PVT) variations.

III. DESIGN METHODOLOGY

Fig. 5 shows the preliminary schematic of the proposed oscillator. The oscillator scheme is modified based on the harmonic-tuned topology which has been found to achieve high efficiency at high output power levels [8]–[10]. The output network along with the feedback network provide the required impedances at f_0 and $2f_0$ to maximize the power efficiency of the oscillator as shown in Fig. 3 (b). Further, the impedance looking into the feedback network from the

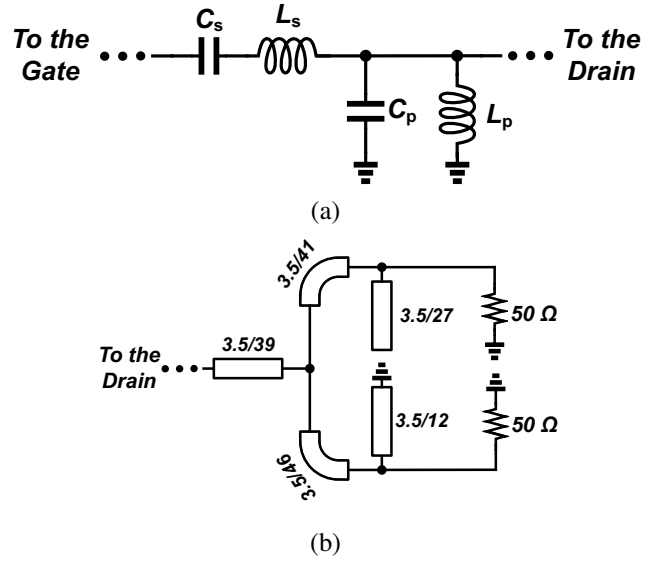


Fig. 6: (a) Schematic of the feedback network, and (b) the output network (width/length in mm).

gate of the transistor must be equal to the optimum source impedance from source-pull (SP) simulation. The feedback network should also meet the following conditions:

- 1) Provide excess phase at f_0 to satisfy the Barkhausen's phase criteria [11].
- 2) Filter out higher order harmonics except the fundamental.

Fig. 6 (a) shows the schematic of the feedback network. It is composed of a parallel and a series LC resonators. The series resistance of the inductors is assumed to be the dominant source of the loss of the feedback network (i.e. $Q_L \gg Q_C$). Although the quality factor of the discrete inductors is high enough to ignore the loss when compared with the loss of the output network, the quality factor of the inductors is set to the value of a typical integrated spiral inductors (i.e. $Q_{p,s} = 20$).

To split the power at two harmonics, the output network shown in Fig. 6 (b) is implemented as a diplexer tuned at f_0 and $2f_0$. It also matches the output impedances, $Z_{1,2}$ to the 50 Ω , the impedance of the antennas. The schematic of the diplexer is shown in Fig. 6 (b). It is implemented using microstrip transmission lines (TLs) on Rogers 4003C substrate. The electromagnetic (EM) simulation is performed for the output network using Keysight EEsof Momentum and its loss is obtained as 0.45 dB and 0.6 dB at first and second harmonics, respectively.

A GaN HEMT (Q_{VAR}), similar to Q_1 , with its source and drain connected is adopted to form a varactor. This enables the oscillation frequency to shift around the center frequency of 2.4 GHz and compensate for the process variations. Fig. 8 shows the characteristic of the varactor versus its control voltage, V_{VAR} . A capacitance variation of 4.5 - 9.0 pF is required to achieve a tuning range of 50 MHz ($\approx 2\%$) around the center frequency which is translated to the control voltage range of 1-3.5 V.

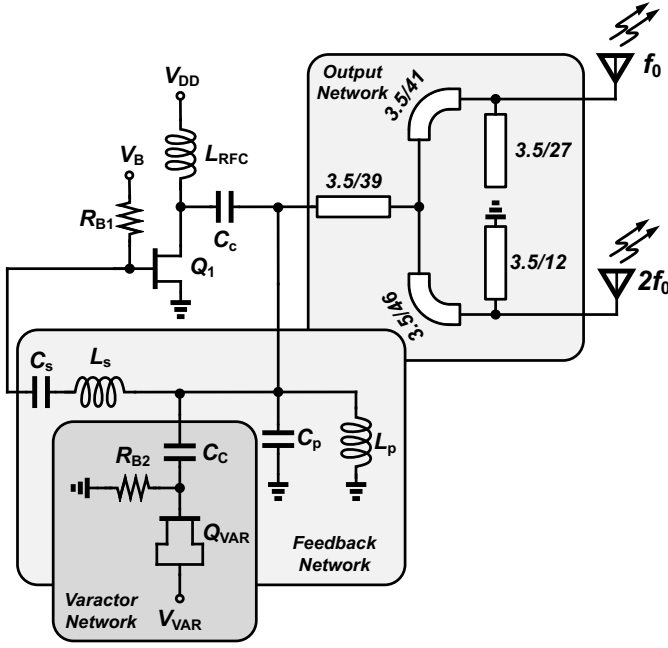


Fig. 7: Complete schematic of the proposed oscillator.

Hajimiri et al. showed that the phase noise of an electrical oscillator at an offset frequency of $\Delta\omega$ as follows [12]

$$L(\Delta\omega) = 10 \log_{10} \left[\frac{\sum F}{P_{RF}} \cdot \left(\frac{\omega_o}{\Delta\omega} \right)^2 \right] \quad (2)$$

where $\sum F$ is a function of the total effective noise generated by the circuit elements, ω_o is the oscillation frequency and P_{RF} is the output RF power. Since the power generated at fundamental is relatively large, a low phase noise level is expected at f_o . Simulation results show that the phase noise at second harmonic varies from -165.1 to -168 dBc/Hz over the tuning range at $\Delta\omega = 10$ MHz. This is an expected result since the input impedance of the output network is matched at the center frequency, and the power delivered to the antenna varies by drifting the oscillation frequency from its center frequency. Furthermore, by changing the bias voltage of the varactor, the amount of its contribution in the total noise (i.e. $\sum F$) changes and hence, the phase noise. It is noted that this phase noise is satisfactory for most applications even with a strict phase noise requirement.

The complete schematic of the proposed WP transmitter is shown in Fig. 7. GaN HEMTs are well suited for high power oscillators due to high breakdown voltages and high electron mobility. The Cree CGH40006P RF GaN HEMT is selected for the amplification device Q_1 and varactor Q_{VAR} [8], [13]–[15].

IV. SIMULATION RESULTS

The proposed oscillator was simulated in Keysight ADS using the large signal model for the GaN HEMT. The drain and the gate of the main transistor are biased at 28 V and -2.6

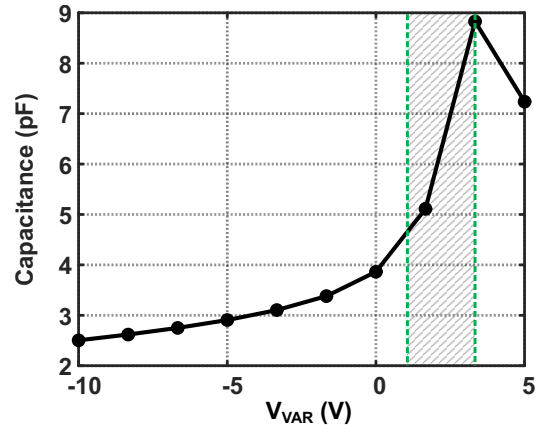


Fig. 8: Characteristic of the varactor.

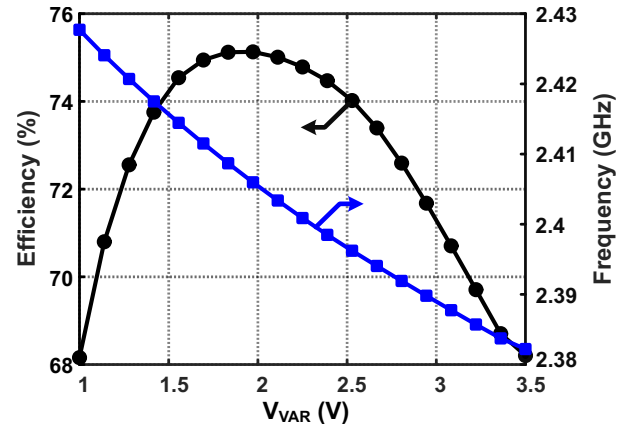


Fig. 9: Power efficiency and fundamental frequency of the oscillation versus V_{VAR} .

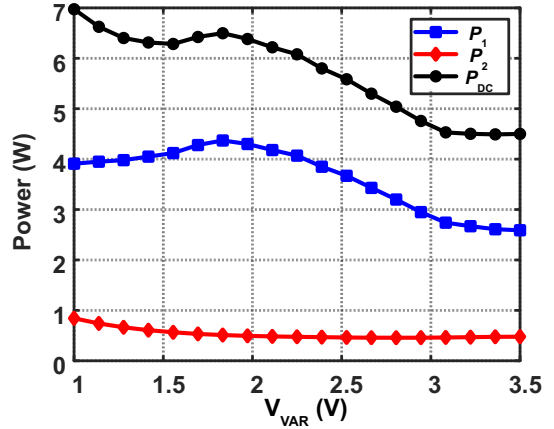


Fig. 10: Power generation at f_o and $2f_o$ and dc power dissipation versus V_{VAR} .

V, respectively. The oscillator draws a DC current of 230 mA at 2.4 GHz. Fig. 9 shows the power efficiency of the oscillator and its tuning frequency range versus the control voltage of the

varactor. It can be seen that the oscillator achieves a maximum DC to RF PCE of 75 %. This is lower than what the LP results in Section II, which can be attributed to the loss of the diplexer. As it is discussed earlier, the change in the oscillation frequency causes a variation in the delivered power to the antenna and hence, the power efficiency. It can be seen in the figure that this results a 7 dB of variation in the efficiency.

The DC power consumption and the RF output power at fundamental and second harmonics versus control voltage is represented in Fig. 10. The RF power at second harmonic, P_2 has the smallest variation over the frequency range, since it depends on the non-linearity of the main transistor and matching condition of the output network. On the other hand, the power, P_1 at the fundamental depends on of the feedback network in addition to the transistor non-linearity and matching condition of the output network. The variation of P_1 is 2.3 dB over the entire tuning range while it is 1.8 dB for P_2 .

Table I compares the performance of the proposed SWIPT scheme to prior works. To the authors best knowledge, this is the first work that presents a multitone WP TX that is optimized for high efficiency. The generated second harmonic signal can be used as an information signal (IF) separate from the wireless power frequency, and unlike [4], it does not require an additional oscillator. A 7.2 GHz IF signal, as a result of the transmitted f_o and $2f_o$ frequencies, could also be generated by utilizing the intermodulation and harmonic components of the tags rectifier, similar to [6]. It is noted that, [9] and [10] present high power oscillators that are suitable for WPT, but the method is unable to synthesize an information signal.

The figure of merit (FoM) of the oscillators noted in Table I can be computed from [16]

$$FoM = -10 \log_{10} \left[L(\Delta\omega) \cdot P_{DC,mW} \cdot \left(\frac{\Delta\omega}{\omega_0} \right)^2 \right] \quad (3)$$

where $P_{DC,mW}$ is the DC power dissipation in mW.

TABLE I:
COMPARISON BETWEEN SIMILAR WORKS

Work	TX Freq (GHz)	IF Freq (GHz)	TX P_{out} (W)	Max TX PCE (%)	PN ^a (dBc /Hz)	FoM (dBc /Hz)
[4]	5.8	3.6	1.2	NA	NA	NA
[6]	0.915	1.83	0.8	NA	NA	NA
[9]	2.45	NA	6.1	83	-118	167
[10]	0.980	NA	6.5	73	-123	183
This Work ^b	2.4/4.8	4.8/7.2	4/0.45	75 ^c	-128	182 ^d

^aPN is considered at a 100 kHz offset. ^bbased on simulation results.

^cTX PCE is total efficiency at two harmonics. ^dindicates FoM for 2.4 GHz.

CONCLUSION

In this paper, an oscillator for transmitting the fundamental and second harmonic frequencies is proposed. The transmitters ability to generate multiple frequencies at high output power makes the proposed system well suited for simultaneous wireless information and power transfer. The design procedure for optimizing the transmitter is presented, and the process is verified through simulation.

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