Temperature Effect on Performance of Enhancement Mode $Al_{0.4}Ga_{0.6}n$-Channel Moshfets with Hybrid Oxide

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ECS Meeting Abstracts, Volume MA2021-01, H01: Wide Bandgap Semiconductor Materials and Devices 22

Citation Shahab Mollah *et al* 2021 *Meet. Abstr.* **MA2021-01** 1071

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https://doi.org/10.1149/MA2021-01331071mtgabs

Abstract

The metal oxide semiconductor heterostructure field effect transistors (MOSHFETs) based on $Al_xGa_{1-x}N$ materials with the high aluminum composition is a promising choice for high-power, high-temperature harsh environment applications. In the present work the temperature stability of MOSHFETS with high-*k* ZrO_2, Al_2O_3 gate dielectrics has been studied. Our data show these high-*k* dielectrics introduce negative fixed charges (Q_{ox}) as high as 1-3×10^{13} cm^{-2} depleting 2DEG density of 2×10^{13} cm^{-2} causing a positive shift of

threshold voltage (V_{TH}) compared to that for HFET which is an important feature for realizing enhanced (E-) mode MOSHFET. ZrO_2 possesses higher Q_{ox} resulting in stronger positive V_{TH} shift in devices, while devices with Al_2O_3 demonstrate lower gate leakage. To take advantages of both oxides, UWBG $Al_{0.4}Ga_{0.6}N$ channel E-mode MOSHFET has been fabricated. E-mode device was realized using the hybrid oxide (ZrO_2/Al2O_3) combined with gate recess. To separate effects of dielectric charges and damage from recess process on device performance depletion (D-) mode and E-mode devices were fabricated on the same wafer simultaneously. D-mode devices were protected during gate recess step to avoid additional damage. Thermally induced V_{TH} instability of these MOSHFETs were studied and potential mechanism for this V_{TH} instability is discussed.

Experimental: Figure 1(a) shows the pseudomorphic device structure that was grown using metalorganic chemical vapor deposition on AlN/sapphire templates. A graded composition ($Al_xGa_{1-x}N$, x=1-0.4) back barrier reduces internal stress and improves gate control in the devices.[i], [ii] The top 200 Å thick graded n-$Al_xGa_{1-x}N$ (x from 0.6 to 0.3) layer assists with the formation of ohmic contacts resistance as low as 1.7 Ω-mm. The *n*-doping of this layer compensates the positive charges resulting from the reverse composition grading.[iii] The 2DEG sheet resistance was ~1900 ohm/□. Device processing details published elsewhere.[iv] The fixed gate-length $L_G \approx 2.0$ μm, source to drain spacing, L_{SD}=6 μm, were used for regular devices with 15 μm channel width, while for precise C(V,T,f) measurements we use a test structure with gate area 200x80 μm^2 .

Results and discussion: The combination of gate recessing and hybrid oxide resulted in threshold-voltage (V_{TH}) shift of +12.2 V from D to E-mode device (Figure 1(b)). The gate leakage current in both D and E-mode MOSHFETs is ~10^3 smaller than that of MOSHFETs using singe Al_2O_3 or ZrO_2 layer (Figure 2(a)) which allows us to apply gate voltage as high as +12 V. The peak DC currents for D and E-mode devices were found to be 1.1 A/mm and 0.48 A/mm respectively while in the pulse mode it was 1.3 A/mm and 0.53 A/mm. ON/OFF ratio as high as 3×10^8 was achieved which is higher than ~2 orders of magnitude than that for Al_2O_3 or ZrO_2. We then performed temperature dependent threshold and gate leakage study of our fabricated MOSHFETs. Figure 2(b) shows the temperature dependent

gate leakage characteristics of MOSHFETs of this study. It has been found that, in the D-mode MOSHFET, the V_{TH} experiences positive V_{TH} shift of + 1.7 V from RT to 150 °C; for the E-mode MOSHFET the shift is negative: -2.9 V (Figure 3(a)). The V_{TH} shift for similar device having Schottky gate (no dielectric) (HFET) is significantly smaller, +0.2 V. This shows that the V_{TH} shift is mainly due to the charges in dielectric or at dielectric-barrier interface. In the E-mode devices, the effective channel mobility and V_{TH} was additionally affected by radiative defects introduced during gate-recess step. The mobility (μ) in D-mode devices decreases with temperature while it increases for the E-mode devices. We estimated temperature dependent interface state density ($D_{IT}(T)$) and Q_{ox} (T) using frequency- dependent C-V measurements as shown in Figure 3(b). Our analysis show that in D-mode device, $Q_{ox}(T)$ dominates over interface charges. These are fixed negative charges which deplete the channel giving a total V_{TH} shift of +1.7 V from RT to 150°C. The extracted SS value for D and E-mode devices were 99 mV/decade and 134 mV/decade, indicating an increased density of interface traps (D_{IT}) at the recessed interface in the E-mode device. Larger D_{IT} value in E-mode devices caused by a radiation damage from the barrier recessing process and becomes comparable with Q_{ox}. Thus the temperature effect on Q_{ox} is compensated by D_{IT} changes, increasing SS and making the $V_{TH}(T)$ more negative.

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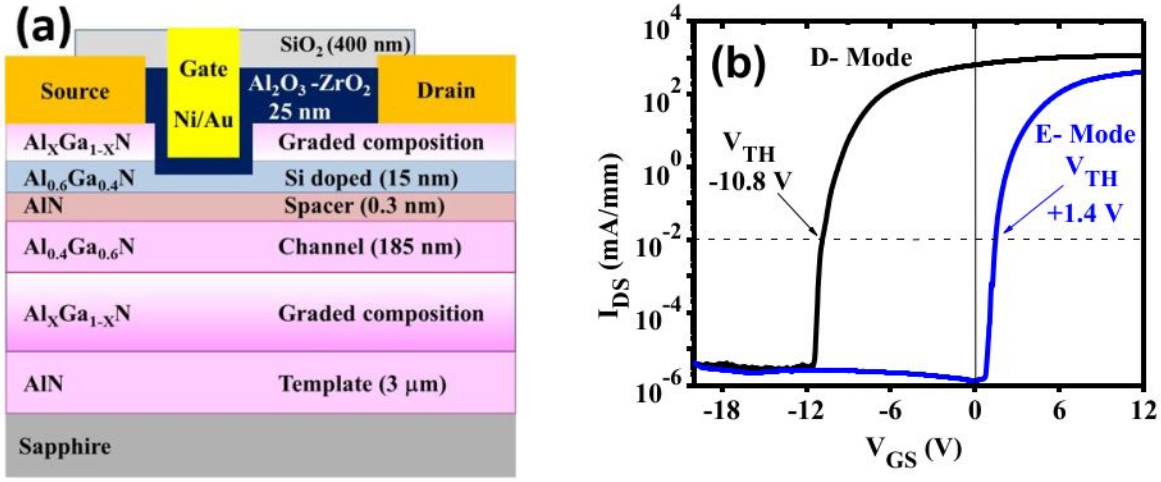

FIG. 1. (a) Schematic of the E-mode MOSHFETs. (b) Semi-log transfer characteristics for the D-mode and the E-mode devices. The threshold shift in E-mode device with respect to D mode device is 12.2 V.

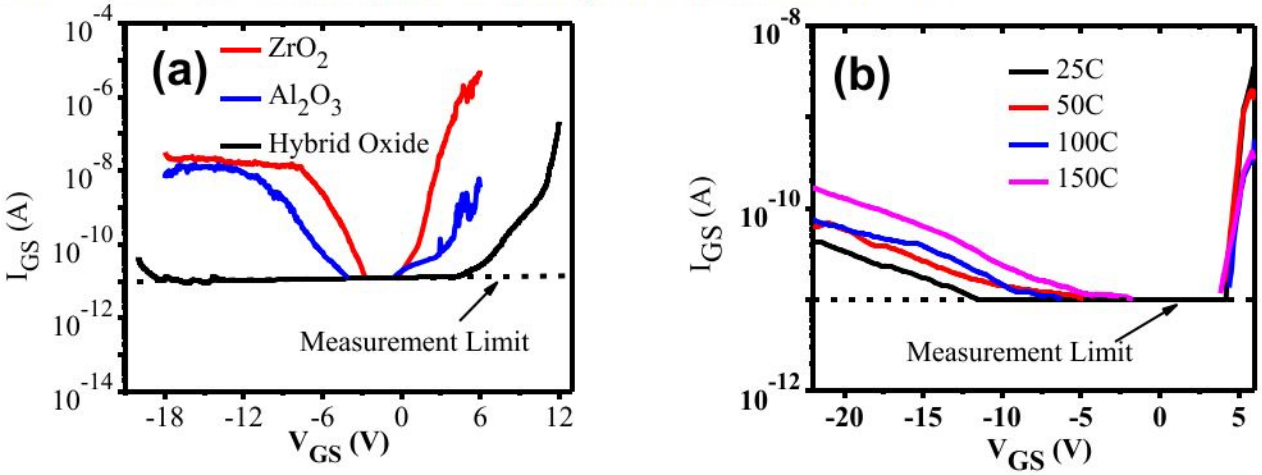

FIG. 2. (a) (a) Comparison of gate leakage current for ZrO_2, Al_2O_3 and hybrid oxide. (b) Temperature dependence of gate leakage current for $Al_{0.4}Ga_{0.6}N$ channel MOSHFETs.

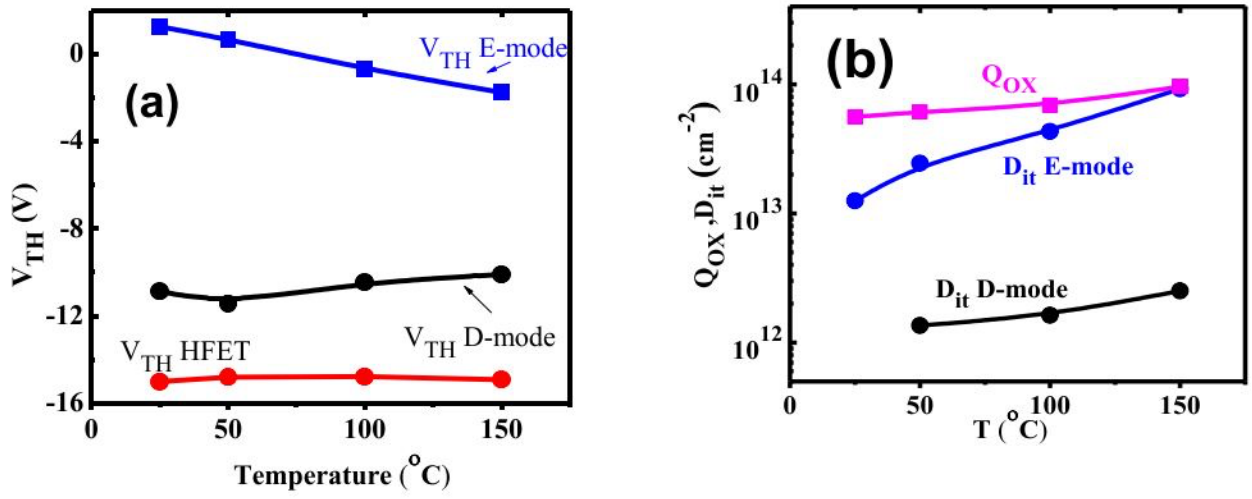

FIG.3. (a) Temperature-dependent threshold voltages for D- and E-mode devices. The V_{TH} shifts from RT to 150^{O} C are -2.9 V for E-mode and + 1.7 V for D-mode MOSHFETs; For comparison, the V_{TH} shift of +0.2 V for Schottky-gate D-mode HFET is also shown. (b)Temperature dependence of interface state density (D_{it}) and oxide charge (Q_{ox})

Figure 1

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