Tri-Gate GaN Junction HEMTs: Physics and Performance Space

Yunwei Ma, Ming Xiao, Zhonghao Du, Han Wang, *Senior Member, IEEE*, and Yuhao Zhang, *Member, IEEE*

***Abstract*— We present the physics and performance space of the tri-gate GaN junction high-electron-mobility transistor (Tri-JHEMT), a new tri-gate GaN device proposed recently. In Tri-JHEMTs, p-n junctions wrap around two-dimensional-electron-gas (2DEG) fins in the gate region. Our fabricated Tri-JHEMT demonstrates, for the first time, the kilovolt blocking capability at 150 ºC in all tri-gate GaN HEMTs. 3-D TCAD simulations were then calibrated with experimental devices and used to study p-GaN-based Tri-JHEMTs with various design parameters for a direct comparison with the industrial planar p-gate GaN HEMTs. Owing to the unique physics of the sidewall p-GaN/2DEG junction, the 2DEG distribution in junction tri-gates is very different from that in conventional tri-gates, enabling smaller gate capacitance and superior gate controllability. As a result, a lower resistance in the gated channel, a higher wafer 2DEG density, and a scaled gate length can be concurrently realized in normally-off Tri-JHEMTs. GaN Tri-JHEMTs designed for a wide range of voltage classes (15~1200 V) are predicted to enable a 15~75% lower on-resistance (R_{ON}), 3~10-fold smaller R_{ON}·Q_G (gate charge), and 45~63% smaller R_{ON}·Q_{OSS} (output charge) as compared to similarly-rated planar p-gate HEMTs. Considering their fabrication compatibility with existing foundry process, Tri-JHEMTs show great potentials as the next-generation lateral GaN power switches.**

***Index Terms*— Gallium nitride, HEMT, power electronics, p-GaN, Tri-gate, FinFETs, on-resistance, gate charges, p-n junction**

I. Introduction

The GaN high electron mobility transistor (HEMT) has been commercialized as a power device superior to Si in the voltage classes from 15 V to 650 V [1], [2]. The lateral GaN HEMT is intrinsically normally-on. Most of commercial enhancement-mode (E-mode) HEMTs (except for the composite devices like cascode and direct-drive) reply on a planar p-GaN gate.

Recently, some 3-D gate stacks, such as FinFET and tri-gate structures, have been introduced to lateral GaN HEMTs and vertical GaN FETs. These devices have been reviewed in [3], [4]. They can realize superior gate controllability and E-mode operation with a higher current on/off ratio and lower gated channel resistance as compared to the planar counterparts. The state of the arts include the large-area vertical GaN FinFETs [5]–[8] and multi-channel tri-gate HEMTs [9]. All of them show a breakdown voltage (BV) of >1.2 kV and a specific on-resistance (R_{ON}) lower than similarly-rated Si and SiC devices.

The first tri-gate GaN HEMT uses a Schottky stack [10], [11]; later, the metal-insulator-semiconductor (MIS) gate stack has become a more popular tri-gate of choice [12]–[15]. Despite excellent performance, some challenges of tri-gate GaN MIS-HEMTs (Tri-MISHEMTs) make their commercialization very slow. First, the E-mode realization requires very narrow fins or an additional AlGaN recess [3]. For example, 15-nm fins were used to make multi-channel E-mode Tri-MISHEMTs [9]. By contrast, most of today's industrial power device manufacturing rely on the 180-nm-node process; even the high-end GaN RF device manufacturing rarely goes below 60-90 nm. Second, the MIS tri-gate produces parasitic MIS channels and interface traps at the fin sidewalls, which increase the gate charge and induce high-temperature instabilities [16]. To date, there has been no reports of a high BV at 150 ºC in GaN Tri-MISHEMTs, while this is required for any commercial power device.

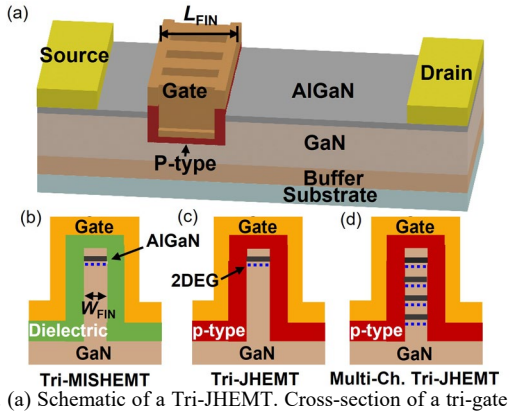

Fig. 1. (a) Schematic of a Tri-JHEMT. Cross-section of a tri-gate fin in the (b) Tri-MISHEMT, (c) Tri-JHEMT, and (d) multi-channel Tri-JHEMT.

Recently, we proposed a new type of tri-gate HEMTs, the tri-gate junction HEMT (Tri-JHEMT), in which the p-n junction wraps around the AlGaN/GaN fins in the gate region [17]. Fig. 1 illustrates the Tri-JHEMT and Tri-MISHEMT structures. As compared to the MIS tri-gate, the junction tri-gate allows stronger depletion, thus relaxing the lithography requirement to realize the E-mode operation and avoiding the punch-through at high drain biases (V_D). Tri-JHEMTs also obviate the sidewall MIS channel and minimize the sidewall trapping. In [17], a GaN Tri-JHEMT was fabricated using the p-type nickel oxide (NiO), which demonstrated many benefits of the Tri-JHEMT concept. Moreover, in this work, we show that these fabricated Tri-JHEMTs have a BV close to 2 kV at 150 ºC. This high-temperature BV was not reported in [17], and shows the true viability of GaN Tri-JHEMTs for industrial applications.

This work aims at comprehensively studying the physics and performance space of GaN Tri-JHEMTs in comparison with the

Y. Ma and M. Xiao contributed equally to this work.

Y. Ma, M. Xiao, and Y. Zhang are with the Center of Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24060 USA (e-mail: yhzhang@vt.edu).

Z. Du and H. Wang are with the Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, California 90086, USA.

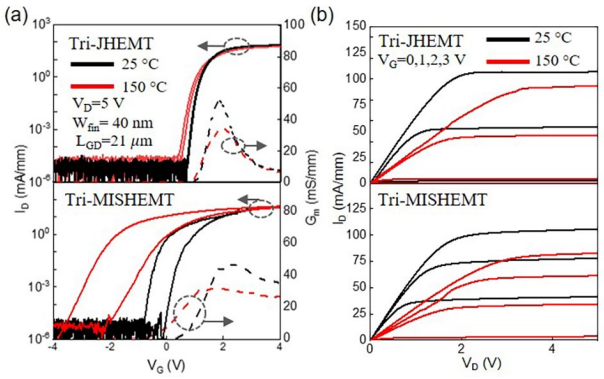

Fig. 2. (a) Double-sweep transfer and transconductance characteristics and (b) output characteristics of the Tri-JHEMT and Tri-MISHEMT at 25 ºC and 150 ºC. Both devices have a 40-nm W_{FIN} and 21-μm L_{GD}.

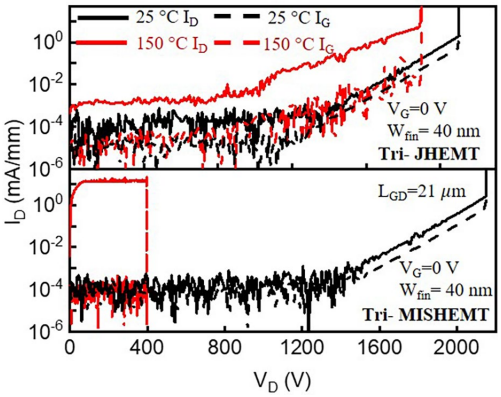

Fig. 3. Off-state I_D-V_D and I_G-V_D characteristics of (top) Tri-JHEMTs and (bottom) Tri-MISHEMTs at 25 °C and 150 °C with V_G = 0 V.

commercial planar p-gate HEMTs. For this, we propose a p-GaN based Tri-JHEMT from three considerations. First, the built-in potential (ϕ_{bi}) of the p-GaN/2DEG junction (~3 V [18]) is higher than that of the p-NiO/2DEG junction (~1.3 V [17]), making it easier to realize the E-mode and allowing a larger headroom for gate voltage (V_G) operation. Second, the p-GaN gate on a planar or recessed AlGaN barrier [19] is an industrial foundry process; high-quality p-GaN/2DEG junctions have also been demonstrated recently [18]. These suggest the feasibility of the industrial manufacturing of Tri-JHEMTs. Third, p-GaN Tri-JHEMT allows a direct comparison with the commercial p-gate HEMTs, thus unveiling the benefits brought by the new device design instead of different p-type materials.

3-D TCAD simulation is employed in this work to traverse a large design space for the p-GaN-based Tri-JHEMT (e.g., fin width, 2DEG density). The simulation models are calibrated with the experimental characteristics of the fabricated p-NiO-based Tri-JHEMTs. This paper is organized as follows. Section II presents the experimental characteristics of p-NiO-based Tri-JHEMTs, highlighting those at 150 ºC. Section III describes the 3-D TCAD simulation models. Subsequently, section IV probes the trade-offs between threshold voltage (V_{TH}) and R_{ON}, section V analyzes the gate capacitances and 2DEG distributions, and section VI analyzes the gate scaling. Section VII compares the performance space of Tri-JHEMTs, Tri-MISHEMTs and planar p-gate HEMTs. Section VIII concludes the paper.

II. Experimental Demonstration

The NiO-based Tri-JHEMTs and Tri-MISHEMTs (15-nm Al_2O_3 as the gate dielectrics) were fabricated on an industrial 6-inch GaN-on-Si wafer from Enkris Semiconductor, with the wafer structure and fabrication process detailed in [17]. The 2DEG density and sheet resistance are 8.5×10^{12} cm^2 and 480 Ω/sq, respectively. The hole concentration in NiO is over 10^{19} cm^{-3}. Fig. 2 shows the transfer and output characteristics of Tri-JHEMTs and Tri-MISHEMTs at 25 °C and 150 °C. Both devices have a 21-μm gate-to-drain distance (L_{GD}), 1-μm fin length (L_{Fin}), 40 nm fin-width (W_{fin}), and 150 nm fin spacing. Tri-JHEMTs show a very small hysteresis and a V_{TH} shift of only -0.19 V at 150 °C. By contrast, Tri-MISHEMTs show a large hysteresis and V_{TH} shift (-2.5 V) at 150 °C. Both devices show a similar R_{ON} increase by about 2-fold at 150 °C.

Fig. 3 shows the off-state I-V characteristics of Tri-JHEMTs and Tri-MISHEMTs at 25 °C and 150 °C, with the substrate floating and V_G = 0 V. Both devices show a similar BV ~ 2 kV at 25 ºC. At 150 ºC, Tri-JHEMTs retain a BV over 1.9 kV with a drain leakage current (I_D) about 10-100 times higher than that at 25 ºC. This I_D increase is smaller than that in commercial p-gate GaN HEMTs [20]. At 150 ºC, Tri-MISHEMTs punch through, as featured by a much higher I_D but a low gate leakage current (I_G). This punch through is due to the reduced potential barrier in the AlGaN/GaN fins [17], [20], which is attributable to the more pronounced interface trapping and the resulted gate control weakening at 150 ºC. With the substrate grounded, at 25 ºC, both devices show a BV of ~1.3 kV limited by the vertical leakage current, while the Tri-MISHEMT still shows the punch through at 150 ºC and V_G = 0 V.

To date, our Tri-JHEMTs, for the first time, demonstrate the kilovolt blocking capabilities at 150 ºC in tri-gate GaN HEMTs. This is attributable to a superior and more thermally stable gate controllability in the Tri-JHEMT.

III. 3-D Simulation Model

Physics-based 3D TCAD simulation is performed in Silvaco Atlas for Tri-JHEMTs and Tri-MISHEMTs. A planar p-gate HEMT, i.e., a gate injection transistor (GIT) with no barrier recess, is simulated as a reference device. For tri-gate devices, 3-D simulation is conducted in a single-fin unit-cell (Fig. 4). The p-GaN-based Tri-JHEMT concept applies to both the Ohmic- and Schottky-type gates, which are the two contacts used in commercial planar p-gate HEMTs [21]. In this work, we simulate the Ohmic-type Tri-JHEMT as a showcase, and the revealed design and performance are expected to be also applicable to Schottky-type Tri-JHEMTs.

The main simulation parameters are listed in TABLE I. The acceptor concentration (N_A) and activation energy in p-GaN are determined via the 2-D simulation of a commercial GIT (with barrier recess) to match the datasheet V_{TH}. The commercial GIT cross-sectional geometry is extracted from [21].

For tri-gate device simulations, the relation between fin width (W_{FIN}) and the 2DEG concentration in the fin region at zero biases (n_{FIN}) is critical. n_{FIN} decreases with W_{FIN} due to the piezoelectric stress release [22] and sidewall surface states [23]. While a physics-based model is not available, we calibrate the W_{FIN} ~ n_{FIN} relation using the experimental V_{TH} data of our fabricated NiO-based Tri-JHEMTs. As shown in Fig. 5(a), n_{FIN}

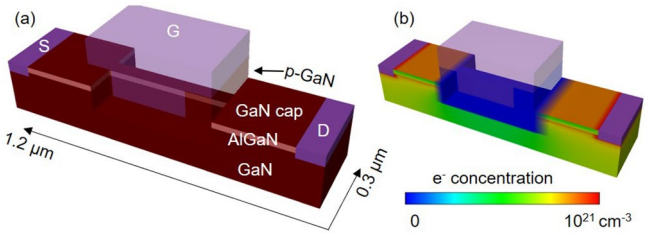

Fig. 4. (a) 3-D schematic of the simulated unit-cell of a p-GaN-based Tri-JHEMT. (b) Simulated electron concentration distribution at zero biases.

TABLE I. Main Simulation Parameters

Symbol	Quantity	Values
L_{GD}	Gate-to-drain distance	0.2 to 21 μm
L_{SD}	Source-to-drain distance	0.2 μm
L_G	Gate length	0.5 to 0.1 μm
t_{cap}	GaN cap thickness	3 nm
$t_{barrier}$	AlGaN barrier thickness	22 nm
t_{FIN}	Fin height	75 nm
W_{FIN}	Fin width	40 to 300 nm
$W_{spacing}$	Fin spacing	= W_{FIN}
L_{FIN}	Fin length	0.5 to 0.1 μm
t_{pGaN}	p-GaN thickness	100 nm
t_{AlO}	Al_2O_3 thickness	15 nm
t_{sub}	Substrate thickness	150 μm
R_c	Contact resistance	0.1 Ω·mm
N_A	P-GaN acceptor concentration	2×10^{19} cm^{-3}
E_A	P-GaN acceptor energy	0.16 eV
n_{2DEG}	Wafer 2DEG concentration	3×10^{12} to 2×10^{13} cm^{-2}

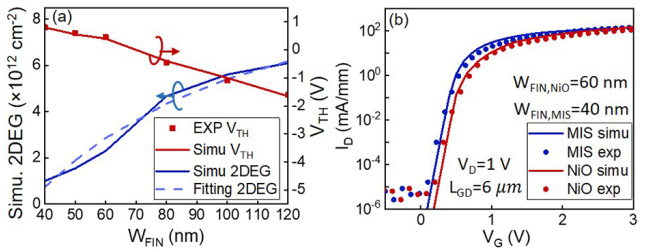

Fig. 5. (a) Derivation of the n_{FIN} *v.s.* W_{FIN} relation through matching the simulated V_{TH} with experimental values, as well as the calibration of an empirical model. (b) Comparison of the experimental and simulated transfer curves of a Tri-MISHEMT and a NiO-based Tri-JHEMT.

was adjusted for different W_{FIN} in simulations to ensure that the simulated V_{TH} matches experimental data. The calibrated n_{FIN} is then empirically fit to the equation below, which is modified based on the empirical n_{FIN} models reported in [22], [24].

$$n_{FIN} = n_{2DEG}[1 - \alpha \cdot e^{-\frac{W_{FIN}}{\beta}} \cdot \left(1 + e^{-\frac{W_{FIN}}{\beta}}\right)] \quad (1)$$

where n_{2DEG} is the wafer 2DEG concentration; α and β are two fitting constants representing the degree of relaxation associated with W_{FIN}. Using $\alpha = 0.9$ and $\beta = 85\ nm$, the fitting matches the experimental and simulated V_{TH}. In the next few sections, this equation will be used to set n_{FIN} in the simulated p-GaN-based Tri-JHEMTs with different W_{FIN} and n_{2DEG}.

All other simulation models are based on our prior GaN FinFET and HEMT simulations [25]–[28]. Fig. 5(b) shows an accordance between the experimental and simulated transfer characteristics of the NiO Tri-JHEMT with 60 nm W_{FIN} and the Tri-MISHEMT with 40 nm W_{FIN}. Such an accordance has been achieved in Tri-JHEMTs and Tri-MISHEMTs with a wide range of W_{FIN}, validating our 3-D simulation models.

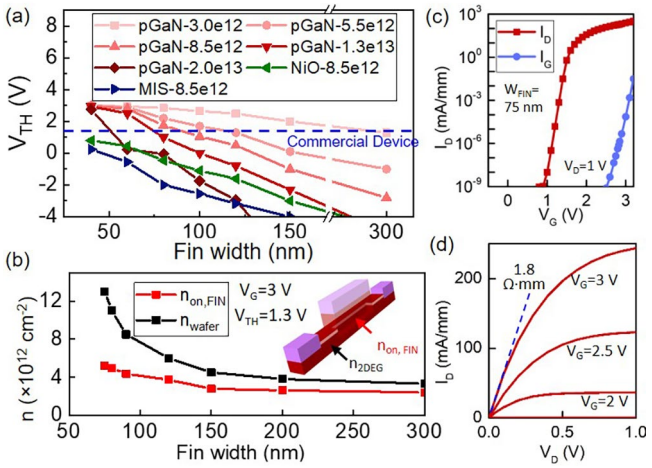

Fig. 6. (a) Simulated V_{TH} *v.s.* W_{FIN} for the p-GaN-based Tri-JHEMTs with various wafer n_{2DEG} (from low to high, pink to red) and the Tri-MISHEMTs and NiO-based Tri-JHEMTs. (b) Extracted n_{2DEG} and $\overline{n_{on,FIN}}$ (at V_G = 3 V) as a function of W_{FIN} in p-GaN-based Tri-HEMTs to enable V_{TH} = 1.3 V. Simulated (c) transfer and (d) output characteristics of a p-GaN-based Tri-JHEMT with W_{FIN} = 75 nm and L_{GD} = 0.2 μm (used for extracting R_{CH_G}).

IV. Threshold Voltage and On-Resistance

The first design consideration for any power tri-gate HEMT is the E-mode operation. Fig. 6(a) shows the simulated V_{TH} of Tri-JHEMTs (p-GaN- and NiO-based) and Tri-MISHEMTs as a function of W_{FIN} and n_{2DEG}. An n_{2DEG} range of 3×10^{12} to 2×10^{13} cm^{-2} is simulated for p-GaN-based Tri-JHEMTs. The lower end is close to the values in commercial E-mode power HEMTs, and the higher end can be realized in either a single 2DEG channel or a multi-channel structure [9], [29]–[31].

Benefitted from the high ϕ_{bi} and the absence of an insulating layer, the p-GaN-based Tri-JHEMT shows the highest V_{TH} in all types of tri-gate HEMTs. This in turns allows a higher n_{2DEG} in the wafer. For example, at W_{FIN} = 90 nm, V_{TH} of the p-GaN-based Tri-JHEMTs is ~1.3 V with an n_{2DEG} of 8.5×10^{12} cm^{-2}, which is 2-fold higher than the typical n_{2DEG} in a commercial p-GaN HEMT wafer. In Tri-JHEMTs with narrow fins, V_{TH} is dominated by sidewall depletion and converges at ϕ_{bi} (~ 3 V), allowing a high V_{TH} for wafers with an n_{2DEG} of 2×10^{13} cm^{-2}.

Note that, in Tri-MISHEMTs, V_{TH} can be raised by using a higher gate capacitance (e.g., thinner gate dielectric). However, it cannot increase indefinitely and will be limited by the ϕ_{bi} between the gate metal and 2DEG, which, regardless of gate metal, is very difficult to approach that of a GaN p-n junction.

To best accommodate GaN converter designs, we design the V_{TH} of Tri-JHEMTs to be 1.3 V, the V_{TH} of most commercial p-gate GaN HEMTs, and study the maximum n_{2DEG} as a function of W_{FIN} to realize this V_{TH}. Fig. 6(b) shows the n_{2DEG} and $\overline{n_{on,FIN}}$ as a function of W_{FIN} for p-GaN-based Tri-JHEMTs at V_G = 3 V, with an identical V_{TH} = 1.3 V. Here $\overline{n_{on,FIN}}$ is the average 2DEG concentration in the gated fin channel when the device is ON, extracted by averaging the simulated 2DEG profile in the fin across the entire gated fin length. Note $\overline{n_{on,FIN}}$ is different from n_{FIN} in Eqn. (1), as n_{FIN} corresponds to the zero-bias condition. $\overline{n_{on,FIN}}$ is determined by gate capacitance and gate overdrive, and it determines the gated channel

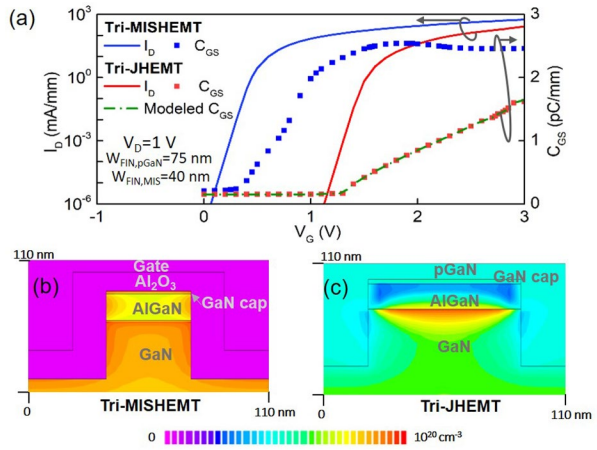

Fig. 7. (a) Simulated C_G-V_G and I_D-V_G characteristics of an E-mode Tri-JHEMT (W_{FIN} = 75 nm) and an E-mode Tri-MISHEMT (W_{FIN} = 40 nm), as well as the modeled C_G-V_G curve of the Tri-JHEMT. Simulated contours of electron concentration in a tri-gate fin in (b) Tri-MISHEMTs and (c) Tri-JHEMTs, both under V_G - V_{TH} = 1.7 V.

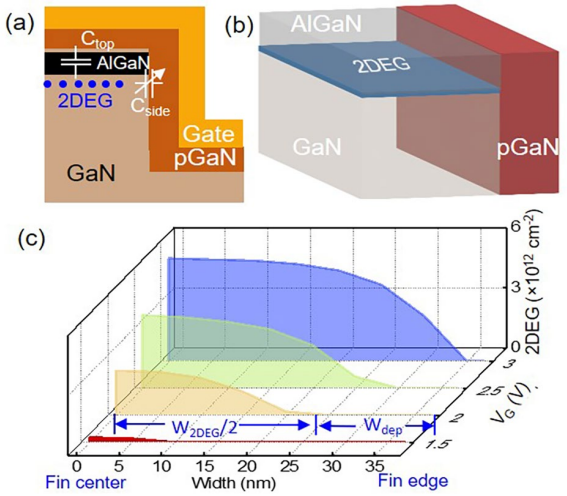

Fig. 8. Schematic of the (a) C_G components in a half-fin tri-gate unit-cell and (b) a sidewall p-GaN/2DEG junction. (c) Simulated 2DEG density profile in a half-fin unit-cell at V_G of 1.5, 2, 2.5, and 3 V. The W_{2DEG} and W_{dep} are illustrated in the 2DEG density profile at V_G = 2 V as an example.

resistance (R_{CH_G}); in comparison, n_{FIN} is material and geometry related and has no direct correlation to R_{CH_G}.

As shown in Fig. 6(b), for Tri-JHEMTs with V_{TH} = 1.3 V, a 75-nm W_{FIN} can accommodate a wafer n_{2DEG} of 1.3×10^{13} cm^{-3}. $\overline{n_{on,FIN}}$ increases with smaller W_{FIN} due to the enhanced gate control in the tri-gate, suggesting an increasingly lower R_{CH_G}. As both n_{2DEG} and $\overline{n_{on,FIN}}$ increases at smaller W_{FIN}, the R_{ON} can be increasingly reduced at the price of a more demanding lithography. Fig. 6(c) and (d) show the simulated transfer and output characteristics of the Tri-JHEMTs with 75-nm W_{FIN}, 0.2-μm L_{GD}, and 1.3×10^{13}-cm^{-3} n_{2DEG}, showing a gate turn-on voltage of 3.1 V extracted at I_G of 1 μA/mm. R_{ON} is 1.8 Ω·mm, and the R_{CH_G} is extracted to be 1.4 Ω·mm.

As shown in Fig. 6(a), our simulation predicts that the V_{TH} of Tri-MISHEMTs and NiO-based Tri-JHEMTs is difficult to reach 1.3 V for a wafer with 8.5×10^{12}-cm^{-3} n_{2DEG} and Ni gate metal, even when W_{FIN} is scaled to 30 nm. This is consistent with experimental reports of the NiO-based Tri-JHEMTs (V_{TH} ~ 1 V [17]) and industrial Tri-MISHEMTs (V_{TH} ~ 0 V [32]).

V. Gate Capacitance and Electron Distribution

The gate capacitance (C_G) of Tri-JHEMTs is expected to be lower than that of Tri-MISHEMTs due to the absence of sidewall and bottom MIS channels. Fig. 7(a) shows the simulated gate-to-source capacitance (C_{GS}) as a function of V_G for an E-mode Tri-JHEMT (75-nm W_{FIN}, 1.3×10^{13}-cm^{-3} n_{2DEG}) and an E-mode Tri-MISHEMT (40-nm W_{FIN}, 8.5×10^{12}-cm^{-3} n_{2DEG}). The C_{GS} of Tri-JHEMTs is much smaller at the same gate overdrive. This can be understood by scrutinizing the electron distribution in the tri-gate fins, which is simulated at V_G - V_{TH} = 1.7 V for both devices (Fig. 7(b) and (c)). In the Tri-MISHEMT, high-density electrons are present at the sidewall and bottom MIS channels; the 2DEG concentration peaks at the fin edge instead of the fin center. Note that the electron mobility at the fin edge or in the MIS channels is expected to be much lower than the planar 2DEG mobility, due to surface roughness and scattering. This suggests that the effective mobility in the MIS tri-gate region is much lower than the 2DEG mobility. The higher electron density brought by the tri-gate cannot be exploited to reduce R_{CH_G} and R_{ON} in Tri-MISHEMTs.

By contrast, as shown in Fig. 7(c), the junction tri-gate has no parasitic conduction paths, and the 2DEG density peaks at the center of the fin. Hence, the effective electron mobility in the junction tri-gate region is close to the wafer 2DEG mobility. Tri-JHEMTs thus present an ideal balance between the high on-state conductivity and the low gate capacitance/charge.

As the C_G of Tri-JHEMTs is fundamentally different from that in Tri-MISHEMTs or planar p-gate HEMTs, we built an analytical model to probe the underlying physics. Fig. 8(a) illustrates the C_G components in a half-cell junction-trigate fin, i.e., a sidewall p-GaN/2DEG junction capacitance (C_{side}) in parallel with a top MIS-like capacitance (C_{top}), which reflects the 2DEG modulation by the side- and top-gates, respectively. C_{top} is identical to the C_G of planar p-gate HEMTs; when the gate is Ohmic-type, it equals to a MIS capacitance with the AlGaN barrier as an effective insulator [33]. As W_{FIN} reduces, C_{side} gradually dominates over C_{top} in the junction tri-gate.

As shown in Fig. 8(b), unlike common bulk PN junctions, the sidewall p-GaN/2DEG junction is a 3D-2D junction, which usually has a longer depletion width that is linearly proportional to the applied bias instead of following the square root relation [34], [35]. Also, the depletion approximation does not hold in 3D-2D junctions; beyond the fully depleted region, a long tail of partially depleted space-charges is present [34]. This faster 2DEG depletion and additional depletion tails lead to smaller junction capacitances. Fig. 8(c) shows the simulated 2DEG concentration profile, i.e., $n_{on,FIN}(x)$, in a half-fin cell of a Tri-JHEMT with 75-nm W_{FIN} and 1.3×10^{13}-cm^{-3} n_{2DEG} [and 6.1×10^{12}-cm^{-3} n_{FIN} according to Eqn. (1)] at various V_G. $n_{on,FIN}(x)$ falls to zero in the full depletion region near the fin edge. It peaks at the fin center and is smaller than n_{FIN} at V_G up to 3 V, suggesting that the partial depletion tail of the p-GaN/2DEG junction has extended to the fin center.

To simplify the C_G modeling, we assume the p-GaN is highly doped so that all depletion occurs in 2DEG. This gives:

$$C_G = \frac{dQ_{2DEG}}{dV_G} = \frac{d(2L_{FIN} \cdot \int_0^{\frac{W_{2DEG}}{2}} n_{on,FIN}(x)dx)}{dV_G} \quad (2)$$

where the total width of 2DEG in a fin can be written as:

$$W_{2DEG}(V_G) = W_{FIN} - 2W_{dep}(V_G) \quad (3)$$

where W_{dep} is the width of the full depletion region adjacent to each fin sidewall, as illustrated in Fig. 8(c). According to [34], W_{dep} of an ideal 3D-2D p-n junction can be written as:

$$W_{dep}^{3D-2D} = \frac{\pi^2 \epsilon(\phi_{bi} - V_G)}{8Gqn_{FIN}} \quad (4)$$

where ϵ is the permittivity of GaN and G is the Catalan's constant. In the junction tri-gate, the top p-GaN gate also needs to be accounted for the 2DEG depletion. As C_{top} functions like a MIS capacitor, its 2DEG depletion is also proportional to $\phi_{bi} - V_G$. Thus, we approximate W_{dep} as

$$W_{dep}(V_G) \approx (1+\gamma)W_{dep}^{3D-2D} \quad (5)$$

where γ is a fitting factor to enable $W_{dep} \approx W_{FIN}/2$ at $V_G = V_{TH}$ (i.e., the 2DEG in the fin is fully depleted at $V_G \leq V_{TH}$). γ is found to be about 0.5 in our fitting.

After $V_G > V_{TH}$, the $n_{on,FIN}(x)$ distribution is impacted by the partial depletion tails of the 3D-2D junction. According to [35], [36], the partially depleted 2D carriers should follow a $1/y$ distribution, where y is the distance to the fully-depleted region, i.e., $y = W_{2DEG}/2 - x$. Let W_{tail} denote the y at which the depletion charge density falls to a fraction t (e.g., 10%) of its peak value. According to [35], W_{tail} is given by

$$W_{tail} = \frac{2\epsilon(\phi_{bi} - V_G)}{\pi t q n_{FIN}} \quad (6)$$

Based on the above $1/y$ distribution, the partial depletion charge density can be calculated and then subtracted from n_{FIN}, producing the $n_{on,FIN}(x)$ distribution:

$$n_{on,FIN}(x) = n_{FIN}\left(1 - \frac{\frac{tW_{tail}}{1-t}}{\frac{W_{2DEG}}{2} - x + \frac{tW_{tail}}{1-t}}\right) \quad (7)$$

The modeled W_{dep} and 2DEG distribution from Eqns. (4)-(7) agree with the simulation results in Fig. 8(c). Plugging Eqns. (3)-(7) into (2) and considering the filling factor (i.e., W_{Fin} over fin spacing), the modeled $C_G \sim V_G$ is plotted in Fig. 7(a), which also agrees with the simulation results. This verifies our models, and more importantly, reflects the critical impact of the sidewall p-GaN/2DEG junction on the C_G and electron distributions in Tri-JHEMTs. The unique properties of the 3D-2D junction, such as the wide and tailed depletion region, enable a strong depletion of the 2DEG in the tri-gate fins and thus a small C_G.

VI. Gate Control and Scaling

Gate controllability determines the short-channel effects and the gate length scaling capability. To compare the gate control in Tri-JHEMTs and Tri-MISHEMTs, the barrier height (Ψ_{Fin}), i.e., the local conduction band energy over fermi level, is extracted in the tri-gate fins. Fig. 9(a)-(b) show the simulated Ψ_{Fin} in tri-gate fins of an E-mode p-GaN Tri-JHEMT (75-nm W_{FIN}) and a Tri-MISHEMT (40-nm W_{FIN}), both with L_{FIN} = 500 nm and at V_G = 0 V and V_D = 1000 V. The lowest Ψ_{Fin} appears

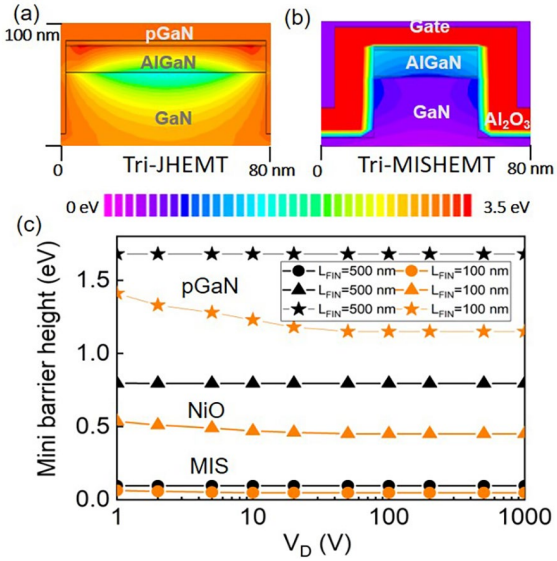

Fig. 9. Simulated Ψ_{FIN} contours in a tri-gate fin of (a) Tri-JHEMT with W_{FIN} = 75 nm and (b) Tri-MISHEMT with W_{FIN} = 40 nm, both at zero V_G and V_D = 1000 V. (c) Extracted minimum Ψ_{FIN} *v.s.* V_D for L_{FIN} of 500 nm and 100 nm in three E-mode devices, i.e., p-GaN-based Tri-JHEMT (W_{FIN} = 75 nm), NiO-based Tri-JHEMT (W_{FIN} = 40 nm), and Tri-MISHEMT (W_{FIN} = 40 nm).

at the center of 2DEG channel, which is over 1.5 eV in the Tri-JHEMT and 0.1 eV in the Tri-MISHEMT. The higher Ψ_{Fin} shows the stronger gate control in Tri-JHEMTs. This 1.5 eV barrier is much higher than the critical barrier (~0.6 eV [37]), below which the punch-through may occur.

To explore the gate scaling capabilities, Fig. 9(c) shows the simulated Ψ_{Fin} versus V_D for different gate technologies and fin length L_{Fin}. Both p-GaN- and NiO-based Tri-JHEMTs show higher Ψ_{Fin} than that of Tri-MISHEMTs. The p-GaN Tri-JHEMT shows the highest Ψ_{Fin}, allowing for further L_{Fin} scaling. For L_{Fin} = 100 nm, the Tri-JHEMT maintains a Ψ_{Fin} > 1 eV and V_{TH} > 1.1 V, while the simulated Ψ_{Fin} and V_{TH} of planar p-gate HEMTs drop to nearing zero. Such a short L_{Fin} can significantly reduce R_{CH_G} and gate charges, which is particularly beneficial for low voltage devices as R_{CH_G} dominates the device R_{ON}.

VII. Performance Space and Benchmark

To understand the performance space of Tri-JHEMTs as compared to Tri-MISHEMTs and planar p-gate HEMTs, we simulate these three types of devices with different L_{GD} for four voltage ratings, i.e., 15-V, 200-V, 600-V and 1200-V. As GaN HEMTs have no avalanche capabilities, commercial devices usually have a 50%-200% over-design in BV [21], [38]. For example, commercial 600/650-V rated GaN HEMTs have a BV of 1150~2200 V and an L_{GD} range of ~11.5 µm to ~21 µm [21], [38], [39]. In our simulations, we design a L_{GD} of 0.2-, 5-, 15- and 21-µm for the ratings of 15-, 200-, 600- and 1200-V, which provide a >50% BV margin. In addition, the Tri-JHEMT has 75-nm W_{FIN} and 1.3×10^{13}-cm^{-3} n_{2DEG}, the Tri-MISHEMT has 40-nm W_{FIN} and 8.5×10^{12}-cm^{-3} n_{2DEG}, and planar p-gate HEMTs has 3×10^{12}-cm^{-3} n_{2DEG}. All devices are E-mode, and the V_{TH} of all Tri-JHEMTs and planar p-gate HEMTs are 1.3 V. A 0.5-µm gate (fin) length is used for three types of devices; in addition, Tri-JHEMTs with 0.1-µm L_{FIN} are also simulated (only Tri-JHEMT can maintain stable V_{TH} and high BV at this L_{FIN}).

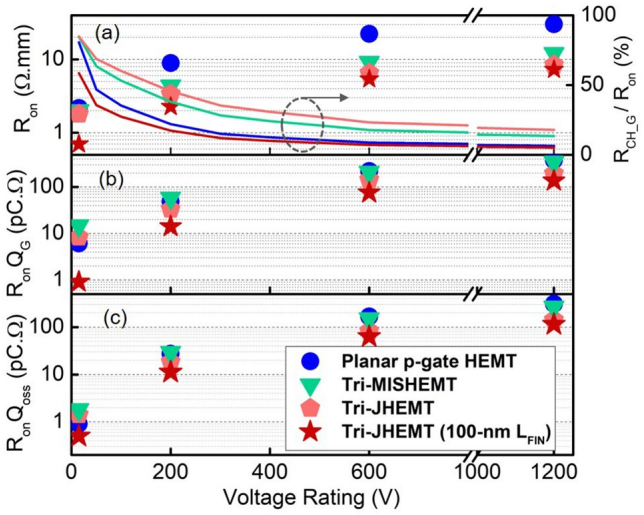

Fig. 10. Simulated (a) R_{ON} (markers) and R_{CH_G}/R_{ON} ratio (lines), (b) $R_{ON}{\cdot}Q_G$ and (c) $R_{ON}{\cdot}Q_{OSS}$ of four types of GaN devices, i.e., planar p-gate HEMT, Tri-MISHEMT, Tri-JHEMT, and the Tri-JHEMT with scaled L_{FIN} (100 nm), each type designed for four voltage ratings (15-, 200-, 600-, and 1200-V).

Fig. 10(a) shows the simulated R_{ON} (at V_G = 3 V) of four types of devices at various voltage ratings. The R_{ON} of tri-gate devices is generally smaller than that of similarly-rated p-gate HEMTs, but the underlying mechanisms vary with voltages. To illustrate them, the R_{CH_G}/R_{ON} ratio is also plotted. In low-voltage devices, R_{ON} is dominated by R_{CH_G}. R_{ON} of Tri-JHEMTs and Tri-MISHEMTs is 10~15% smaller than p-gate HEMTs, due to the higher 2DEG concentration in the gated fins enabled by the tri-gate structure. Whereas this higher 2DEG density is offset by the fin filling ratio (set as 50% for all tri-gate devices). Tri-JHEMTs show smaller R_{ON} than Tri-MISHEMTs due to a higher effective mobility in the tri-gate fins. A greater R_{ON} decrease (>30%) is shown in 100-nm L_{Fin} Tri-JHEMTs benefitted from the gate scaling.

In high-voltage devices, R_{ON} is dominated by the gate-drain access region, and the smaller R_{ON} of tri-gate devices is mainly due to higher wafer n_{2DEG}. Tri-JHEMTs allow much higher n_{2DEG} and thereby up to ~75% reduction in R_{ON} as compared to planar p-gate HEMTs for 600~1200-V ratings.

Note that, despite the lowest R_{CH_G} in the Tri-JHEMT, its R_{CH_G}/R_{ON} ratio is higher than that of Tri-MISHEMTs and planar p-gate HEMTs with the same L_{FIN}, suggesting that Tri-JHEMTs allow an even more significant reduction in access region resistance benefited from the higher wafer n_{2DEG}. When L_{FIN} scales down, the R_{CH_G}/R_{ON} ratio of Tri-JHEMTs is significantly reduced.

For power devices, R_{ON} controls the conduction loss and charges the switching loss. Current industry trend is using GaN HEMTs in high-frequency soft-switching applications, where the switching losses include the device output capacitance loss and gate driver loss. The former loss is controlled by the device output charge (Q_{OSS}) and the latter by the gate charge (Q_G). Considering the conduction loss, two figure of merits (FOMs) are often used for device comparison: $R_{ON}{\cdot}Q_G$ and $R_{ON}{\cdot}Q_{OSS}$ [5]. Q_{OSS} and Q_G of each device can be calculated by

$$Q_{OSS} = Q_{GD} + Q_{DS} = \int_0^{V_{DD}} [C_{GD}(V_D) + C_{DS}(V_D)] \cdot dV_D \quad (8)$$

$$Q_G = Q_{GD} + Q_{GS} = Q_{GD} + \int_0^{3\,V} C_G(V_G) \cdot dV_G \quad (9)$$

where V_{DD} is the converter bus voltage (usually 60% the device rated voltage). In (8), C_{GD} and C_{DS} are simulated at V_G = 0 V for V_{DS} up to V_{DD}. In (9), $C_G \sim V_G$ are simulated at V_{DS} = 1 V.

Fig. 10(b) and (c) show the $R_{ON}{\cdot}Q_G$ and $R_{ON}{\cdot}Q_{OSS}$ FOMs of four types of devices at various voltage ratings. For low rated voltages, Tri-JHEMTs and Tri-MISHEMTs cannot provide a superior $R_{ON}{\cdot}Q_G$ as compared to the planar p-gate HEMTs with a similar gate length. This is because the higher $\overline{n_{on,FIN}}$ in the tri-gate decreases R_{CH_G} but increases Q_G. In particular, Tri-MISHEMTs show higher $R_{ON}{\cdot}Q_G$ due to the low effective mobility in the MIS tri-gate. Nevertheless, the gate scaling in Tri-JHEMTs makes a great difference. As compared to planar p-gate HEMTs, the Tri-JHEMTs with 100-nm L_{FIN} show 10-fold lower $R_{ON}{\cdot}Q_G$ at 15-V class and 3-fold lower at 1200 V.

Similar to $R_{ON}{\cdot}Q_G$, at low voltage classes, Tri-JHEMTs and Tri-MISHEMTs show higher $R_{ON}{\cdot}Q_{OSS}$ as compared to the planar p-gate HEMTs with the same gate length, but the Tri-JHEMTs with 100-nm L_{FIN} allows 45% reduction in $R_{ON}{\cdot}Q_{OSS}$. At higher voltage classes, as the R_{ON} benefit prevails, the Tri-JHEMTs with 500-nm and 100-nm L_{FIN} shows 55 % and 63% reduction in $R_{ON}{\cdot}Q_{OSS}$, respectively, as compared to planar p-gate HEMTs. In comparison, despite 40% decrease in R_{ON}, Tri-MISHEMTs only show 10% decrease in $R_{ON}{\cdot}Q_{OSS}$ due to the large junction capacitance.

Finally, these comparisons reflect the performance spaces in the context of idealized device designs. For example, $R_{ON}{\cdot}Q_G$ and $R_{ON}{\cdot}Q_{OSS}$ of our simulated planar p-gate HEMTs were found to be at least 2-fold smaller than the similarly-rated commercial devices, because complicated field plates, metal interconnects and multi-layer dielectrics are used in commercial devices. This implies an underestimation of the advantages of the proposed Tri-JHEMTs over the commercial counterparts.

VIII. Summary and Discussion

This work reveals the device physics and performance space of Tri-JHEMTs in comparison with the planar p-gate HEMTs and Tri-MISHEMTs via 3-D TCAD simulations and analytical models. 3-D simulations are calibrated with the experimental NiO-based Tri-JHEMTs, which demonstrate the first kilovolt blocking capability at 150 °C in all GaN tri-gate HEMTs.

Benefitted from superior gate controllability, Tri-JHEMTs show a lower R_{CH_G}, a superior n_{2DEG}~V_{TH} trade-off, and better gate scaling capability as compared to planar p-gate HEMTs. The unique physics of the sidewall p-GaN/2DEG junctions make the 2DEG distribution in junction tri-gates quite different from that in MIS tri-gates, enabling a higher effective mobility and smaller C_G. E-mode Tri-JHEMTs with 75-nm fins are predicted to enable 15~75% lower R_{ON}, 3~10-fold smaller $R_{ON}{\cdot}Q_G$ and 45~63% smaller $R_{ON}{\cdot}Q_{OSS}$ as compared to the similarly-rated planar p-gate HEMTs across a wide range of voltage classes from 15 V to 1200 V.

Finally, we discuss the technological challenges for device fabrication. Building upon the experimental demonstration of NiO-based Tri-JHEMTs, the challenges of fabricating p-GaN-based Tri-JHEMTs may be associated with the p-GaN regrowth in the nonplanar gate region. While industry has demonstrated this process in vertical GaN FinFETs [7], [8] and lateral GITs [40], many academic groups have reported a high Si impurity and the resulted high leakage current at the regrown interface [41], [42]. In addition to scrutinizing the regrowth interface, more efforts are needed to study the properties of p-GaN/2DEG junctions. The first demonstration of this junction has shown a considerable sensitivity of its characteristics to fabrication process [18]. Despite these possible challenges, we believe that there are no fundamental barriers to manufacture p-GaN-based Tri-JHEMTs using the existing p-gate GaN foundry process. Hence, Tri-JHEMTs show great potentials as the next-generation GaN lateral power switches that are manufacturable and can deliver breakthrough performance.

ACKNOWLEDGEMENT

This work is in part supported by the National Science Foundation under Grants ECCS-2036740 and ECCS-2036915. The Virginia Tech work is also in part supported by the Office of Naval Research (No. N00014-21-S-B001) monitored by Lynn Petersen and the CPES Power Management Consortium. The authors acknowledge the collaborations with Silvaco for device simulations.

REFERENCES

[1] H. Amano *et al.*, "The 2018 GaN power electronics roadmap," *J. Phys. Appl. Phys.*, vol. 51, no. 16, p. 163001, 2018, doi: 10.1088/1361-6463/aaaf9d.

[2] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016, doi: 10.1109/JESTPE.2016.2582685.

[3] Y. Zhang, A. Zubair, Z. Liu, M. Xiao, J. A. Perozek, Y. Ma, and T. Palacios, "GaN FinFETs and trigate devices for power and RF applications: review and perspective," *Semicond. Sci. Technol.*, vol. 36, no. 5, p. 054001, Mar. 2021, doi: 10.1088/1361-6641/abde17.

[4] Y. Zhang and T. Palacios, "(Ultra)Wide-Bandgap Vertical Power FinFETs," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 3960–3971, Oct. 2020, doi: 10.1109/TED.2020.3002880.

[5] Y. Zhang, M. Sun, J. Perozek, Z. Liu, A. Zubair, D. Piedra, N. Chowdhury, X. Gao, K. Shepard, and T. Palacios, "Large-Area 1.2-kV GaN Vertical Power FinFETs With a Record Switching Figure of Merit," *IEEE Electron Device Lett.*, vol. 40, no. 1, pp. 75–78, Jan. 2019, doi: 10.1109/LED.2018.2880306.

[6] Y. Zhang, M. Sun, D. Piedra, J. Hu, Z. Liu, Y. Lin, X. Gao, K. Shepard, and T. Palacios, "1200 V GaN vertical fin power field-effect transistors," in *2017 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2017, p. 9.2.1-9.2.4, doi: 10.1109/IEDM.2017.8268357.

[7] J. Liu, M. Xiao, Y. Zhang, S. Pidaparthi, H. Cui, A. Edwards, L. Baubutr, W. Meier, C. Coles, and C. Drowley, "1.2 kV Vertical GaN Fin JFETs with Robust Avalanche and Fast Switching Capabilities," in *2020 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2020, p. 23.2.1-23.2.4, doi: 10.1109/IEDM13553.2020.9372048.

[8] J. Liu, M. Xiao, R. Zhang, S. Pidaparthi, H. Cui, A. Edwards, M. Craven, L. Baubutr, C. Drowley, and Y. Zhang, "1.2-kV Vertical GaN Fin-JFETs: High-Temperature Characteristics and Avalanche Capability," *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 2025–2032, Apr. 2021, doi: 10.1109/TED.2021.3059192.

[9] L. Nela, J. Ma, C. Erine, P. Xiang, T.-H. Shen, V. Tileli, T. Wang, K. Cheng, and E. Matioli, "Multi-channel nanowire devices for efficient power conversion," *Nat. Electron.*, vol. 4, no. 4, pp. 284–290, Apr. 2021, doi: 10.1038/s41928-021-00550-8.

[10] T. Tamura, J. Kotani, S. Kasai, and T. Hashizume, "Nearly Temperature-Independent Saturation Drain Current in a Multi-Mesa-Channel AlGaN/GaN High Electron Mobility Transistor," *Appl. Phys. Express*, vol. 1, no. 2, p. 023001, Feb. 2008, doi: 10.1143/APEX.1.023001.

[11] K. Ohi and T. Hashizume, "Drain Current Stability and Controllability of Threshold Voltage and Subthreshold Current in a Multi-Mesa-Channel AlGaN/GaN High Electron Mobility Transistor," *Jpn. J. Appl. Phys.*, vol. 48, no. 8R, p. 081002, Aug. 2009, doi: 10.1143/JJAP.48.081002.

[12] B. Lu, E. Matioli, and T. Palacios, "Tri-Gate Normally-Off GaN Power MISFET," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 360–362, Mar. 2012, doi: 10.1109/LED.2011.2179971.

[13] J. Ma and E. Matioli, "High Performance Tri-Gate GaN Power MOSHEMTs on Silicon Substrate," *IEEE Electron Device Lett.*, vol. 38, no. 3, pp. 367–370, Mar. 2017, doi: 10.1109/LED.2017.2661755.

[14] M. Zhu, J. Ma, L. Nela, C. Erine, and E. Matioli, "High-Voltage Normally-off Recessed Tri-Gate GaN Power MOSFETs With Low on-Resistance," *IEEE Electron Device Lett.*, vol. 40, no. 8, pp. 1289–1292, Aug. 2019, doi: 10.1109/LED.2019.2922204.

[15] C.-H. Wu, J.-Y. Chen, P.-C. Han, M.-W. Lee, K.-S. Yang, H.-C. Wang, P.-C. Chang, Q. H. Luc, Y.-C. Lin, C.-F. Dee, A. A. Hamzah, and E. Y. Chang, "Normally-Off Tri-Gate GaN MIS-HEMTs with 0.76 $m\Omega \cdot cm^2$ Specific On-Resistance for Power Device Applications," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3441–3446, Aug. 2019, doi: 10.1109/TED.2019.2922301.

[16] D.-H. Son, Y.-W. Jo, V. Sindhuri, K.-S. Im, J. H. Seo, Y. T. Kim, I. M. Kang, S. Cristoloveanu, M. Bawedin, and J.-H. Lee, "Effects of sidewall MOS channel on performance of AlGaN/GaN FinFET," *Microelectron. Eng.*, vol. 147, pp. 155–158, Nov. 2015, doi: 10.1016/j.mee.2015.04.101.

[17] Y. Ma, M. Xiao, Z. Du, X. Yan, K. Cheng, M. Clavel, M. K. Hudait, I. Kravchenko, H. Wang, and Y. Zhang, "Tri-gate GaN junction HEMT," *Appl. Phys. Lett.*, vol. 117, no. 14, p. 143506, Oct. 2020, doi: 10.1063/5.0025351.

[18] M. Xiao, Z. Du, J. Xie, E. Beam, X. Yan, K. Cheng, H. Wang, Y. Cao, and Y. Zhang, "Lateral p-GaN/2DEG junction diodes by selective-area p-GaN trench-filling-regrowth in AlGaN/GaN," *Appl. Phys. Lett.*, vol. 116, no. 5, p. 053503, Feb. 2020, doi: 10.1063/1.5139906.

[19] E. Persson, "CoolGaN^{TM} application note."

[20] Y. Ma, M. Xiao, Y. Zhang, Z. Du, X. Yan, H. Wang, K. Cheng, M. Clavel, M. K. Hudait, L. Tao, F. Lin, and I. Kravchenko, "Kilovolt Tri-Gate GaN Junction HEMTs with High Thermal Stability," in *2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2021, pp. 139–142, doi: 10.23919/ISPSD50666.2021.9452203.

[21] R. Zhang, J. P. Kozak, M. Xiao, J. Liu, and Y. Zhang, "Surge-Energy and Overvoltage Ruggedness of P-Gate GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13409–13419, Dec. 2020, doi: 10.1109/TPEL.2020.2993982.

[22] J. Ma, G. Santoruvo, L. Nela, T. Wang, and E. Matioli, "Impact of Fin Width on Tri-Gate GaN MOSHEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 9, pp. 4068–4074, Sep. 2019, doi: 10.1109/TED.2019.2925859.

[23] M. A. Alsharef, R. Granzner, and F. Schwierz, "Theoretical Investigation of Trigate AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3335–3341, Oct. 2013, doi: 10.1109/TED.2013.2279264.

[24] A. Chakrabarty and R. Swain, "Modelling of fin width dependent threshold voltage in fin shaped nano channel AlGaN/GaN HEMT," *Superlattices Microstruct.*, vol. 141, p. 106497, May 2020, doi: 10.1016/j.spmi.2020.106497.

[25] Y. Zhang, M. Sun, Z. Liu, D. Piedra, H. S. Lee, F. Gao, T. Fujishima, and T. Palacios, "Electrothermal Simulation and Thermal Performance Study of GaN Vertical and Lateral Power Transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2224–2230, Jul. 2013, doi: 10.1109/TED.2013.2261072.

[26] M. Xiao, R. Zhang, D. Dong, H. Wang, and Y. Zhang, "Design and Simulation of GaN Superjunction Transistors With 2-DEG Channels and Fin Channels," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 3, pp. 1475–1484, Sep. 2019, doi: 10.1109/JESTPE.2019.2912978.

[27] H. Wang, M. Xiao, K. Sheng, T. Palacios, and Y. Zhang, "Switching Performance Analysis of Vertical GaN FinFETs: Impact of Interfin Designs," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 2, pp. 2235–2246, Apr. 2021, doi: 10.1109/JESTPE.2020.2980445.

[28] M. Xiao, T. Palacios, and Y. Zhang, "ON-Resistance in Vertical Power FinFETs," *IEEE Trans. Electron Devices*, vol. 66, no. 9, pp. 3903–3909, Sep. 2019, doi: 10.1109/TED.2019.2928825.

[29] M. Xiao, Y. Ma, K. Liu, K. Cheng, and Y. Zhang, "10 kV, 39 mΩ·cm2 Multi-Channel AlGaN/GaN Schottky Barrier Diodes," *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 808–811, Jun. 2021, doi: 10.1109/LED.2021.3076802.

[30] M. Xiao, Y. Ma, Z. Du, X. Yan, R. Zhang, K. Cheng, K. Liu, A. Xie, E. Beam, Y. Cao, H. Wang, and Y. Zhang, "5 kV Multi-Channel AlGaN/GaN Power Schottky Barrier Diodes with Junction-Fin-Anode," in *2020 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2020, p. 5.4.1-5.4.4, doi: 10.1109/IEDM13553.2020.9372025.

[31] M. Xiao, Y. Ma, K. Cheng, K. Liu, A. Xie, E. Beam, Y. Cao, and Y. Zhang, "3.3 kV Multi-Channel AlGaN/GaN Schottky Barrier Diodes With P-GaN Termination," *IEEE Electron Device Lett.*, vol. 41, no. 8, pp. 1177–1180, Aug. 2020, doi: 10.1109/LED.2020.3005934.

[32] T. Palacios, A. Zubair, J. Niroula, J. Perozek, N. Chowdhury, D. Pei, M. Dipsey, H. Emmer, and B. Lu, "GaN 2.0: Power FinFETs, Complementary Gate Drivers and Low-Cost Vertical Devices," in *2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2021, pp. 6–10, doi: 10.23919/ISPSD50666.2021.9452205.

[33] T.-L. Wu, B. Bakeroot, H. Liang, N. Posthuma, S. You, N. Ronchi, S. Stoffels, D. Marcon, and S. Decoutere, "Analysis of the Gate Capacitance–Voltage Characteristics in p-GaN/AlGaN/GaN Heterostructures," *IEEE Electron Device Lett.*, vol. 38, no. 12, pp. 1696–1699, Dec. 2017, doi: 10.1109/LED.2017.2768099.

[34] A. Nipane, S. Jayanti, A. Borah, and J. T. Teherani, "Electrostatics of lateral p-n junctions in atomically thin materials," *J. Appl. Phys.*, vol. 122, no. 19, p. 194501, Nov. 2017, doi: 10.1063/1.4994047.

[35] V. K. Gurugubelli and S. Karmalkar, "Analytical theory of the space-charge region of lateral *p-n* junctions in nanofilms," *J. Appl. Phys.*, vol. 118, no. 3, p. 034503, Jul. 2015, doi: 10.1063/1.4926478.

[36] H. Yu, A. Kutana, and B. I. Yakobson, "Carrier Delocalization in Two-Dimensional Coplanar p–n Junctions of Graphene and Metal Dichalcogenides," *Nano Lett.*, vol. 16, no. 8, pp. 5032–5036, Aug. 2016, doi: 10.1021/acs.nanolett.6b01822.

[37] M. Xiao, X. Gao, T. Palacios, and Y. Zhang, "Leakage and breakdown mechanisms of GaN vertical power FinFETs," *Appl. Phys. Lett.*, vol. 114, no. 16, p. 163503, Apr. 2019, doi: 10.1063/1.5092433.

[38] R. Zhang, J. P. Kozak, Q. Song, M. Xiao, J. Liu, and Y. Zhang, "Dynamic Breakdown Voltage of GaN Power HEMTs," in *2020 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2020, p. 23.3.1-23.3.4, doi: 10.1109/IEDM13553.2020.9371904.

[39] Q. Song, R. Zhang, J. P. Kozak, J. Liu, Q. Li, and Y. Zhang, "Failure Mechanisms of Cascode GaN HEMTs Under Overvoltage and Surge Energy Events," in *2021 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2021, pp. 1–7, doi: 10.1109/IRPS46558.2021.9405208.

[40] H. Okita, M. Hikita, A. Nishio, T. Sato, K. Matsunaga, H. Matsuo, M. Tsuda, M. Mannoh, S. Kaneko, M. Kuroda, M. Yanagihara, A. Ikoshi, T. Morita, K. Tanaka, and Y. Uemoto "Through Recess and Regrowth Gate Technology for Realizing Process Stability of GaN-Based Gate Injection Transistors," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1026–1031, Mar. 2017, doi: 10.1109/TED.2017.2653847.

[41] M. Xiao, X. Yan, J. Xie, E. Beam, Y. Cao, H. Wang, and Y. Zhang, "Origin of leakage current in vertical GaN devices with nonplanar regrown p-GaN," *Appl. Phys. Lett.*, vol. 117, no. 18, p. 183502, Oct. 2020, doi: 10.1063/5.0021374.

[42] A. Aragon, M. Monavarian, I. Stricklin, G. Pickrell, M. Crawford, A. Allerman, A. M. Armstrong, and D. Feezell, "Interfacial Impurities and Their Electronic Signatures in High-Voltage Regrown Nonpolar m-Plane GaN Vertical *p–n* Diodes," *Phys. Status Solidi A*, vol. 217, no. 7, Apr. 2020, Art. no. 1900757, doi: 10.1002/pssa.201900757.