Applied Physics Letters

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Cite as: Appl. Phys. Lett. **117**, 232105 (2020); https://doi.org/10.1063/5.0031462
Submitted: 30 September 2020 • Accepted: 27 November 2020 • Published Online: 08 December 2020

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Applied Physics Letters ARTICLE scitation.org/journal/apl

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Submitted: 30 September 2020 · Accepted: 27 November 2020 ·
Published Online: 8 December 2020

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Note: This paper is part of the Special Topic on Ultrawide Bandgap Semiconductors.
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ABSTRACT

We present the temperature-dependent electrical characteristics of high-current depletion (D-mode) and barrier-recessed enhancement-mode (E-mode) ultrawide bandgap (UWBG) $Al_xGa_{1-x}N$ channel insulated gate heterojunction field-effect transistors fabricated on the same wafer. The key motivation is the higher Baliga figure of merit for devices with the UWBG AlGaN channel and their strong potential for use in high-power, high-temperature harsh environmental applications. Over a temperature range of 125 °C, the V_{TH} shifted in the opposite direction for D- and E-mode devices with a rate of +13.5 mV/K and −23 mV/K, respectively, giving an overall shift of +1.7 V and −2.9 V. This was attributed to changes in the fixed and trapped charge densities in the dielectric and at the dielectric–AlGaN barrier interface. A single deep sub-bandgap trap level was sufficient to explain the threshold shifts in both devices. The effective channel mobility in the E-mode devices was argued to be limited by charge scattering, arising from the same charges introduced during barrier recessing that shifted V_{TH}.

Ultrawide bandgap (UWBG) $Al_xGa_{1-x}N$ ($x > 0.4$) channel heterostructure field effect transistors (HFETs) have drawn significant attention in recent years due to their very strong potential for use in high-temperature, high-voltage, and high-power applications. The higher breakdown field of AlGaN channel HFETs leads to a higher Baliga Figure of Merit (BFOM).[1,2] Devices with channel alloy compositions of 40% or higher have been reported by several groups including ours.[3–7] Until recently, most reported AlGaN channel devices had drain currents well below 1 A/mm, i.e., much lower than the typical values for GaN channel HFETs.[8–11] Recently, our group achieved high peak current depletion mode (D-mode) and enhancement mode (E-mode) UWBG AlGaN channel insulated gate HFETs (MOSHFETs). The D-mode MOSHFET peak current of 1.3 A/mm opens the possibility of several practical applications.[12] The superior device performance of the D-mode and E-mode devices was a result of incorporating several features: a thin channel epilayer structure with an $Al_xGa_{1-x}N$ back barrier, a perforated gate device design, and an Atomic Layer Deposited (ALD) Al_2O_3-ZrO_2 composite dielectric gate insulator. Despite their critical importance for power electronics applications, to date, there is very little work on UWBG AlGaN channel E-mode devices. This is very different from GaN channel HFET technology where E-mode devices are now commercially available. Recently, using fluorine treatment, Klein *et al.* reported the E-mode UWBG $Al_{0.7}Ga_{0.3}N$ channel HFET with $V_{TH} = +0.5$ V (at $I_{DS} = 0.1$ mA/mm) with a peak current of only 35 mA/mm (at $V_{GS} = +10$ V).[13]

Our group recently reported high-current E-mode UWBG AlGaN channel MOSHFETs[14] using the same epilayer structure that was the basis for the high current D-mode MOSHFETs of Ref. 12. Using a recessed-gate design, we demonstrated the E-mode Al_2O_3-ZrO_2/$Al_{0.6}Ga_{0.4}N$/$Al_{0.4}Ga_{0.6}N$ MOSHFET with drain current as high as 0.48 A/mm at a gate-source voltage of +12 V. Using the $I_{DS} = 10$ μA/mm criterion used by Asubar *et al.*,[15] our device has a threshold voltage $V_{TH} = +1.4$ V and a linearly extrapolated threshold voltage of +3.6 V. Both D- and E-mode MOSHFETs can be fabricated on the same wafer with the same major processing steps except masking D-mode devices during gate recess etching. More details can be found in Ref. 14. In this work, we present the studies of performance characteristics of these high current D-mode and E-mode devices at elevated temperatures up to 150 °C. Such studies are critically important for devices intended for high-power, high-temperature, and harsh environmental condition operation.

The D- and E-mode MOSHFET design is shown in Fig. 1. We have incorporated a graded composition ($Al_xGa_{1-x}N$, x from 1 to 0.4) back barrier, which is grown directly on the 3 μm thick AlN template on sapphire. The back-barrier design enables a reduction in leakage currents by screening the substrate-epilayer growth interface. It also leads to a tighter confinement of the 2-DEG, which improves the ON-OFF ratios, drain-currents, and the sub-threshold swing factor.[16–18] The second barrier on the gate side of the epilayer structure is itself a multilayer structure. It consisted of a 3 A thick AlN spacer layer, a 150 A thick Si-doped n-$Al_{0.6}Ga_{0.4}N$ barrier layer, followed by a 20 nm thick reverse composition graded Si-doped $Al_xGa_{1-x}N$ (x from 0.6 to 0.3) layer. The reverse composition graded layer assists with the formation of low resistivity Ohmic contacts. The n-doping of this layer compensates the positive charges resulting from the reverse composition grading.[19] The epilayer growth was carried out using low pressure metalorganic chemical vapor deposition (LP-MOCVD), and the details of the growth procedure were the same as described elsewhere.[20]

For this study, both D-mode and E-mode MOSHFET devices were fabricated as shown in Fig. 1. For either device type, first using Inductively Coupled Plasma Reactive Ion Etching (ICPRIE), isolated mesas were fabricated. The Ohmic metal stacks Zr/Al/Mo/Au (150/1000/400/300 Å) for the two were also identical and were deposited by E-beam evaporation and annealed for 30 s at 950 °C under N_2 ambient using rapid thermal annealing (RTA). The device design also incorporated a perforated channel (PC) layout to reduce access resistances (see the supplementary material for more details). This approach is like that reported by Simin *et al.* for GaN channel HFETs.[12,21] Because of the perforations, the device channel consists of relatively narrow ($W_S \approx 3.75\ \mu$m) 2-DEG conducting sections ("straits") separated by current blocking islands ($W_B \approx 8.25\ \mu$m), which were formed using a BCl_3 RIE process after the formation of the source-drain Ohmic contacts. The effective channel width of a perforated device is 15.6 μm for a regular (unperforated) 50 μm width device. This geometry corresponds to an optimal island/gap ratio of 2–2.5 as was determined following the procedure outlined in Ref. 21. Next, only for the E-mode devices, the gate recessing was carried out using a BCl_3 etching process. Then, a 25 nm-thick ZrO_2-Al_2O_3 insulator stack was deposited in the gate region of both device types before the formation of the Ni/Au gates. For either device type, the gate-length was kept fixed at $L_G \approx 2.0\ \mu$m, but the gate-source and gate-drain spacings (L_{SG}, L_{GD}) were varied. The transistor surfaces were protected with a PECVD deposited 400 nm thick SiO_2 film for high-voltage breakdown measurements. In addition to regular devices, we also fabricated unperforated TLM pads of 80 μm × 200 μm to extract the contact and sheet resistance values.

From TLM measurements, we found the sheet-resistance $R_{SH} \approx 1700\ \Omega/\square$ and the contact resistance $R_C \approx 1.7\ \Omega$-mm, which translates to a specific contact resistivity of $3.4 \times 10^{-5}\ \Omega\ cm^2$. The field-effect electron mobility estimated from C–V and gated TLM IV data is 200 $cm^2/V\ s$ at gate voltage $V_G = 12$ V, which increases up to 1050 $cm^2/V\ s$ at $V_G = 4$ V (depleted channel) for the E-mode devices, in line with estimates at low carrier concentrations $<10^{11}\ cm^{-2}$ taking alloy scattering as the limiting factor in this ternary.[22] For D-mode ZrO_2 MOSHFETs, the typical mobility values are 191 $cm^2/V\ s$ and 554 $cm^2/V\ s$ for gate voltage $V_G = 0$ V and −7 V, respectively.[23]

The source-drain and current–voltage (I–V) characteristics for the D-mode and the E-mode MOSHFETs are presented in Fig. 2(a). The maximum dc for the D- and E-mode devices is 1.2 A/mm and 0.48 A/mm, respectively. The currents were normalized to the effective channel width of 15.6 μm. We also present short pulse I–Vs measured using a DIVA D265 dynamic IV analyzer with a pulse duration of 500 ns and a low duty cycle of 0.1% to avoid device heating. As seen, in the pulsed mode, peak drain currents over 1.3 A/mm and 0.53 A/mm are achieved for the D- and E-mode devices, respectively, at a gate voltage of + 10V. The gate-current at this gate voltage (+10 V) was only 10^{-7} A, showing that our ALD gate oxides are of a high quality.

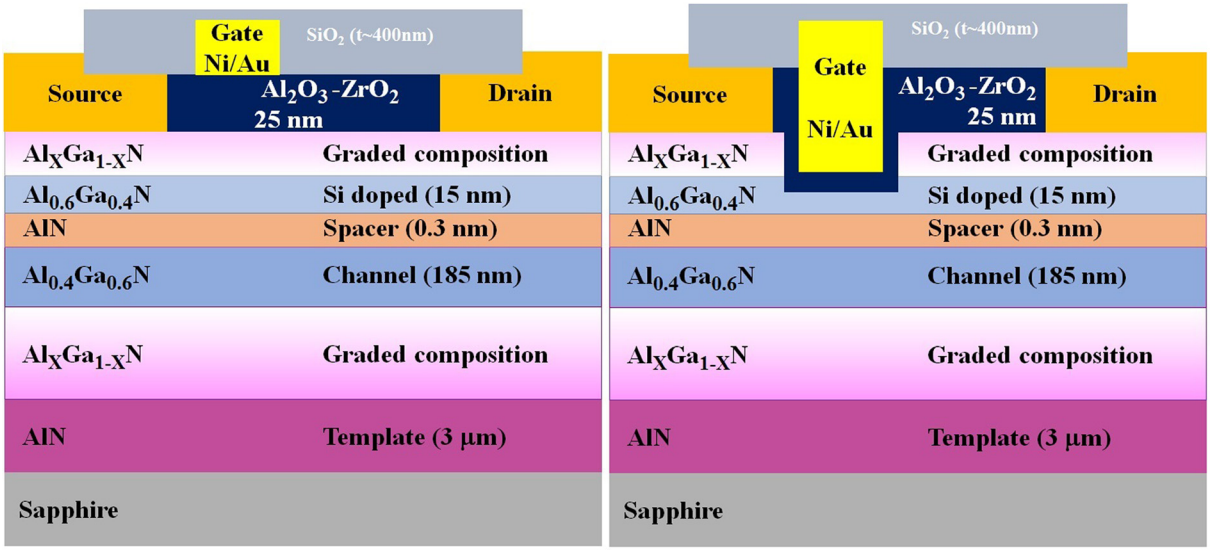

FIG. 1. Schematic of the D-mode (left) and E-mode (right) MOSHFETs.

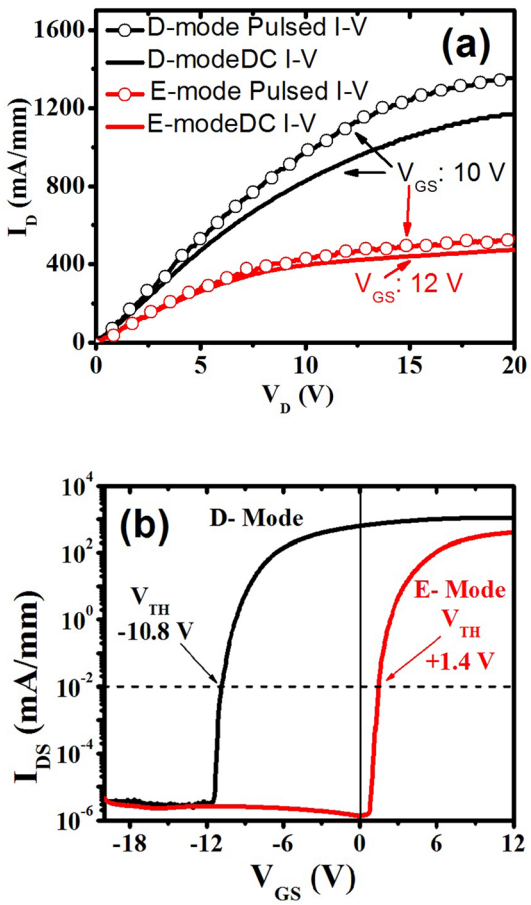

FIG. 2. (a) Maximum source-drain DC IV characteristics of D-mode and E-mode MOSHFETs at $V_G = +10$ V and +12 V, respectively. Also shows pulsed IV characteristics for D- and E-mode MOSHFETs at $V_G = 10$ V. (b) Semi-log transfer characteristics for the D-mode and the E-mode devices. The threshold shift in the E-mode device with respect to the D mode device is 12.2 V.

Figure 2(b) shows the transfer characteristics for D- and E-mode devices. From these data, the E-mode device has $V_{TH} = +1.4$ V using the criterion of Ref. 15 (voltage at $I_{DS} = 10$ μA/mm) and the linearly extrapolated threshold voltage is $V_{TH} = +3.6$ V. Thus, our recessed ALD oxide technique leads to the shift in the threshold voltage of the D-mode devices by approximately +12 V.

Next, we studied the temperature dependencies of the threshold voltages of D- and E-mode MOSHFETs [Fig. 3(a)]. These were measured using the heated probe station for the devices on the same wafer. The temperature-dependent V_{TH} are shown in Fig. 3(a). As seen, for the D-mode MOSHFET, the V_{TH} experiences a positive V_{TH} shift of + 1.7 V from RT to 150 °C; for the E-mode MOSHFET, the shift is negative: −2.9 V. Figure 3(b) shows the mobility variation with temperature, μ(T), for a sheet carrier density $N_S = 1 \times 10^{13}$ cm^{-2}. μ(T) in D-mode devices decreases with temperature, while it increases for E-mode devices. By power law fitting of μ(T), indices (α) in the equation $\mu = AT^{\alpha}$ were obtained as −0.4 and +0.5 for D- and E-mode devices, respectively. This means that in D-mode devices, the mobility

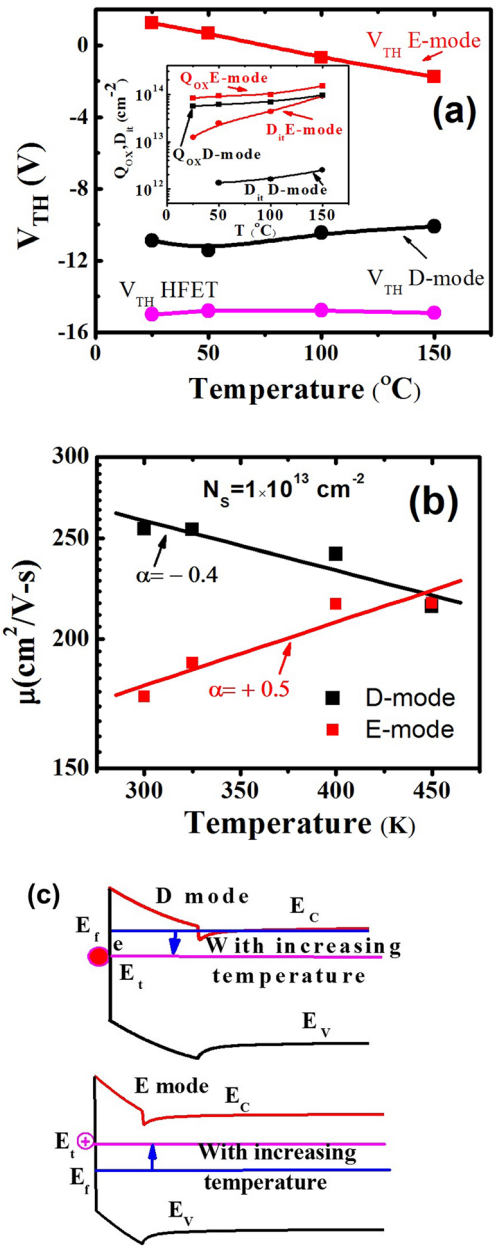

FIG. 3. (a) Temperature-dependent threshold voltages for D- and E-mode devices. The V_{TH} shifts from RT to 150 °C are −2.9 V for E-mode and + 1.7 V for D-mode MOSHFETs. For comparison, the V_{TH} shift of +0.2 V for the Schottky-gate D-mode HFET is also shown. The inset graph shows the temperature dependence of interface state density (D_{it}) and oxide charge(Q_{ox}) (b) power law fitting of mobility vs temperature to extract power law indices (α). (c) Schematic energy band diagram showing the trap energy level (E_t) and position of the Fermi level relative to E_t.

is dominated by phonon scattering (typically in GaN $-2 < \alpha < -1$) mixed with alloy scattering ($\alpha \approx 0$) while in E-mode it is dominated by ionized impurity or charge scattering (typically in GaN $+1 < \alpha < 2$) and alloy scattering ($\alpha \approx 0$).[24,25] We attribute the increased charge scattering in E-mode devices to the additional fixed charges and interface

traps introduced by barrier recess, as will be discussed separately below. For the D-mode device, the V_{TH} gets more positive with the temperature increase. This means that the total channel charge decreases, along with μ(T). We, therefore, expect the drain current to decrease with temperature. For the E-mode device, the V_{TH} gets more negative reflective of an increased channel charge, as μ(T) also increases. Therefore, the overall drain current is expected to increase with the temperature, as was observed (supplementary material).

To further analyze the mechanisms leading to significant V_{TH} shifts with temperature in MOSHFETs, we compared them with those of a similar device having Schottky gate (no dielectric). As seen from Fig. 3(a), the V_{TH} shift for HFET is significantly smaller, +0.2 V. This shows that the V_{TH} shift is mainly due to the charges in the dielectric or at the dielectric-barrier interface. The extracted subthreshold swing (SS) values for D- and E-mode devices were 99 mV/decade and 134 mV/decade, giving an ideality factor (n) of 1.7 and 2.3, respectively (supplementary material), indicating an increased density of interface traps at the recessed interface in the E-mode device.[26] We estimated the total interface density of states, D_{IT} vs T, using the difference between the area of frequency-dependent C–V measurements (supplementary material).[23] The extracted dependencies are shown in the inset of Fig. 3(a). Like the observed V_{TH} shifts, the D_{IT} for the E-mode MOSHFET is higher than that for the D-mode device. We attribute this larger D_{IT} value in E-mode devices to the barrier recessing process, which introduces traps at the oxide/semiconductor interface, consistent with the increased SS. Similar trends have been observed in a study from Yang *et al.*[27]

In addition to D_{IT} causing the V_{TH} shift, we will argue that fixed oxide charges (Q_{ox}), as measured by C–V, are also responsible. For these C–V measurements, we used devices with gate-length $L_G = 80\ \mu$m and gate-width $W = 200\ \mu$m. With the measured C–V data, we conducted electrostatic analysis as follows to determine the fixed oxide charges.[28] The built-in voltage V_{bi}, measured from the $1/C^2$ x-intercept, can be expressed in terms of the depletion region width in the barrier layer, x_d, as follows:[28]

$$V_{bi} = \frac{qN_d x_d^2}{2\epsilon_s} + E_{ox} t_{ox}. \tag{1}$$

We determine the E_{ox} from Gauss's law at the oxide/barrier interface, where Q_{ox} is the fixed sheet charge density at this interface,

$$\epsilon_{ox} E_{ox} - \epsilon_s E_s = Q_{ox} = \epsilon_{ox} E_{ox} - \epsilon_s \left(\frac{qN_d x_d}{\epsilon_s} \right). \tag{2}$$

If we solve for E_{ox} in terms of Q_{ox}, We can rewrite Eq. (1) as

$$V_{bi} = \frac{qN_d x_d^2}{2\epsilon_s} + \frac{qN_d x_d}{\epsilon_{ox}} t_{ox} + \frac{Q_{ox}}{\epsilon_{ox}} t_{ox}. \tag{3}$$

x_d is calculated from the fact that the oxide capacitance, $C_{ox}=\epsilon_{ox}/t_{ox}$, and the depletion capacitance in the barrier, ϵ_s/x_d, are in series. From the measured 0 bias capacitance C (0), $x_d = (C_{ox}\epsilon_s - C(0)\epsilon_s)/C(0)C_{ox}$. Inserting this x_d into Eq. (3), we have an equation with only unknown parameter Q_{ox}, in terms of the measured V_{bi}, N_d, and the known oxide parameters. The extracted Q_{ox} (T) is plotted in the inset of Fig. 3(a). It shows that in the D-mode device, Q_{ox}(T) is much higher than D_{IT}(T). These are fixed negative charges, which deplete the channel, and shift V_{TH} more positively, giving a total shift of +1.7 V from RT to 150 °C. In the E-mode device, the Q_{ox} and D_{IT} values are comparable [see Fig. 3(a) inset] and, thus, the effect of Q_{ox} is compromised by D_{IT}, thus shifting the V_{TH} in the opposite direction. We use these values of fixed charges in a 1D Poisson Solver simulation[29] and observe a similar V_{TH} shift from RT to 150 °C (supplementary material).

Our results suggest that a deep sub-bandgap trap level (E_t) located near the mid-bandgap plays the role for positive and negative V_{TH} shifts in D- and E-mode devices, respectively, as has been done with AlGaN/GaN HEMTs.[30] We assume this state is donor-like, neutral when occupied, and positive when empty. In the D-mode device, at RT, the majority of the trap states contribute electrons (positively charged) to form N_S and the Fermi level (E_f) is well above the bottom of the conduction band [Fig. 3(c)].[30,31] As the temperature increases, trap states start occupying electrons from 2DEG, moving E_f down toward the intrinsic midgap position. At elevated temperature, the 2DEG density is less than that of room temperature. As a result, less negative voltage is required to deplete the channel compared to room temperature, causing a positive threshold shift.

In the E-mode devices, at RT, the E_f is between E_t and E_v. With a temperature rise, the E_f moves up, filling more trap states. Electron transfer then occurs to the conduction band of $Al_{0.4}Ga_{0.6}N$, which is close to E_t. As the temperature keeps increasing, more and more electrons transfer from the trap states to 2DEG. Additional negative voltage is required to deplete the excess electrons, causing a more negative threshold shift.

The three terminal breakdown voltages for the D-mode devices were found to be over 1000 V for a gate-drain spacing of 8 μm. For an E-mode device with a gate-drain spacing $L_{GD} = 4.1\ \mu$m, the breakdown voltage was measured to be over +700 V (supplementary material). The breakdown field is still far from the theoretical limit, and we believe that the surface flashover is the dominating factor here. These values are expected to improve with field-plating and better control of surfaces. Nevertheless, these devices exceed the 600 V standard for power electronics.

In summary, we presented Al_2O_3-ZrO_2/$Al_{0.6}Ga_{0.4}N$/$Al_{0.4}Ga_{0.6}N$ D-mode and E-mode MOSHFET devices with drain currents as high as 1.3 A/mm and 0.48 A/mm and studied their temperature dependencies. For D- and E-mode devices, the threshold voltage shift from RT to 150 °C is +1.7 V and −2.9 V, respectively. The temperature shift of V_{TH} for the MOSHFET is attributed to the activation of fixed and trapped charges in the dielectric and/or the dielectric/AlGaN interface. Scattering from these increased charges dominates the channel mobility in E-mode devices.

See the supplementary material for the optical and SEM image of the perforated channel (PC) MOSHFETs; cross-sectional view of unperforated and perforated portions of the channel; temperature-dependent subthreshold swing (SS); temperature-dependent peak current for D- and E-mode devices; high-low C–V for D_{it} extraction and breakdown characteristics.

This work was supported by the DARPA DREAM program (ONR No. N00014-18-1-2033, Program Manager Dr. Young-kai Chen, monitored by ONR, Program Manager Dr. Paul Maki), ARO Contract No. W911NF-18-1-0029 monitored by Dr. M. Gerhold, ONR MURI program (Contract No. N00014-18-1-2429) monitored by Mr. Lynn Petersen, AFOSR through Dr. K. Goretta NSF, and

ECCS Award Nos. 1711322, 1810116, and 1831954 under supervision of Dr. Dimitris Pavlidis.

DATA AVAILABILITY

The data that support the findings of this study are available within the paper and its supplementary material.

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