Jitter-Aware Economic PDN Optimization With a Genetic Algorithm

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***Abstract*— This article proposes a jitter-aware decoupling capacitors placement optimization method that uses the genetic algorithm (GA). A novel method for defining the optimization target function in regard to power delivery network (PDN) and power source-induced jitter (PSIJ) optimization based on the GA-based tool is proposed. The proposed method can provide an optimum and economic solution for the number of decoupling capacitors to use in a PDN to reach the target impedance. Then, by modifying the optimization target function with our proposed method, an optimum solution of the number of decoupling capacitors regarding the PSIJ can be obtained. The PSIJ analytical expressions are derived in conjunction with a resonant cavity model that includes the coordinates of the decoupling capacitors and the PSIJ transfer function. The GA-based optimization algorithm with the proposed target function is first applied to optimize the number of decoupling capacitors regarding the PSIJ. Finally, the measured jitters from HSPICE simulation results are used to verify our optimization method such that both the simulated results and analytically calculated results support the efficiency of our proposed optimization method.**

***Index Terms*— Decoupling capacitor, genetic algorithm (GA), jitter, power delivery network (PDN), power integrity, power source-induced jitter (PSIJ).**

I. Introduction

BECAUSE high-speed applications have spread to all types of electronics, the operating data rate of a typical device can now reach hundreds of Gb/s. Meanwhile, the size of modern electronics has decreased significantly, either consistent with Moore's law or, in some cases, even surpassing it [1]. Some of the challenges that have previously been ignored now must be considered. One of the most challenging tasks for electronic designers is maintaining the power and signal integrity in a high-speed system while reducing cost [2], [3]. In addition, due to the incorporation of a large number of transistors inside the typical integrated circuit (IC), the current level of the power traces can reach values as great as 100 A [4]. Such large currents generate significant supply voltage fluctuations if the power delivery network (PDN) is not well designed. The induced supply voltage fluctuations significantly affect both the signal and power integrity (SI and PI). Aside from the large current generated by the on-chip circuit, the subsystems of a typical high-speed system, such as its voltage regulator modules (VRMs), interconnects, and packages, also remain significant problems for the SI and PI.

The SI and PI normally interact in high-speed systems and correspond, respectively, to the signal quality and power delivery quality. The major SI and PI issues include reflection, insertion loss, crosstalk, ground bounce, simultaneous switching noise (SSN), and so on [5]. The first three issues are current questions for the SI, whereas the latter two items concern the PI. In high-speed applications, SSN is a significant problem for both SI and PI engineers because the SSN generates noise in the PDN network that also impacts the SI in terms of timing variations at the data/clock output [6]. In particular, a high SSN affects the supply noise by that can cause signal distortion, jitter, and bit error rate (BER) [7].

Time variation remains a challenging issue in high-speed designs and is also known as the jitter that occurs at the transition edges of the clock and data signals. Time variation can be defined as the timing difference at the transition edges from their ideal positions. The jitter in a high-speed system is categorized as either random jitter (RJ) or deterministic jitter (DJ) [8]. The deterministic jitter can be characterized by different methods. Many investigations have been carried out on power supply-induced jitter (PSIJ) [7], which is one type of DJ. The jitter budget can be achieved by minimizing the PSIJ for some high-speed applications, such as USB, DDR, and PCIe. For a post-product validation, the jitter can be measured by using a phase analyzer [2], [9], jitter analyzer, or oscilloscope, among others. However, for a prelayout design, only simulations are possible to evaluate the jitter performance. To study PSIJ, PDNs need to be included. Due to the distribution characteristics of PDNs at high frequency, the layout parasitic capacitance and inductance cannot be ignored in the PDN design for high-speed applications. As the behavior of the power/ground plane pair that supports the radial wave propagation grows increasingly complex, lumped models are no longer efficient for the characterization of PDN performance.

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The placement of the decoupling capacitors in a device significantly influences its performance [10]–[12]. In previous studies [13]–[15], different effective decoupling regions of decoupling capacitors were investigated, in which the influence of their placement was analyzed based on the resonant cavity model, which is known to support high-frequency PDN performance characterization. The resonant cavity model has been employed to efficiently compute the optimal locations of the decoupling capacitors based on the Newton iteration method [16], [17]. However, this kind of method is only applicable to a single capacitor at a single-frequency point. Recently, an investigation of the placement of multiple capacitors over a frequency band was proposed in [18]. However, the method that those authors applied was still fundamentally an iteration method used for frequencies, where the frequency points at the peaks of the PDN impedance curve were selected individually to optimize the decoupling capacitor positions to decrease the PDN impedance curve. This method is not suitable for PSIJ optimization, in part because the proposed methods are based on single-frequency point optimization, which means that for each optimization, only one frequency is used. However, because the PSIJ is a time-domain phenomenon, an integration process over the entire frequency band with all decoupling capacitors is necessary.

Another important issue is that PDN optimization is normally based on the target impedance definition [18]. When the target impedance is satisfied with a certain number of decoupling capacitors, the PSIJ may not be satisfied. In addition, different locations and types of decoupling capacitors that meet the target impedance also exhibit differences in terms of PSIJ. The existing studies or tools can only consider the target impedance, such that once the target impedance is met, the optimization process or search is stopped. Since PSIJ becomes significant in high-speed data transmission, the PSIJ optimization based on decoupling capacitors is needed. Therefore, the placement of the decoupling capacitors must be simultaneously optimized for all of the frequency points to reduce the PSIJ and achieve a clean power supply. Although there is a specific PSIJ requirement at an early design stage, the designers always want to meet the required eye width, which is highly related to the jitter based on different standards. The PSIJ can be reduced by optimizing the PDN.

Heuristic optimization methods have been applied for many high-dimensional nonlinear constrained optimization problems. The original groups of heuristic optimization algorithms were mostly inspired by physical or biochemical processes in the natural environment. Recent works on artificial intelligence successfully applied heuristic optimization algorithms for complex system optimization tasks, such as neural network reasoning [19], robot path planning [20], and SARS-CoV-2 drug design [21]. The genetic algorithm (GA) is one of the best known heuristic frameworks for solving such nonlinear optimization tasks. The decoupling capacitor placement optimization can be treated as a discrete constrained nonlinear optimization task. The optimization variables include the positioning and selection of the capacitors. To employ the GA algorithm to optimize the placements of the decoupling capacitors, we must mathematically define the optimization loss function of the problem. Some works based on GA for PDN design optimization have been developed [22]–[27]. In [25], the multilayer finite-element method (MFEM) combined with GA has been proposed for decoupling capacitor placement optimization, the measurement has been done to verify the MFEM method. However, the optimum number of capacitors is not considered in their fitness function. In [26] and [27], the number of decoupling capacitors is considered. However, the proposed methodology places one capacitor at each optimization run iteratively until the maximum number of capacitors reached, which consume huge amount of time because each optimization needs to be converged, and this kind of process will lose best cases regarding the optimum number of capacitors compared to optimize all capacitors at the same time. In addition, third-party software was used for the impedance calculation.

Optimizing the decoupling capacitors placement and its number in each optimization run that includes the optimum number of decoupling capacitors in the fitness function is necessarily needed for cost saving. In addition, none of the previous works have been done for PSIJ reduction by optimizing the number of decoupling capacitors and its positions. Therefore, in this article, a new target problem definition is proposed to achieve the goal of an economic number of decoupling capacitors, which can meet the target impedance or target PSIJ. With our proposed method, an optimum solution of the number of decoupling capacitors and their locations regarding the PSIJ can be obtained.

Section II presents the analytical derivations of the PSIJ, including PDN cavity models and the PSIJ transfer function. The coordinates of the decoupling capacitors are considered in the PDN resonant cavity model. The derived analytical expressions are integrated into our proposed method in Section III. Section IV examines our optimization algorithm by comparing both the PDN impedance and jitter results for two case studies. In Section V, the optimized results are verified with an HSPICE simulation. Finally, the achievements and weaknesses of the proposed method are analyzed in Section VI.

II. Jitter-Aware Analytical PDN Impedance Derivation

Analytical expressions for the PSIJ that considers the placement of the decoupling capacitors are presented in this section. The PSIJ can be reduced by optimizing the coordinates and number of decoupling capacitors through the derived expressions.

A. Cavity Model-Based Matrix Expression of the Power/Ground Plane Pair With Multiple Capacitors

The cavity model's expression has been widely used to compute the impedance matrix of a power/ground pair [11], [13]

$$Z_{ij} = \frac{j\omega\mu d}{ab} \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \frac{c_m^2 c_n^2 F_{PO} F_{CO}}{k_m^2 + k_n^2 - k^2} \tag{1}$$

where a and b are the width and length of the plane pair, respectively, d is the dielectric thickness, c_m and c_n are,

respectively, the mode types and the waveguide number k, C_m and C_n are the coefficients of the mth and nth modes along the edges of the cavity, respectively, cm and cn are equal to 1 for $m, n = 0$ and $\sqrt{2}$ for $m, n \neq 0$, k is the wavenumber, $k_m = m\pi/a$, $k_n = n\pi/a$, and F_P and F_C, as calculated below, representing the port size and decoupling capacitor coordinates functions, respectively [13]

$$k = \omega\sqrt{\mu_d \varepsilon_d} \cdot \left(1 - j\left(\frac{\tan\delta + \sqrt{2/\omega\mu_c\sigma_c}/d}{2}\right)\right) \tag{2}$$

$$F_P = \operatorname{sinc}\frac{k_m W_{xi}}{2} \cdot \operatorname{sinc}\frac{k_n W_{yi}}{2} \operatorname{sinc}\frac{k_m W_{xj}}{2} \cdot \operatorname{sinc}\frac{k_n W_{yj}}{2} \tag{3}$$

$$F_c = \cos k_m x_i \cdot \cos k_n y_i \cdot \cos k_m x_j \cdot \cos k_n y_j \tag{4}$$

where (W_{xi}, W_{yi}) and (W_{xj}, W_{yj}) are the dimensions of ports i and j, both of which are very small in comparison to the plane dimension and, therefore, are ignored in this article. (x_i, y_i) and (x_j, y_j) are the coordinates of ports i and j, respectively.

Based on a matrix expression of the power/ground plane pair with multiple decoupling capacitors as developed in [28]

$$\mathbf{Z} = (\mathbf{E} + \mathbf{Z_{pg}} * \mathbf{Y_C})^{-1} * \mathbf{Z_{pg}} \tag{5}$$

where $\mathbf{E}$ is a unit matrix, and the impedance matrix $\mathbf{Z_{pg}}$ of the bare power/ground plane without any decoupling capacitors is obtained through the equation in (1). $\mathbf{Y}$ is the conductance matrix of all of the added capacitors, VRM impedance, and so on and can be expressed in a diagonal matrix as

$$\mathbf{Y} = \begin{pmatrix} 0 & 0 & 0 & \cdots & 0 \\ 0 & Y_{\mathrm{VRM}} & 0 & \cdots & 0 \\ 0 & 0 & Y_{C1} & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & Y_{CN} \end{pmatrix} \tag{6}$$

where N represents the number of capacitors applied in the PDN optimization and Y_{VRM} and Y_C represent the admittance of the VRM and the capacitors, respectively. The diagonal element will be zero if an IC port is added, such as the first element. Every component in $\mathbf{Y}$ has its own coordinate, and all of the coordinates (x, y) shown in (7) will be put into (1) to obtain the bare power/ground plane impedance $\mathbf{Z_{pg}}$ with the same size as $\mathbf{Y}$

$$(x, y) = \begin{bmatrix} x_{\mathrm{IC}} & x_{\mathrm{VRM}} & x_1 & \cdots & x_N \\ y_{\mathrm{IC}} & y_{\mathrm{VRM}} & y_1 & \cdots & y_N \end{bmatrix} \tag{7}$$

where $(x_{\mathrm{IC}}, y_{\mathrm{IC}})$ and $(x_{\mathrm{VRM}}, y_{\mathrm{VRM}})$ are the coordinates of the IC port and VRM, respectively, and (x_p, y_p) with $p = \{1, \ldots, N\}$ are the coordinates of the decoupling capacitors.

Looking from the IC port, the impedance is represented as Z_{pdn}, which is the first element of matrix $\mathbf{Z}$. The magnitude of Z_{pdn} is defined by the following expression:

$$\begin{aligned} Z_{\mathrm{pdn}}(x_p, y_p, f) &= |Z(1,1)| \\ &= \sqrt{Z(1,1)Z(1,1)^*} \end{aligned} \tag{8}$$

where $p = \{1, \ldots, N\}$ with N the number of different capacitors applied.

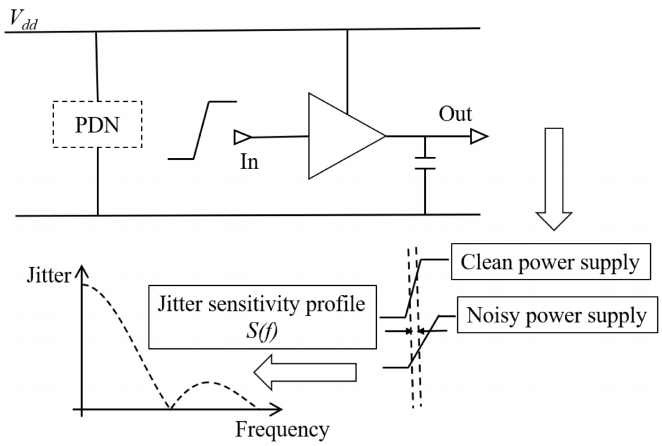

Fig. 1. Circuit system for PSIJ sensitivity transfer function establishment.

B. Frequency-Domain PSIJ Transfer Function

The jitter caused by the supply fluctuation is defined as continuous-time interval error (CTIE). The peak-to-peak value of the CTIE is used to define the PSIJ. The CTIE, as described in [30] and [31], covers all of the possible time interval error values if no fixed phase relationship is added. The frequency-domain PSIJ is determined based on two factors. One is the supply fluctuation noise spectrum $V(f)$, and the other is the dependent PSIJ sensitivity transfer function $S(f)$ [31], [32]. The following expression is usually adopted to describe the transfer relationship between the power supply fluctuations and PSIJ [7], [33]

$$J(f) = V(f) \cdot S(f). \tag{9}$$

The supply fluctuation noise can be calculated as shown in (10) when the impedance of PDN and the current spectrum are available. The current noise source can be approximated to a triangular-shaped waveform from the information of the operation mode of the CMOS inverter [30], [34]. Also, this is true for most cases generally [34], [35]

$$V(f) = Z_{\mathrm{pdn}}(x_p, y_p, f) \cdot I_{\mathrm{ICnoise}}. \tag{10}$$

The PSIJ sensitivity transfer function in a real application can be obtained through the system with PDN responding to an input stimulus, as shown in Fig. 1. By sweeping the frequency of the single-tone sinusoidal wave in a dedicated frequency band and add into the supply voltage V_{dd} as in the following:

$$V_{\mathrm{dd}} = V_{\mathrm{dd0}} + V_{\mathrm{noise}} \sin(2\pi f t) \tag{11}$$

where $f = f_1, \ldots, f_n$, V_{dd0} represents the voltage supply amplitude without add-in noise, and V_{noise} is the noise amplitude. Then, the PSIJ sensitivity transfer function can be established, as shown at the bottom of Fig. 1. The x- and y-axes represent the single-tone frequencies and the PSIJ sensitivity amplitude, respectively.

An analytical method based on propagation delay is usually used to extract $S(f)$ for the IC without PDN on the PCB. $S(f)$ is analytically expressed as a sinc function, as given the

following [36]:

$$S(f) = \frac{T_{\text{pmaxDC}} - T_{\text{pminDC}}}{\text{VDDmax} - \text{VDDmin}} \text{sinc}\left(f \frac{T_{\text{pmaxDC}} + T_{\text{pminDC}}}{2}\right) \tag{12}$$

where T_{pmaxDC} and T_{pminDC} are the maximum and minimum propagation delays from the input to the output of the chip, respectively, and VDD_{max} and VDD_{min} are the corresponding maximum and minimum dc power supplies, respectively. VDD_{max} and VDD_{min} can be extracted from either the datasheet or the operating conditions. T_{pmaxDC} and T_{pminDC} can be obtained through the datasheet or simulation of the chip circuit. With the optimized PDN impedance, the time-domain PSIJ can be obtained by using the inverse discrete Fourier transform over the frequency band, as shown in the following [7], [33]:

$$j(t) = \frac{1}{L} \sum_{n=0}^{L-1} J(f) e^{j\frac{2\pi n}{N} f} \tag{13}$$

where L represents the number of frequency points. Then, the peak-to-peak PSIJ can be obtained

$$j_{\text{pp}} = \text{Max}(j_{(t)}) - \text{Min}(j_{(t)}). \tag{14}$$

To optimize the decoupling capacitor placement in regard to the number and PSIJ, the IC current noise source and PSIJ sensitivity transfer function are assumed to be known. Therefore, the PSIJ optimization becomes a question of optimizing the integration of Z_{pdn} over the desired frequency band. As the derivations of Z_{pdn} are carried out from (1) to (8), the optimization question changes to optimize the coordinates of the decoupling capacitors to meet the PSIJ criterion with a minimum number of decoupling capacitors.

III. Optimization With Utility Maximization

Four sets of variables exist in this optimization question.

1) The frequency, which is a known discrete vector with a large size that normally includes hundreds to thousands of points, depending on the application.
2) The number of capacitors.
3) The coordinate vector variables of the decoupling capacitors, which include x and y with the same size.
4) The indexes of the capacitors, which is also a vector variable with the same size as the coordinates vector.

All of these four group variables have interacted with each other. The coordinates and indexes of capacitors are optimized over the desired frequency band to obtain a minimum number of decoupling capacitors, which can meet the target impedance or PSIJ depending on applications. To handle such a complex problem, a GA-based method can be proposed in this section to handle such a complex problem.

A. Formal Definition of the Target Problem

First, we construct a loss function by considering selection matrix of the decoupling capacitors. Our argument variables include the following.

1) The variable m encodes the action of selecting a combination of capacitors $C' \subseteq C$ from a set of capacitors $C : \{c_p \in C, p \in \mathcal{N}\}$, where p is the index of the corresponding capacitors.
2) Variables (x_p, y_p) indicate the placement position of the selected capacitor $c_p(x_p, y_p)$.

The selection matrix $\mathbf{M}$ is an encoder matrix that indicates whether or not the corresponding capacitors have been selected. We can define $\mathbf{M}$ as a binary diagonal matrix

$$\mathbf{M} = \begin{pmatrix} 1 & 0 & 0 & \cdots & 0 \\ 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & m_1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & m_N \end{pmatrix}, \quad \mathbf{m_p} \in \{\mathbf{0}, \mathbf{1}\} \tag{15}$$

where the first two diagonal elements are defined as one because they are related to the port and the VRM, which have the defined coordinates but none of the capacitors are attached. $m_p = 1$ means that the capacitor c_p is selected or vice versa. Therefore, the updated (x', y') becomes

$$(x', y') = (x, y) * \mathbf{M} \tag{16}$$

and the updated $\mathbf{Y}'$ becomes

$$\mathbf{Y}' = \mathbf{Y} * \mathbf{M}. \tag{17}$$

Next, we rewrite (5) by introducing the selection matrix (15) as

$$\mathbf{Z} = (\mathbf{E} + \mathbf{Z_{pg}}(x', y', f) * \mathbf{Y} * \mathbf{M})^{-1} * \mathbf{Z_{pg}}(x', y', f). \tag{18}$$

The magnitude of $Z_{\text{pdn}}(x', y', f, \mathbf{M})$ and $j_{\text{pp}}(x', y', f, \mathbf{M})$ can be computed through (8) and (14).

1) Target Impedance Optimization Based on the Proposed Method: The direct minimization of (8) would lead to a full selection of the available capacitors, which is not desired. Thus, we must constrain the optimization target by considering the number of capacitors selected, which would be the trace $\mathbf{tr}(\mathbf{M})$ of the selection matrix $\mathbf{M}$. By considering the number of capacitors, we now define the optimization target as

$$\begin{aligned} \underset{x,y \in \mathbf{R}^N, m_i \in \{0,1\}}{\arg\max} \quad & T(x, y, f, \mathbf{M}) \\ & = Z_{\text{pdn}}(x, y, f, \mathbf{M}) \cdot \mathbf{tr}(\mathbf{M}) \\ \mathbf{s.t.} \quad & \max(Z_{\text{pdn}}(x, y, f, \mathbf{M})) < \hat{\mathbf{z}} \end{aligned} \tag{19}$$

where $\hat{z}$ is the target impedance value that can be defined by the designer.

2) Jitter-Aware PDN Optimization Based on the Proposed Method: In high-speed applications, meeting the criterion of PSIJ is more significant than meeting the target impedance. By manipulating the target function as in (20), the PSIJ can be the criterion to meet without considering the target impedance. The optimized output will meet the PSIJ with a minimum number of decoupling capacitors

$$\begin{aligned} \underset{x,y \in \mathbf{R}^N, m_i \in \{0,1\}}{\arg\max} \quad & T(x, y, f, \mathbf{M}) \\ & = j_{\text{pp}}(x, y, f, \mathbf{M}) \cdot \mathbf{tr}(\mathbf{M}) \\ \mathbf{s.t.} \quad & \max(j_{\text{pp}}(x, y, f, \mathbf{M})) < \hat{\mathbf{j}} \end{aligned} \tag{20}$$

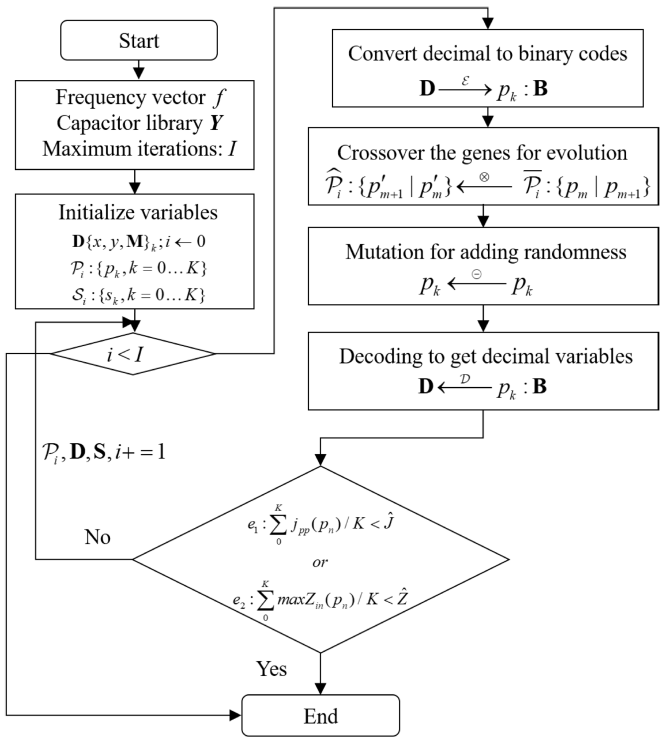

Fig. 2. Diagram for showing the GA applied for decoupling capacitor placement.

where $\hat{j}$ is the target PSIJ value that can be defined by the designer.

The defined target function leads the optimization problem to an inequality-constructed nonlinear mixture integer optimization, which can be tackled by the GA algorithm. The output of the optimization gives an economic solution to the number of decoupling capacitors.

B. GA Optimization for Decoupling Capacitor Placement

The GA algorithm is based on Charles Darwin's theory of natural selection and the principle of genetic biological inheritance. Because the frequency variable is a known vector, to leverage the GA method for capacitor placement, we must consider the variable set $\{x, y, \mathbf{M}\}$ that feeds the loss function (19) as an encoding genetic chain. The diagram Fig. 2 shows the workflow of the GA optimization process.

1) The decimal variables must be encoded as binary numbers (encoding step) during the initialization process for application to genetic operations. The encoding step converts the decimal variable set **D** into a binary code set **B**.
2) The group of different binary encoded chains (species) consists of the population set $\mathcal{P}_i\{p_n\}$ that contains the status of the different capacitors. All of the genetic chains are allocated with a score that computed from (19). The score represents the quality of the genetic chain (species). An evolution probability function $P(i, T(x, y, f, \mathbf{M}))$ is defined by the bias weight placed on the high-scoring species that leads the higher scoring species to be preferred for the selection for crossover.
3) The species are randomly sampled from the population $\mathcal{P}_i$ to generate the next generation's species. This is realized by crossover operation that two genetic chains exchange partial gene segments, as shown in Fig. 3.
4) For the crossover-generated species, a subset of species with the probability of $P_{\text{mutations}}$ is selected, and then, one bit of the genetic chain is randomly inverted and put back into the species set from which the next population $\mathcal{P}_{i+1}$ is obtained.
5) Perform the iterative evolution process until the average score of the population arrives at a certain threshold or satisfies the constraint functions.

A detailed pseudo algorithm describes in detail the full optimization procedures, which can be found in Algorithm 1. Conditions e_1 or e_2 will be used depending on applications.

IV. Jitter-Aware Decoupling Capacitor Placement Optimization

In this section, the optimization algorithm has been applied to meet the target impedance first by optimizing the coordinates and number of decoupling capacitors. Then, the algorithm is applied to optimize the PSIJ. A comparison of the two optimized results is made. A library with ten different capacitors as shown in Table I has been built, and the capacitor's information is implemented in the Z_{pdn} calculation as shown from (1) to (8) and then is included in (9)–(14) for jitter calculation. Since the selection matrix is defined in (15), which means that the capacitors used for calculated Zpdn will be selected by (15), with the definition of the target function in (20), a GA-based method can be proposed in this section to handle such a complex problem. In the experiment of this article, the capacitors' locations are varied continuously in the 2-D plane. Yet, the GA algorithm allows discrete variables or mixed continuous and discrete design variables optimization. [37].

A. Algorithm Process for Jitter-Aware Decoupling Capacitor Placement Optimization

Fig. 4 shows the workflow of the PSIJ optimization process. The general algorithm process is described as follows.

1) Compute the bare-plane PDN impedance without any capacitor in place.
2) Set the capacitor library.
3) Optimize the location and number of the decoupling capacitors.
4) Compute the optimized PDN impedance with related PSIJ.
5) If the optimized results meet the target impedance or PSIJ depends on the applications, then the process moves on to the next step; else, the process goes back to step 2, and the capacitor library must be increased.

B. Target Impedance Optimization Based on Decoupling Capacitor Placement Optimization

In this case, the target function from (19) is applied to obtain the minimum number of decoupling capacitors

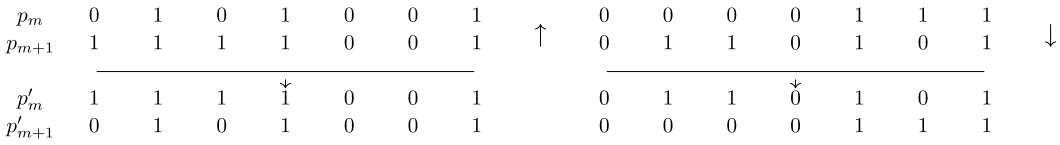

Fig. 3. Diagram demonstrating the genetic chain crossover process. Two genetic chains p_m and p_{m+1} are exchanging their gene fragments (p_m swap half-segments with p_{m+1}), resulting in two new genetic chains.

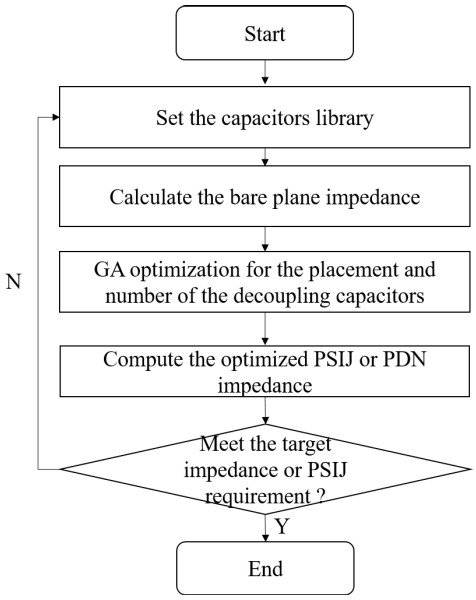

Fig. 4. Jitter-aware decoupling capacitor placement optimization methodology.

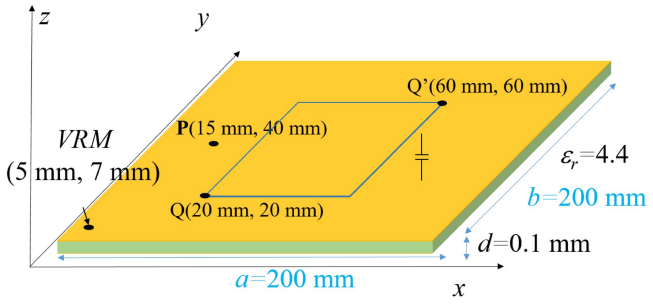

Fig. 5. Plane pair with dedicated optimization area.

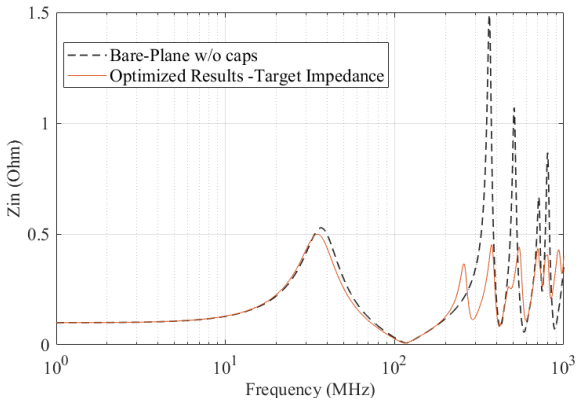

Fig. 6. Impedance comparison between the bare-plane pair and optimized results.

needed to meet the target impedance, while the PSIJ is not considered. The proof-of-concept (POC) is designed, as shown in Fig. 5. In this case, the power plane pair consists of two 200 mm × 200 mm planes with a 0.1-mm dielectric thickness, 0.035-mm conductor thickness, and dielectric constant 4.4. The input port is located at (15 mm, 40 mm) on the plane, and the VRM is located at (5 mm, 7 mm). The decoupling capacitors are placed near the port in a rectangular region from position (20 mm, 20 mm) to (60 mm, 60 mm), because for the PCB designers, an approximate region to place the capacitors is needed due to the limit of surface of the PCB. Also, this square region is flexible, and we can define even the whole board as the boundary for the capacitors. The capacitor library is set as in Table I. Specifically, ten types of capacitors are set in the capacitors library. The number of species K in the GA algorithm is set to be 300. The optimization process produces a minimum number of decoupling capacitors needed to decrease the PDN impedance curve to a value less than the target impedance. In this example, the placements of the decoupling capacitors are optimized by considering only the target impedance. The target impedance is set 0.5 Ω until 1 GHz in this case.

The impedance results, looking from Port P (15 mm, 40 mm) of the bare-plane pair without any capacitors placed, are shown as the black dashed trace in Fig. 6. After the optimization process shown in Fig. 4, the optimized results, shown as the orange solid trace, decreased the impedance curve to less than 0.5 Ω to a frequency of 1 GHz, in which case only five capacitors have been applied. Their locations are listed in Table II. In common sense, the closer the capacitor is placed to the IC port, the self-impedance/input impedance of the IC port will be smaller. Since the optimization process for the target impedance is to find the locations, types, and number of decoupling capacitors to meet the target impedance, the optimized locations of the capacitors might be different to the common sense when the target impedance is large enough. However, generally, the impedance lower than the defined target impedance by employing a minimum number of decoupling capacitors is desired. In this case, although the optimized capacitors are not very close to the IC port, the target impedance is already met. The effectiveness of the cavity model proposed in (1) has been proved by measurements in [11].

C. Jitter-Aware Decoupling Capacitor Placement Optimization Based on the Proposed Method

The same POC is applied for the jitter-aware decoupling capacitor placement optimization to obtain a comparison with

Algorithm 1 GA Optimization for PDN Capacitor Placements

Inputs: Frequency vector f; Capacitor Library $\mathbf{Y_C}$; Maximum iterations: I
Output: Last population $\mathcal{P}_n$ and score $\mathcal{S}_n$;
// PSIJ constraint, $\hat{J}$
Condition: $e_1 : \sum_0^K j_{pp}(p_n)/K < \hat{J}$
// Taget impedance constraint, $\hat{Z}$
Or **Condition**: $e_2 : \sum_0^K max Z_{in}(p_n)/K < \hat{Z}$
// Decimal to binary
Define: Encoder $\mathcal{E} : \mathbf{B} \xleftarrow{\mathcal{E}} \mathbf{R}$;
// Binary to decimal
Define: Decoder $\mathcal{D} : \mathbf{B} \xrightarrow{\mathcal{D}} \mathbf{R}$
// Sorting function: sorting array $< A|B >$ based on key array B
Define: Sort $\Omega : \mathbf{A}|\mathbf{B} \xrightarrow{\Omega} \mathbf{A}'|\mathbf{B}'$
Define: Crossover $\otimes$
Define: Mutation $\ominus$
Initialize variables $\mathbf{D}\{x, y, \mathbf{M}\}_\mathbf{k}$; $i \leftarrow 0$
$\mathcal{P}_i : \{p_k, k = 0 \dots K\}$
$\mathcal{S}_i : \{s_k, k = 0 \dots K\}$
while $NOT\ e_1 or e_2$ **do**
  // The population size is K
  for $k = 0; k < K; k++$ **do**
    // Get genetic chain $\mathbf{B}_k$
    Encoding $\mathbf{D}\{x, y, \mathbf{M}\}_\mathbf{k} \xrightarrow{\mathcal{E}} \mathbf{p_k} : \mathbf{B}\{\mathbf{x}, \mathbf{y}, \mathbf{M}\}_\mathbf{k}$
    Decoding $\mathbf{D}\{x, y, \mathbf{M}\}_\mathbf{k} \xleftarrow{\mathcal{D}} \mathbf{B}\{\mathbf{x}, \mathbf{y}, \mathbf{M}\}_\mathbf{k}$
    // Computing species score $\mathcal{S}_k$
    $s_k \leftarrow T(\mathbf{D}\{x, y, \mathbf{M}\}_\mathbf{k})$
  end
  // Sorting pairs on the scores
  $(\mathcal{P}_i|\mathcal{S}_i) \xrightarrow{\Omega} (\mathcal{P}_i|\mathcal{S}_i)$
  // Take $2 \times M$ species based on score ranking for crossover
  $\bar{\mathcal{P}}_i \xleftarrow{P(i,\mathcal{P}_i|\mathcal{S}_i)} \mathcal{P}_i$
  for $m = 0; m < 2 \times M; m + 2$ **do**
    Crossover $\hat{\mathcal{P}}_i : \{p'_{m+1}|p'_m\} \xleftarrow{\otimes} \bar{\mathcal{P}}_i : \{p_m|p_{m+1}\}$
  end
  $\mathcal{P}_i \leftarrow \hat{\mathcal{P}}_i \cup \{\mathcal{P}_i \setminus \bar{\mathcal{P}}_i\}$
  for $k = 0; k < K; k++$ **do**
    Mutation $p_k \xleftarrow{\ominus} p_k$
    Decoding $\mathbf{D}\{x, y, \mathbf{M}\}_\mathbf{k} \xleftarrow{\mathcal{D}} \mathbf{p_k} : \mathbf{B}\{\mathbf{x}, \mathbf{y}, \mathbf{M}\}_\mathbf{k}$
  end
  $i \leftarrow i + 1$
end

the results presented in the previous section. The PSIJ will meet the defined criterion after the optimization with the target function shown in (20). In this case, the target impedance is not considered, and the PSIJ criterion is defined as 3 ps. To optimize the decoupling capacitor locations to meet the PSIJ criterion, as explained in Section II, the IC noise source and the PSIJ sensitivity transfer function need to be defined first.

TABLE I
DECOUPLING CAPACITOR LIBRARY

Type	C (nF)	ESR (mΩ)	ESL (nH)
1	68	41.5	0.264
2	10	92	0.268
3	2.2	214	0.273
4	1	70	0.25
5	0.33	114	0.272
6	0.22	114	0.2
7	0.1	180	0.272
8	0.019	11.8	0.299
9	0.0082	180	0.3385
10	0.003	222.7	0.352

TABLE II
EMPLOYED DECOUPLING CAPACITORS AND LOCATIONS FOR THE PDN TARGET IMPEDANCE OPTIMIZATION

Type	C (nF)	ESR (mΩ)	ESL (nH)	**Coordinates (mm)**
4	1	70	0.25	**(40.6, 53.4)**
5	0.33	114	0.272	**(25.9, 51.8)**
6	0.22	114	0.2	**(39, 47.4)**
7	0.1	180	0.272	**(29.6, 53.1)**
8	0.019	11.8	0.299	**(34.8. 23.3)**

TABLE III
SIMULATION SETUP PARAMETERS

Characteristics	Amplitude	Period	Pulse width	Rise/Fall
Input	1.8 V	4 ns	2 ns	10 ps
Current source	80 mA	4 ns	0	1 ns
VDD	Nominal = 1.8 V, Max = 1.9 V, Min = 1.7 V			

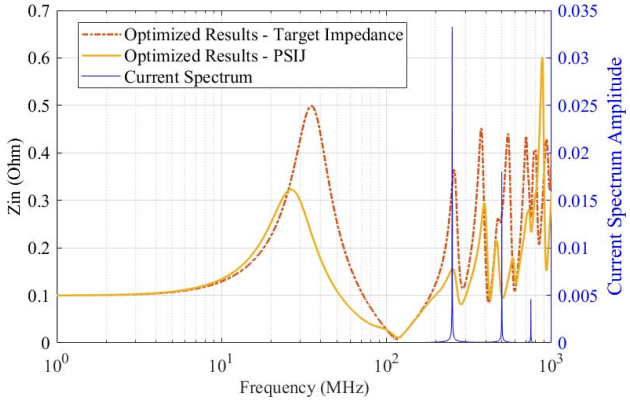

Fig. 7. Jitter-aware and target impedance optimization comparison.

1) The IC noise source is assumed to be a current source in a triangular waveform, which is generally true for most practical cases [34], [35]. The characteristics of the current source and all other required parameters in the optimization are presented in Table III. The spectrum of the current noise source is obtained through the Fourier transformation, as shown in Fig. 7, the blue dashed line on the right.
2) The PSIJ sensitivity transfer function can be obtained by substituting the values from datasheet for VDD_{max} and VDD_{min} and simulated values or analytically obtained for T_{pmaxDC}, T_{pminDC} to (1).

After the optimization process, the employed capacitors are selected, as shown in Table IV. The locations of the capacitors

TABLE IV
EMPLOYED DECOUPLING CAPACITORS AND LOCATIONS FOR THE PSIJ OPTIMIZATION

Type	C (nF)	ESR (mΩ)	ESL (nH)	**Coordinates (mm)**
2	10	92	0.268	**(29.6, 38.9)**
3	2.2	214	0.273	**(20, 46.2)**
4	1	70	0.25	**(20, 41.7)**
5	0.33	114	0.272	**(20.1, 23.1)**
6	0.22	114	0.2	**(20. 36.7)**

follow the common sense. Both the capacitors and locations are different to the previous target impedance optimization case. The optimized input impedance curve is shown as the purple solid curve in Fig. 7. The frequency-domain PSIJ is calculated by (9)–(12). The results of (10) are proportional to the resulted PSIJ. In the figure, the crossover points of the optimized results and the current spectrum, represented as the purple solid curve and the blue dashed curve, respectively, are lower than the optimization case for target impedance, shown as the orange dotted line. Theoretically, this exposes that the resulted PSIJ, in this case, will be smaller than the optimization case for target impedance. The PSIJ can be calculated for these two cases through the previously developed equations.

1) Target impedance optimization based on decoupling capacitor placement optimization

$$j_{\text{pp}} = 4.47 \text{ ps}. \tag{21}$$

2) Jitter-aware decoupling capacitor placement optimization

$$j_{\text{pp}} = 2.42 \text{ ps}. \tag{22}$$

Obviously, when the constraint region of the capacitors, board size, and target impedance changed, the decoupling scheme optimized with condition of target impedance might have lower jitter compared to that with condition of PSIJ because the target function is defined to satisfy the target impedance not the PSIJ. However, the decoupling scheme optimized with condition of PSIJ will *always* give us a jitter smaller than the target jitter because the target function is defined directly related to the PSIJ. Since our article is targeting at the jitter-aware PDN optimization, the latter is more interesting in this article.

V. JITTER-AWARE DECOUPLING CAPACITOR PLACEMENT OPTIMIZATION RESULTS VALIDATION

The HSPICE simulation is employed to prove the efficiency of our proposed optimization method. The simulation setups for different scenarios are presented, and then, the results are discussed in this section.

A. Propagation Delay and Jitter Transfer Function

In our analytical model, the linear approximated jitter transfer function in (12) is used. There are two unknown parameters T_{pmaxDC} and T_{pminDC}, which can be obtained analytically and through simulation as well. However, they have been obtained from the simulation for the simplicity in this study, because

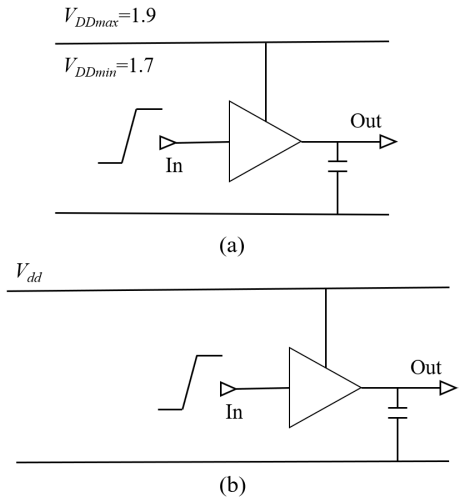

Fig. 8. Simulation setups. (a) Propagation delay. (b) Jitter transfer function.

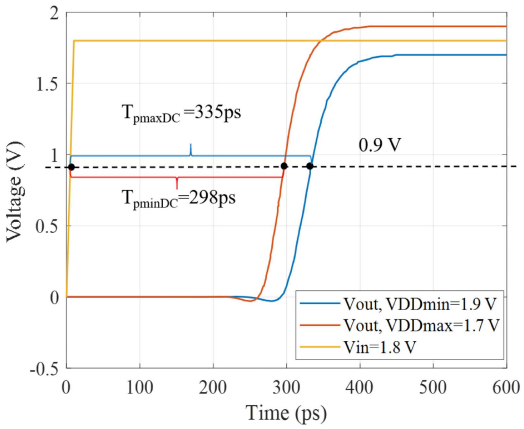

Fig. 9. Maximum and minimum propagation delays.

we are trying to validate our optimization methodology, not to validate the jitter transfer function. The simulation setup for propagation delay simulation is shown as in Fig. 8(a), the input pulse parameter is shown in Table III. The maximum and minimum propagation delays due to an unstable power supply can be simulated. As shown in Fig. 9, the propagation delays are corresponding to the supply voltage. By substituting the obtained $T_{\text{pmaxDC}} = 335$ ps and $T_{\text{pminDC}} = 298$ ps values to (12), the analytical PSIJ sensitivity transfer function can be obtained, as shown in the blue dashed line of Fig. 10.

However, the jitter transfer function is based on a linear approximation, which can fail to estimate jitter in a certain circumstance, mostly when the power noise is large enough to break the linear relationship [29]. Therefore, the jitter transfer functions were simulated for different voltage noise levels, as shown in Fig. 10. Based on the jitter transfer function definition, the simulation setup was created as shown in Fig. 8(b) with V_{dd} equal to (11). The noise voltage levels were simulated from $V_{\text{noise}} = 50$ to 500 mV with $V_{\text{dd0}} = 1.8$ V. The input parameters are the same as previous case and presented in Table III. The frequencies were swept from 1 MHz to 5 GHz with 14 steps. The simulation time step is set to be 2 ps, and the stop time is set to be 2 μs. Since it has

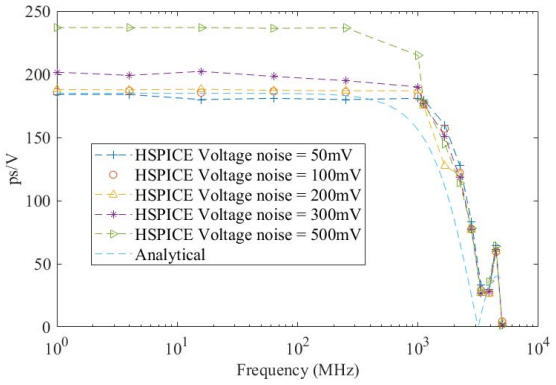

Fig. 10. PSIJ sensitivity transfer function versus noise level.

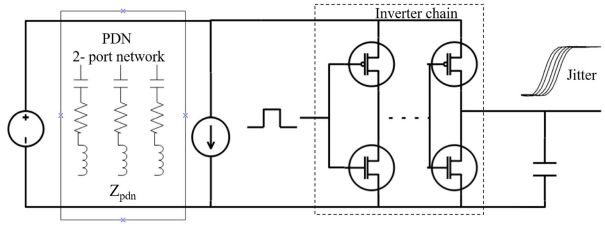

Fig. 11. Jitter simulation schematic for verification.

been proved that the jitter transfer function should be power noise independent [29], as shown in Fig. 10, the jitter transfer function curves are almost the same when the power noise amplitude is lower than 200 mV. However, when the noise level is increased from 300 mV, the low-frequency part of the jitter transfer function starts to fail. In this study, the power noise is small as the IC current noise has an amplitude 80 mA, and with our PDN impedance, the generated voltage noise level will be very small because the target impedance is limited to 0.5 Ω; even for the bare plane, the maximum amplitude is only 1.5 Ω. The generated voltage noise level will be lower than 200 mV. All these evidences prove that the linear approximated jitter transfer function would work in this study.

It is observed that the linear jitter transfer functions, obtained with voltage noise lower than 200 mV, are in good agreement with analytical ones below 3 GHz. This analytical jitter transfer function has also been verified by many articles [29]–[31]. Since the jitter caused by power voltage fluctuations is influenced by the nonideal rise time of the gate input signal and the rise time of the gate input signal is assumed to be ideally zero when deriving the linear jitter transfer function, the discrepancy occurs, which is understandable [29]. In this study, the discrepancies in high frequency can be ignored since the spectrum of this IC current noise shown as the blue dashed curve in Fig. 7 represents very low amplitude after 1 GHz.

B. Optimization Result Validation

To verify our proposed optimization method, a simple inverter chain, a modeled PDN with decoupling capacitors, and an approximated IC current noise source are employed in an HSPICE simulation, as shown in Fig. 11. The simulation time step is set to be 2 ps, and the stop time is set to be 2 μ.

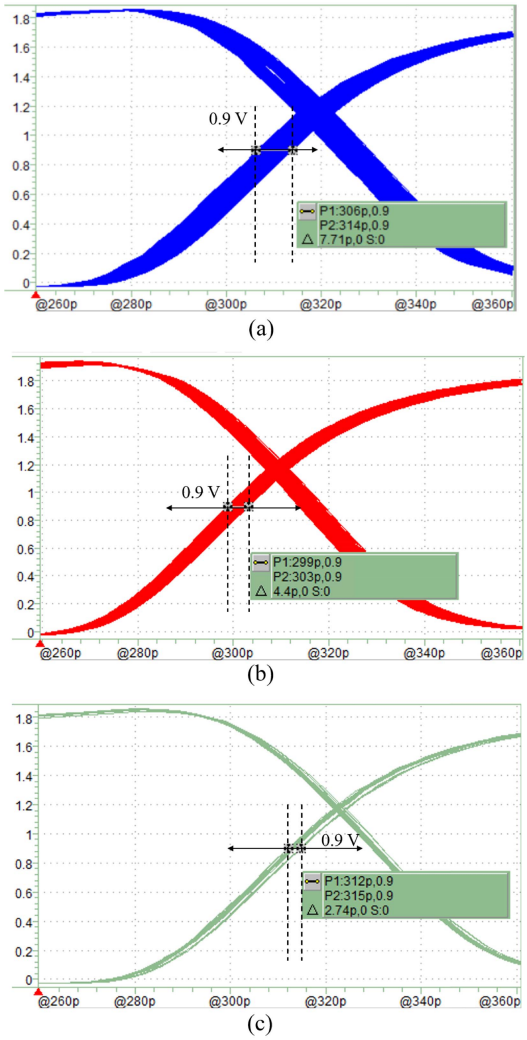

Fig. 12. (a) Plane pair without capacitors. (b) Target impedance optimized. (c) PSIJ optimized.

Since we do not have the package and die information of the buffer chain, they are not included in the buffer chain circuit we used for simulation; for simplicity, the package and die portions are ignored in this study and the VRM is modeled as an R-L circuit. However, they can be easily implemented to (8) when developing the cavity model or cascading the equivalent circuit to the cavity model. The IC current noise source and other characteristics applied in this HSPICE simulation are presented in Table III.

The optimized PDN impedance parameters are implemented in the transient simulations. Two optimized PDN cases and are studied in the HSPICE simulation as well as the case of PDN without decoupling capacitors.

1) PDN without decoupling capacitors.
2) The optimized PDN parameters without considering the PSIJ; only the target impedance requirement is considered.
3) The optimized PDN parameters considering PSIJ without considering the target impedance.

Fig. 12 shows the jitters simulated for different cases, where the jitters are measured at the amplitude equal to (VDD/2)

for the rising edges. The measured result shows a jitter with 7.71 ps for case (1) as shown in Fig. 12(a), and a jitter with 4.4 ps for case (2) as shown in Fig. 12(b), which is very close to what we calculated in Section IV-C, and the difference is within 10%. Another objective is to optimize the coordinates and indexes of capacitors over the desired frequency band to obtain a minimum number of decoupling capacitors, which can meet the PSIJ criterion, and Fig. 12(c) shows the jitter simulated by using the optimized results from case (3): 2.74 ps of jitter is measured in this case, which is also close to the calculated result in (22). The jitter values in both the analytical solution and simulation demonstrate that our proposed optimization method for the PDN network can provide an economic solution with a minimum number of decoupling capacitors to meet the target impedance or PSIJ.

VI. Conclusion

An analytical expression that combines the PDN impedance, which is related to the decoupling capacitor placement and PSIJ sensitivity function is developed. A new concept of target function definition, applied in a GA, is proposed to optimize the PSIJ or target impedance with a minimum number of decoupling capacitors. A comparison of the optimization results between the optimization with the condition of target impedance only and the optimization with conditions of PSIJ is carried out. The results show that the jitter-aware optimization method has smaller jitter compared to the target impedance optimization. When the size of board and the constraint region of the capacitor placement changed, the optimization with the condition of target impedance only might have smaller jitter than the optimization with conditions of PSIJ. However, the proposed optimization with conditions of PSIJ can always reach the PSIJ to the defined value. The optimized results are implemented in the HSPICE simulation. Both the simulated and analytical results show that the PSIJ is reduced to a similar value defined by the target PSIJ. However, because modern electronics are heading toward communication speeds as great as 100 Gb/s, a more accurate analytical model of the PSIJ transfer function is needed in further research.

References

[1] W. Arden, M. Brillouët, P. Cogez, M. Graef, B. Huizing, and R. Mahnkopf, "More-than-Moore white paper," *Version*, vol. 2, p. 14, Apr. 2010.

[2] J. Fan, X. Ye, J. Kim, B. Archambeault, and A. Orlandi, "Signal integrity design for high-speed digital circuits: Progress and directions," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 2, pp. 392–400, May 2010.

[3] J. Kim and E. Li, "Special issue on PCB level signal integrity, power integrity, and EMC," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 2, pp. 246–247, May 2010.

[4] M. Swaminathan, J. Kim, I. Novak, and J. P. Libous, "Power distribution networks for system-on-package: Status and challenges," *IEEE Trans. Adv. Packag.*, vol. 27, no. 2, pp. 286–300, May 2004.

[5] D. Brooks, *Signal Integrity Issues and Printed Circuit Board Design*. Upper Saddle River, NJ, USA: Prentice-Hall, 2003.

[6] A. B. Kahng, B. Liu, and X. Xu, "Statistical timing analysis in the presence of signal-integrity effects," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 26, no. 10, pp. 1873–1877, Oct. 2007.

[7] J. N. Tripathi, V. K. Sharma, and H. Shrimali, "A review on power supply induced jitter," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 9, no. 3, pp. 511–524, Mar. 2019.

[8] J. M. Kizer and C. J. Madden, "Method and apparatus for estimating random jitter (RJ) and deterministic jitter (DJ) from bit error rate (BER)," U.S. Patent 7 246 274, Jul. 17, 2007.

[9] I. Zamek and S. Zamek, "Jitter transformations in measurement instruments and discrepancies between measurement results," in *Proc. IEEE Int. Conf. Test*, Nov. 2005, p. 10.

[10] B. Archambeault and S. Connor, "The effect of decoupling capacitor distance on printed circuit boards using both frequency and time domain analysis," in *Proc. Int. Symp. Electromagn. Compat. (EMC)*, Aug. 2005, pp. 650–654.

[11] J. Fan *et al.*, "Quantifying SMT decoupling capacitor placement in DC power-bus design for multilayer PCBs," *IEEE Trans. Electromagn. Compat.*, vol. 43, no. 4, pp. 588–599, Nov. 2001.

[12] I. Novak *et al.*, "Distributed matched bypassing for board-level power distribution networks," *IEEE Trans. Adv. Packag.*, vol. 25, no. 2, pp. 230–243, May 2002.

[13] J. Wang, J. Lu, and Y. Li, "Placement of decoupling capacitor on packages based on effective decoupling radius," in *Proc. IEEE 18th Electron. Packag. Technol. Conf. (EPTC)*, Nov. 2016, pp. 195–198.

[14] H. Chen, J. Fang, and W. Shi, "Effective decoupling radius of decoupling capacitor," in *Proc. 10th Top. Meeting Electr. Perform. Electron. Packag.*, Oct. 2001, pp. 277–280.

[15] M. Popovich, M. Sotman, A. Kolodny, and E. G. Friedman, "Effective radii of on-chip decoupling capacitors," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 16, no. 7, pp. 894–907, Jul. 2008.

[16] I. Erdin and R. Achar, "Efficient decoupling capacitor placement based on driving point impedance," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 2, pp. 669–677, Jan. 2018.

[17] I. Erdin and R. Achar, "Decoupling capacitor placement on resonant parallel-plates via driving point impedance," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 6, pp. 2162–2171, Jun. 2019.

[18] Z. Xu, J. Wang, and J. Fan, "Decoupling capacitor placement optimization with Lagrange multiplier method," in *Proc. IEEE Int. Symp. Electromagn. Compat. Signal/Power Integrity (EMCSI)*, Jul. 2020, pp. 22–25.

[19] B. Cheng *et al.*, "Panoptic-deeplab: A simple, strong, and fast baseline for bottom-up panoptic segmentation," in *Proc. IEEE/CVF Conf. Comput. Vis. Pattern Recognit.*, Jun. 2019, pp. 12475–12485.

[20] B. K. Patle, D. R. K. Parhi, A. Jagadeesh, and S. K. Kashyap, "Matrix-binary codes based genetic algorithm for path planning of mobile robot," *Comput. Electr. Eng.*, vol. 67, pp. 708–728, Apr. 2018. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S004579061630996X

[21] T. Basu. (Jun. 2020). *Genetic Algorithm-Based Docking of Potent Inhibitors Against SARS-CoV-2 Main Protease: A Comparison Between Natural Products and Synthetic Drugs*. [Online]. Available: https://chemrxiv.org/articles/preprint/Genetic_Algorithm-Based_Docking_of_Potent_Inhibitors_Against_SARS-CoV-2_Main_Protease_A_Comparison_Between_Natural_Products_and_Synthetic_Drugs_/12526592/1

[22] I. Erdin and R. Achar, "Multipin optimization method for placement of decoupling capacitors using a genetic algorithm," *IEEE Trans. Electromagn. Compat.*, vol. 60, no. 6, pp. 1662–1669, Dec. 2018.

[23] K.-B. Wu, A.-S. Liu, G.-H. Shiue, C.-M. Lin, and R.-B. Wu, "Optimization for the locations of decoupling capacitors in suppressing the ground bounce by genetic algorithm," in *Proc. PIERS*, Hangzhou, China, 2005, pp. 411–415.

[24] K. Shibasaka, K. Kanazawa, and M. Yasunaga, "Decoupling-capacitor allocation problem solved by genetic algorithm," in *Proc. IEEE Electr. Design Adv. Packag. Syst. Symp. (EDAPS)*, Dec. 2013, pp. 225–228.

[25] J. Y. Choi and M. Swaminathan, "Decoupling capacitor placement in power delivery networks using MFEM," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 10, pp. 1651–1661, Oct. 2011.

[26] F. de Paulis, R. Cecchetti, C. Olivieri, and M. Buecker, "Genetic algorithm PDN optimization based on minimum number of decoupling capacitors applied to arbitrary target impedance," in *Proc. IEEE Int. Symp. Electromagn. Compat. Signal/Power Integrity (EMCSI)*, Jul. 2020, pp. 428–433.

[27] R. Cecchetti, F. de Paulis, C. Olivieri, A. Orlandi, and M. Buecker, "Effective PCB decoupling optimization by combining an iterative genetic algorithm and machine learning," *Electronics*, vol. 9, no. 8, p. 1243, Aug. 2020.

[28] J. Wang, J. Lu, X. Chu, Y. Liu, and Y. Li, "Modeling of multilayered power/ground planes based on resonant cavity algorithm," *IEEE Access*, vol. 6, pp. 67360–67372, 2018.

[29] C. Hwang, J. Kim, B. Achkir, and J. Fan, "Analytical transfer functions relating power and ground voltage fluctuations to jitter at a single-ended full-swing buffer," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 1, pp. 113–125, Jan. 2013.

[30] Y. Sun, J. Kim, M. Ouyang, and C. Hwang, "Improved target impedance concept with jitter specification," *IEEE Trans. Electromagn. Compat.*, vol. 62, no. 4, pp. 1534–1545, Aug. 2020.
[31] J. N. Tripathi, R. Achar, and R. Malik, "Efficient modeling of power supply induced jitter in voltage-mode drivers (EMPSIJ)," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 10, pp. 1691–1701, Oct. 2017.
[32] H. Kim, J. Fan, and C. Hwang, "Modeling of power supply induced jitter (PSIJ) transfer function at inverter chains," in *Proc. IEEE Int. Symp. Electromagn. Compat. Signal/Power Integrity (EMCSI)*, Aug. 2017, pp. 591–596.
[33] H. Lan, R. Schmitt, and C. Yuan, "Prediction and measurement of supply noise induced jitter in high-speed I/O interfaces," in *Proc. DesignCon*, Santa Clara, CA, USA, 2009, pp. 7–9.
[34] H. J. M. Veendrick, "Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits," *IEEE J. Solid-State Circuits*, vol. SSC-19, no. 4, pp. 468–473, Aug. 1984.
[35] J. Kim *et al.*, "Closed-form expressions for the maximum transient noise voltage caused by an IC switching current on a power distribution network," *IEEE Trans. Electromagn. Compat.*, vol. 54, no. 5, pp. 1112–1124, Oct. 2012.
[36] X. J. Wang and T. Kwasniewski, "Propagation delay-based expression of power supply-induced jitter sensitivity for CMOS buffer chain," *IEEE Trans. Electromagn. Compat.*, vol. 58, no. 2, pp. 627–630, Apr. 2016.
[37] V. B. Gantovnik, C. M. Anderson-Cook, Z. Gürdal, and L. T. Watson, "A genetic algorithm with memory for mixed discrete–continuous design optimization," *Comput. Struct.*, vol. 81, no. 20, pp. 1–22, 2003.

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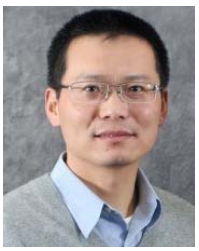

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Dr. Fan served as a member of the Board of Directors, the Chair for the Technical Advisory Committee, the Chair for the TC-9 Computational Electromagnetics Committee, and a Distinguished Lecturer for the IEEE EMC Society. He is currently an Associate Editor of the IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY and *IEEE Electromagnetic Compatibility Magazine*. He was the Technical Paper Chair and the Technical Program Chair for a few IEEE International Symposia on EMC, the General Chair for the IEEE International Conference on Signal and Power Integrity, the Founding Chair for the SC-4 EMC for Emerging Wireless Technologies Special Committee, and so on. He received the IEEE EMC Society Technical Achievement Award in August 2009.