Transient Analysis of ESD Protection Circuits for High-Speed ICs

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***Abstract*—Electrostatic discharge (ESD) failures in high-speed integrated circuits (ICs) cause critical reliability problems in electronic devices. Transient voltage suppressor (TVS) diodes are installed on high-speed I/O traces to improve system-level ESD protection. To protect the circuit, the majority of ESD current must flow into the external TVS diode rather than into the IC, but due to turn-ON behavior, the TVS diode may not snap back when needed and the IC's internal protection may take most of the current. These race conditions between the internal and external ESD protection circuits were investigated for a universal serial bus(USB) interface board. The transient turn-ON behavior of the on-chip and off-chip protection circuitry was characterized by measurements and by system efficient ESD design (SEED) simulations. The effect of transmission line pulses (TLP pulses) and power supply voltages of different sizes on the response of the protection circuitry were monitored and compared with SEED simulations. SEED models showed good agreement with measurements and were used to study the impact of passive components added to a high-speed trace or within the IC package on the ESD protection response. Results show the importance of properly accounting for the parasitic resistance and inductance between the on-chip diode and off-chip TVS diode, as well as the length of the transmission line when choosing the external TVS device. Results also show that testing must be performed using mid-level events to account for possible problems due to race conditions.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection, filter, integrated circuit (IC), system-level ESD, transient voltage suppressor (TVS).**

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I. Introduction

FAILURE of a high-speed integrated circuit (IC) resulting from an electrostatic discharge (ESD) event is one of the main reliability issues in electronic products. While it is possible to entirely protect the IC using on-chip circuitry, on-chip protection components are area intensive and costly, so they are typically only made large enough to protect against the smaller ESD events present during IC handling and not against the high-voltage ESD pulses present at the system-level. Different kinds of ESD protection circuits exist for the input/output, power bus, and radio frequency(RF) pins of complementary metal-oxide semiconductor(CMOS) ICs [1]–[5]. A silicon-controlled rectifier (SCR) device is often used in the input/output pads of high-speed ports of a CMOS IC to protect the ports against ESD damage [6]–[11]. The low-voltage-trigger SCR was invented to reduce the switching voltage of the SCR device [9], [10] and to optimize the trigger criteria [12]–[16]. Within emerging high-speed and high pin-count ICs, the design of area-efficient on-chip protection circuits with high ESD performance is a major challenge due to the large size of the required on-chip protection and the substantial parasitics that are often associated with them [1]–[5].

Fig. 1 illustrates an ESD protection scheme for a high-speed datalink I/O pin. The ESD protection diodes limit the overshoot and undershoot resulting from large over or under voltage stresses. Ideally, the off-chip protection device should carry the ESD current to the ground before this current can reach the IC's ports. This only happens through proper selection of the off-chip diode, however, often along with optimization of other design factors derived from system-level ESD simulations. The presence of passive components, i.e., a series resistor, inductor, common mode choke, or transmission line, between the off-chip diode and on-chip diodes helps to provide added voltage drop at the off-chip TVS diode. As a consequence, it is more likely the TVS diode turns ON, takes the majority of the ESD current, and protects the IC. The key contributors influencing a robust ESD design include V_{dd}, passive components on the datalink between the off-chip and on-chip diodes, the trace length, and the inductive behavior of the high-speed transmission line and IC package. This information along with the quasi-static *I–V* curves for both the off-chip and on-chip diodes (obtained with a transmission line pulser (TLP) for different pulse rise

times) determines, the protection strategy for the high-speed data link.

A device- and circuit-level ESD model is presented in this article to better predict these situations and to evaluate the ESD robustness of the protection devices. Preferably, the ESD model can describe not only the transient turn-on behavior of the components, but also their dc and ac performance. Substantial research has previously been conducted to perform system efficient ESD design (SEED) and simulation for ESD protection circuits [18]–[22]. These studies did not consider the on-board impedances and trace lengths that are part of the ESD coupling path and the associated impact of the rise-time of the voltage waveforms seen at the IC pin on TVS performance. The ESD protection devices switch from high resistance to low resistance during an ESD event, which can cause convergence difficulties during the simulation. Further, many ESD snapback models use an empirical piecewise linear model, and "if-else" statements in the code used to model the behavior, which may induce convergence issues [23], [24]. The previously published materials are unable to capture dynamic effects like overshoot, reverse recovery, and self-heating along with a nonoscillating time-domain response. ESD designers need to have one complete ESD model that can accurately predict the dc, ac, and transient dynamic characteristics for both device-level and circuit-level evaluation.

The work presented in this article attempts to address these issues by predicting circuit-level ESD responses and validating simulations through measurements. In the following sections, a successful characterization of the ESD protection circuit for a high-speed USB 3.x repeater is reported, targeting the transient turn-ON behavior of the on-chip and off-chip protection. The rest of this article is organized as follows. Section II describes the device operation and the selection of the off-chip TVS diode based on its quasi-static *I–V* curve. Section III discusses the simulation and measurement results and covers some practical notes for the protection circuitry. Finally, Section IV concludes this article.

II. ESD Protection Circuits for High-Speed ICs

A. Snapback Device and I–V Characteristics

Snapback type protection devices are generally capable of handling higher currents than non-snapback schemes [25]. The grounded-gate NMOS, grounded-coupled NMOS, and SCR are ESD protection devices which use snapback mechanisms [25]. A typical *I–V* characteristic of a snapback ESD device for a positive event voltage is given in Fig. 2. These characteristics can be seen in both off-chip and on-chip SCR diode devices. During normal operation, the snapback diode has a high resistance and turns ON when a voltage greater than the trigger voltage of the diode (V_{t1}, I_{t1}) is applied. When the applied voltage exceeds the trigger voltage, the ESD device experiences snapback and a large amount of current will flow through the device, but at a lower voltage.

If the holding voltage (V_h, I_h) is maintained, the device will remain in the snapback mode and incur no damage unless the current level becomes high enough to cause a secondary breakdown or thermal runaway after reaching (V_{t2}, I_{t2}). In this case, resistivity increases with temperature due to mobility

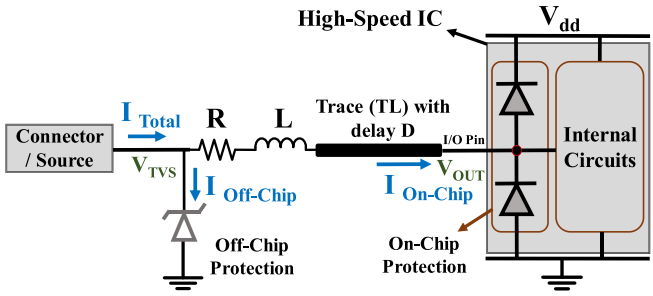

Fig. 1. Proposed ESD protection circuit for an I/O pin of a high-speed IC.

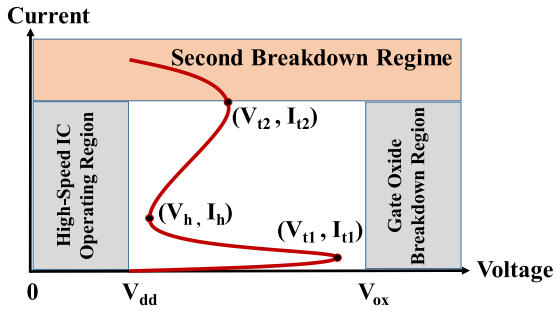

Fig. 2. Typical *I–V* characteristic of a snapback ESD protection device.

degradation, but the intrinsic carrier concentration also increases with temperature, which results in an overall reduction in the device resistivity. The positive feedback between temperature and resistivity ultimately results in device failure. The current level of the second breakdown I_{t2} is dependent on the ESD pulsewidth [26]. After the second breakdown happens, the device behaves like a resistor. Without loss of generality, the second breakdown and thermal runaway regime are not considered in the following discussion for on-chip and off-chip protection device selection.

B. Unidirectional and Bidirectional Diodes

The selection of the off-chip diode has a significant impact on the overall protection strategy and should be based on the on-die protection behavior. These selections fall into different categories based on the uni/bidirectional behavior of the protection diodes as well as its value of V_t, V_h (for snapback devices), and its dynamic resistance R_{DYN}. A bidirectional ESD structure is needed to protect an I/O pin with an operating voltage ranging between negative and positive values [27]. Fig. 3 shows the simplified *I–V* behavior of a bidirectional snapback diode [see Fig. 3(a)], a unidirectional snapback diode [see Fig. 3(b)], and a unidirectional non-snapback diode [see Fig. 3(c)] known as a Zener diode. The dynamic resistance (R_{DYN}), forward operating point (V_F, I_F), triggering point (V_t, I_t), holding point (V_h, I_h), and Zener point (V_Z, I_Z) are shown in the figures [29].

Fig. 4 shows two protection schemes for an off-chip TVS device connected to a high-speed IC with on-chip diode protection. The on-chip ESD network should provide clamping which assists with both overvoltage protection as well as chip functional performance. This network is placed in the I/O pads and can be constructed to provide ESD protection from multiple types of ESD events [6]. Here, it is assumed that the on-chip

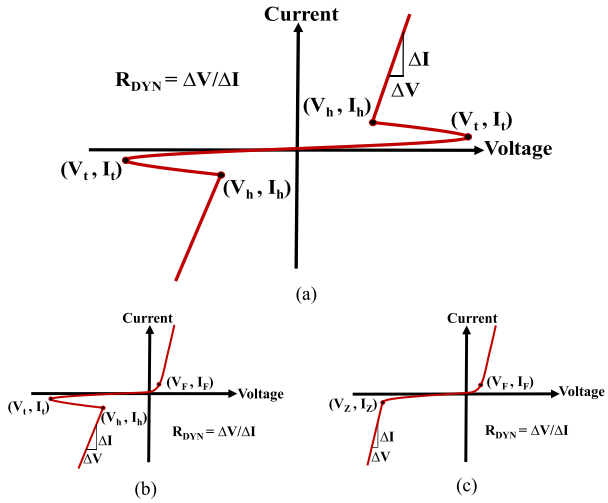

Fig. 3. Typical *I–V* characteristic of protection diodes. (a) Bidirectional snapback diode. (b) Unidirectional snapback diode. (c) Unidirectional nonsnapback diode.

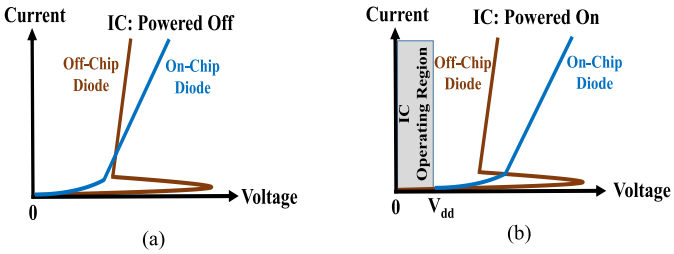

Fig. 4. Simplified illustration of the behavior of an external TVS diode and an internal protection circuit for a high-speed IC. (a) Powered OFF IC. (b) Powered ON IC.

protection network is a dual-diode which can provide protection against both positive and negative ESD events while the off-chip protection is a TVS diode with snapback behavior. Fig. 4(a) shows a method of protecting a high-speed data pin with a dual-diode protection scheme (on-chip diode) using a TVS diode (off-chip diode). Under certain situations which provide sufficient voltage drop over the TVS diode, the off-chip diode is likely to take the high current under the ESD stress for a powered-OFF IC. The situation is better for a powered-on IC when the *I–V* curve of the on-chip diode is shifted to higher voltages as shown in Fig. 4(b). Considering the high-trigger voltage requirement for SCR devices, and the requirement for low R_{DYN}, the selection of the proper TVS diode is complex. The turn-ON time of the protection device is particularly important if it is to react during the overshoot of the ESD pulse [30]. The selection of an off-chip diode using only the quasi-static *I–V* curve of the on-die protection circuit may be insufficient to protect against all ESD events. In the next sections, we will see that for "mid-sized" ESD events, the on-chip diode may turn on at a level that exceeds its current-carrying capacity without triggering the off-chip TVS diode. Even when the off-chip TVS diode turns ON, the turn-ON time is longer for small events than for large events which may cause problems for the on-chip protection circuitry.

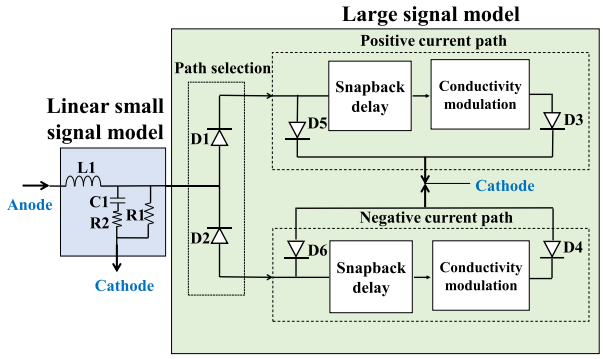

Fig. 5. Transient behavior model for a TVS diode.

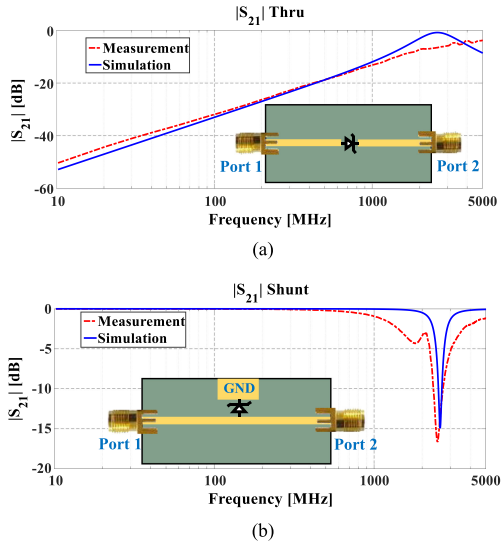

Fig. 6. Measured and simulated *S*-parameter curves for the on-chip diode. (a) |*S*21| Thru. (b) |S21| Shunt.

C. Simulation Framework

A simulation model has been developed to predict the ESD response and to characterize the turn-ON behavior of the on- and off-chip diodes for the ESD protection circuit. The simulation framework was adopted from [19]–[22]. To model the transient behavior of the TVS diodes, a symmetric model accounting for both charge polarities was applied as shown in Fig. 5.

The model includes the device's small-signal parasitic behavior as derived from S-parameter data (see Fig. 6). The large-signal model is separated into negative- and positive-current submodels (D1 and D2), preclamping models (D5 and D6), TVS turn-on behavior models (snapback delay model and conductivity modulation model), and a quasi-static *I–V* model for the behavior after the device is turned ON (D3 and D4). After the TVS diode is turned on, the device can be modeled as a *P-N* diode, as shown by D3 and D4, to capture the quasi-static *I–V* curve behavior of the device, as derived from TLP measurements.

SEED simulations were performed with Agilent ADS using transient simulations under TLP excitations. Fig. 7 shows a typical SEED simulation framework to characterize each device. For simplicity in drawing some of the figures in this article, the TLP model is represented with a dashed box.

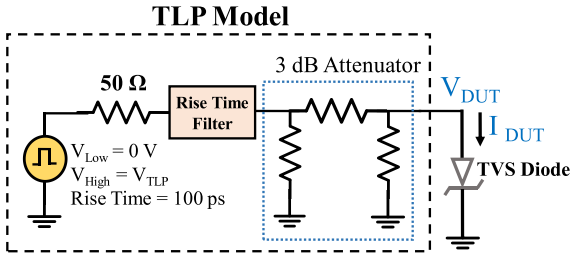

Fig. 7. SEED simulation framework to characterize the ESD protection device.

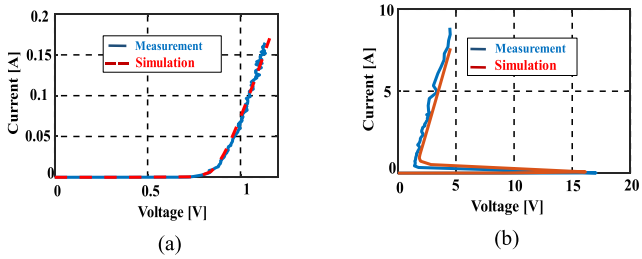

Fig. 8. Measured and simulated quasi static *I–V* curves. (a) On-chip diode [31]. (b) Off-chip diode [32].

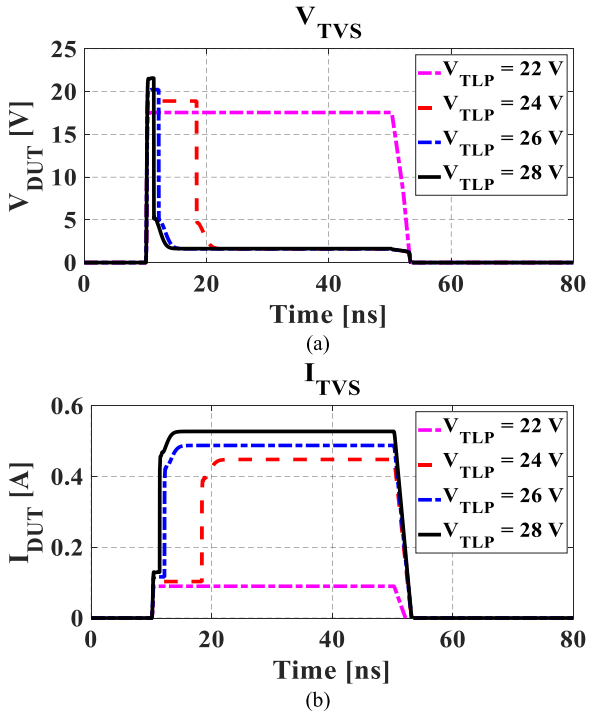

Fig. 9. Simulation results for transient response of the off-chip TVS diode for different TLP voltage levels with 40 ns wide pulse. (a) Voltage waveforms. (b) Current waveforms.

The *I–V* simulation and measurement data for the on-chip and off-chip diodes used in this article are shown in Fig. 8(a) and Fig. 8(b), respectively. The figures confirm a good match between the simulation and measurement results. The diodes were characterized using a standard TLP system (100 ns pulse width). An ESDEMC TLP-1000 transmission line pulse generator with 400 ps rise time was used in the measurements. The pulse should be long enough to capture the static voltage level, as determined from the average value from 70% to 90% of the total pulse length. The accuracy of the SEED simulation model can be evaluated by comparing the quasi-static *I–V* curves and time domain waveforms obtained from simulation and measurement during TLP injection. The simulation framework and ways to get a good match between the simulation and measurement results for both the transient peak voltage value and the quasi-static *I–V* curve is discussed in [22].

Fig. 9 illustrates the simulated transient voltage and current responses of the off-chip TVS diode from a 40 ns TLP excitation. A low V_{TLP} voltage cannot trigger the TVS diode. By increasing the V_{TLP} voltage, the carrier concentration in the high-resistance region increases, causing its resistivity to decrease. As a result, its forward voltage drop decreases, causing the TVS diode to act as a protection device with low on-state voltage. The increase in conductivity (reduction in resistivity) during a conduction period is called conductivity modulation. For higher V_{TLP} voltages, the inductive overshoot dominates, resulting in a higher peak voltage as shown in the voltage waveform plots. In practical measurements at higher current levels of device operation, the resistance is not constant and the injected free charge also changes with increasing temperature due to self-heating. Temperature related phenomena are important, but can substantially increase the complexity of the SEED modeling framework. Here we considered only the operation of the device at room temperature, and for relatively short, relatively low current events, where self-heating was not significant.

As illustrated in these plots, adequate simulation models have been developed to predict the transient response and turn-ON behavior of the on- and off-chip protection devices of a USB IC, as will be discussed next. Different cases are compared through measurements as shown in Section III.

D. Race Condition and the Effect of Rise Time Filters

Whether the on-chip or the off-chip diode turns on depends on the rise-time of the pulse and the inductance between the diodes. The pulse rise-time may be much slower than a typical ESD pulse because of the filtering that occurs in the system. The point at which the discharge occurs usually is not at the connections to the IC, but, instead, to the case of the product or to the contact of a plug. There is often a length of conductor between this point and the victim IC that has significant inductance. This inductance slows the rise-time of the discharge current, which decreases the chance of turning on the off-chip TVS diode and therefore puts the USB IC at risk. This problem is demonstrated with a simple circuit in this section. The simulation model follows the model shown in Fig. 1, with the source represented by the TLP model, R $= 0.5\ \Omega$, L $= 0$ nH, and the trace as a 50-Ω transmission line with $D = 0.5$ ns. The protection device switches from high resistance to low resistance during an ESD event which causes multiple reflections in the high-speed transmission line. The absorptive rise time filter in the TLP system helps to attenuate the multiple reflections between the TLP source and DUT. To quantify the effect of the rise-time of the incoming pulse on the response

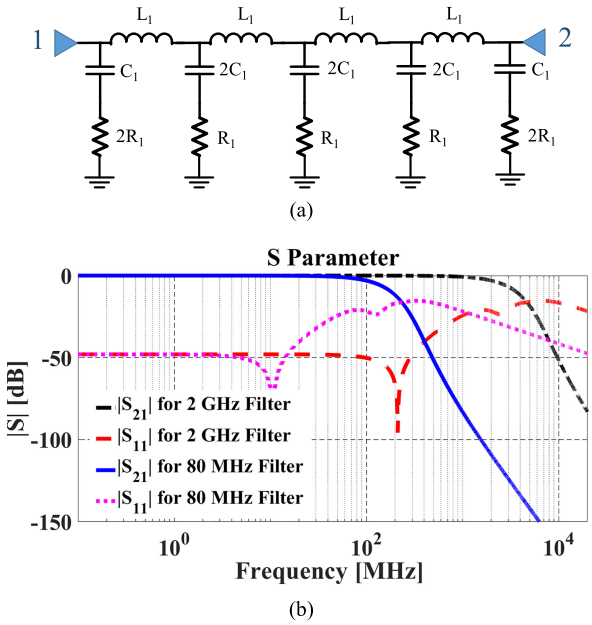

Fig. 10. Absorbtive low pass filters represented as rise-time filters. (a) Circuit model. (b) Frequency response. For 2 GHz filter, $R_1 = 25\ \Omega$, $L_1 = 2.37$ nH, and $C_1 = 0.475$ pF, and for 80 MHz filter, $R_1 = 25\ \Omega$, $L_1 = 59.25$ nH, and $C_1 = 11.87$ pF.

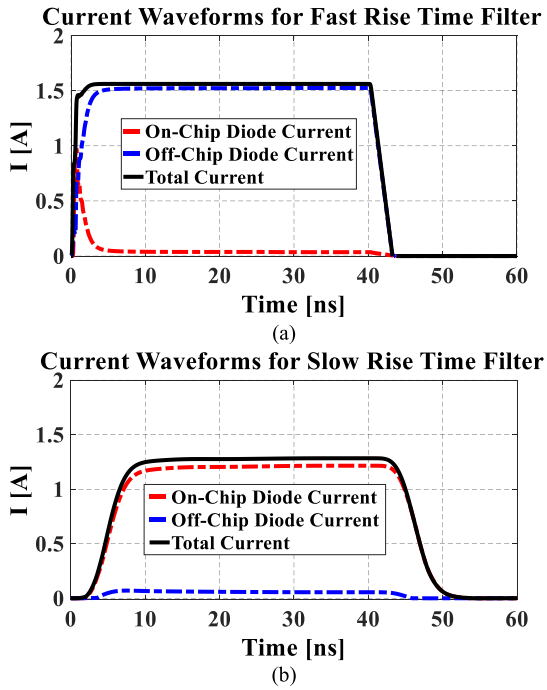

Fig. 11. Simulated current waveforms with different rise-time filters for a 40 ns wide TLP pulse. (a) 2 GHz filter. (b) 80 MHz filter.

of the diodes, two different fourth-order absorptive low-pass RLC filters were placed in series with the TLP model. The filters, a 2 GHz low-pass filter and an 80 MHz low-pass filter, are shown in Fig. 10(a). The frequency responses of these filters are plotted in Fig. 10(b).

The simulated current in the on- and off-chip diodes are shown in Fig. 11 when using these two rise-time filters in the TLP model

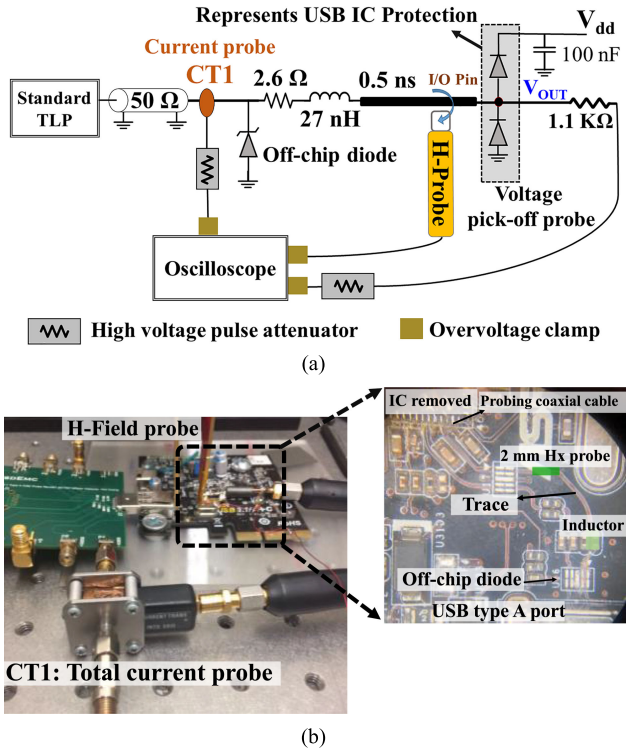

Fig. 12. Measurement setup. (a) Measurement blocks to characterize the ESD circuit. (b) Fabricated USB repeater board to characterize the race condition between the off-chip diode and on-chip diode.

with $V_{\mathrm{TLP}} = 40$ V and a 40 ns pulse width. The off-chip TVS diode turns on, takes the majority of the current, and protects the on-chip diode for the case with fast rise-time filter (2 GHz). In contrast, the off-chip TVS diode does not turn on completely and the majority of the ESD current flows to the on-chip diode when the slow rise-time filter (80 MHz) is used. Considering 1 A as the maximum current the IC can consume and remain undamaged, the chip will fail for the 80 MHz rise-time filter when $V_{\mathrm{TLP}} = 40$ V.

A comprehensive discussion about the transient behavior of the ESD circuit for high voltage pulses along with a comparison to the simulation results is presented in the following section.

III. Measurement Results

A. Measurement Procedure

A similar setup to Fig. 1 was built to experimentally characterize the ESD protection for a USB repeater board. Fig. 12 shows a block diagram and a picture of the experimental setup. The protection diodes are oriented to be blocking during the normal operation of the IC and are positioned between the I/O pin and ground, or the I/O pin and the supply voltage line.

The power supply (V_{dd}) was provided directly to the USB IC and filtered with a 100 nF on-board decoupling capacitor. In a practical application, the decoupling capacitor connected to V_{dd} may change the transient behavior of the on-chip protection devices. This effect is not considered in this article. The effect of turning the power supply off ($V_{\mathrm{dd}} = \mathrm{OFF}$) and of varying the power supply voltage V_{dd} were considered in this article. A Rohde & Schwarz (RTO-1024) oscilloscope with 2 GHz bandwidth

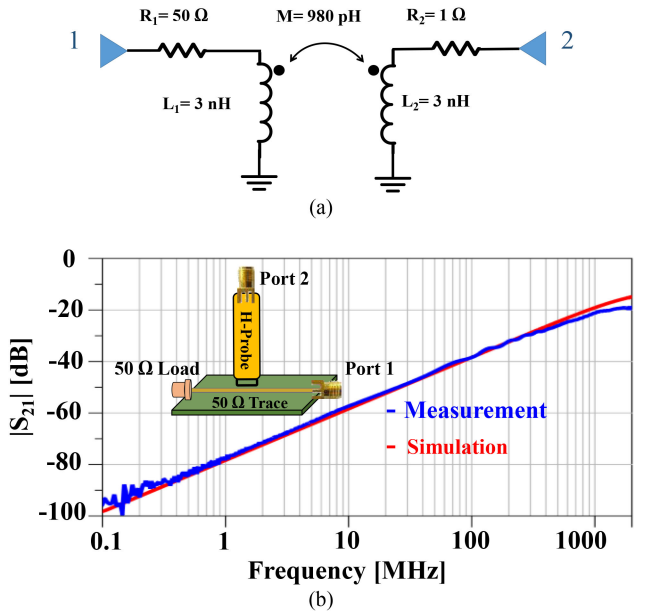

Fig. 13. H-field probe. (a) Equivalent circuit model. (b) Measured and simulated frequency response of the probe.

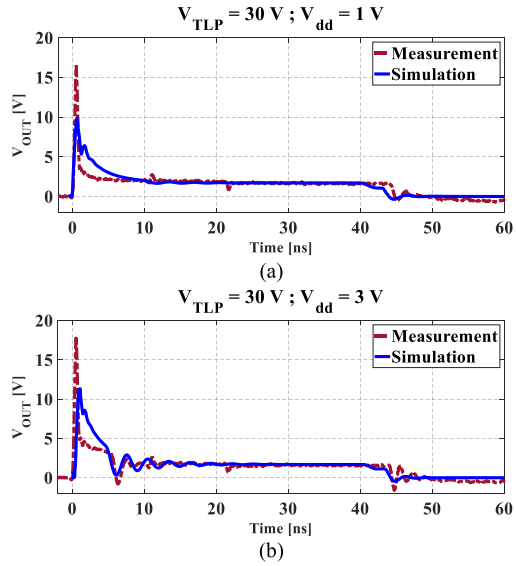

Fig. 14. Measured and simulated voltage data for the ESD protection circuit in the presence of a 30 V TLP with 45 ns pulsewidth when $R = 2.6\ \Omega$, $L = 27$ nH, and the trace is a 0.5 ns 50- Ω transmission line. (a) $V_{\rm dd} = 1$ V. (b) $V_{\rm dd} = 3$ V.

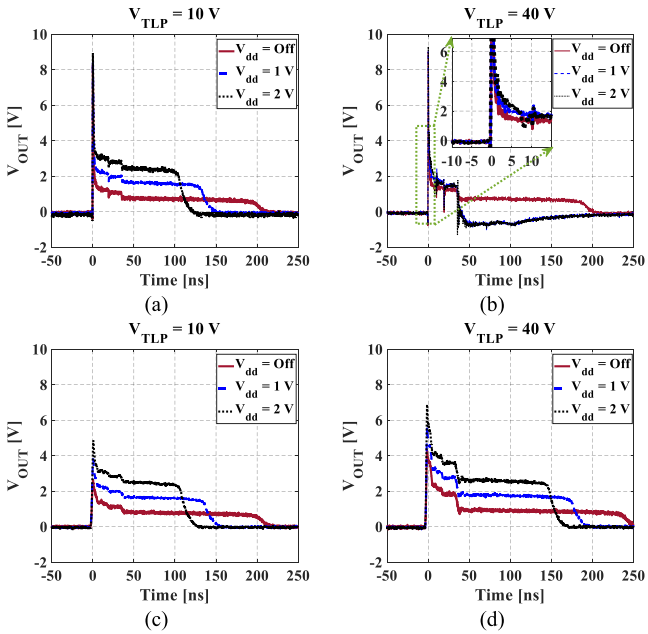

Fig. 15. Measured voltage data for the ESD protection circuit with and without a rise-time filter when R=0.5 o Ω, L=0 nH, and $D = 0.5$ ns. (a) $V_{\rm TLP} = 10$ V, without rise-time filter. (b) $V_{\rm TLP} = 40$ V, without rise-time filter. (c) $V_{\rm TLP} = 10$ V, with rise-time filter. (d) $V_{\rm TLP} = 40$ V, with rise-time filter. 30 ns wide TLP pulses were applied for each case.

and 175 ps rise time was used to capture the transient waveforms. To ensure oscilloscope safety, high-voltage pulse attenuators, and over-voltage clamps were installed in the test set-up. The voltage pick-up probe forms a voltage divider with a 1.1 KΩ series resistor and the 50 Ω input impedance of the oscilloscope. A high-bandwidth, small form-factor current probe (CT1) was used to capture the total current driven into the circuit. The printed circuit board (PCB) under test and the CT1 current probe were connected to the output of the standard TLP source using a 1.5 m long 50 Ω coaxial cable. The on-chip diode current was determined using a magnetic-field probe placed in the vicinity of the USB I/O trace. The voltage measured by the H-field probe may be used to reconstruct the on-chip diode current using the current-reconstruction technique in [28]. The equivalent circuit model of the H-field probe is shown in Fig. 13(a). The frequency response of the probe was measured and compared with circuit simulation as shown in Fig. 13(b). One can expect to capture a signal with a maximum frequency content less than 1.5 GHz using this H-field probe before unwanted E-field components begin to negatively influence results.

B. Comparison With Simulation Results

The simulation model follows the model shown in Fig. 1, with the source represented by the TLP model, $R = 2.6\ \Omega$, $L = 27$ nH, and the trace as a 50-Ω transmission line with $D = 0.5$ ns. The inductor and resistor were added to represent the impact of a common-mode choke between the TVS device and USB IC. Simulations and measurements were performed for varying voltages on $V_{\rm dd}$ as depicted in Fig. 14 using a TLP system with a 30 V amplitude and a 45 ns pulsewidth. To better analyze the waveforms in this article, the waveforms are compared for $V_{\rm dd} = 1$ V and $V_{\rm dd} = 3$ V, respectively. Under these conditions, the ESD protection circuit with $V_{\rm dd} = 3$ V provides a larger voltage drop at the off-chip TVS diode as illustrated in Fig. 14(b). Fig. 14(b) also shows that the TVS diode experienced an overshoot voltage peak (a combination of conductivity modulation and inductive overshoot), then a snapback delay before reaching the quasi static region (on-state) of the voltage clamp. Here, the on-state voltage clamp was 1.8 V. Assuming the protection TVS diode switches from high impedance to low impedance when it turns on, an oscillation occurs as a result of reflections between the turned-ON TVS diode and the (turned-ON) on-chip diode along

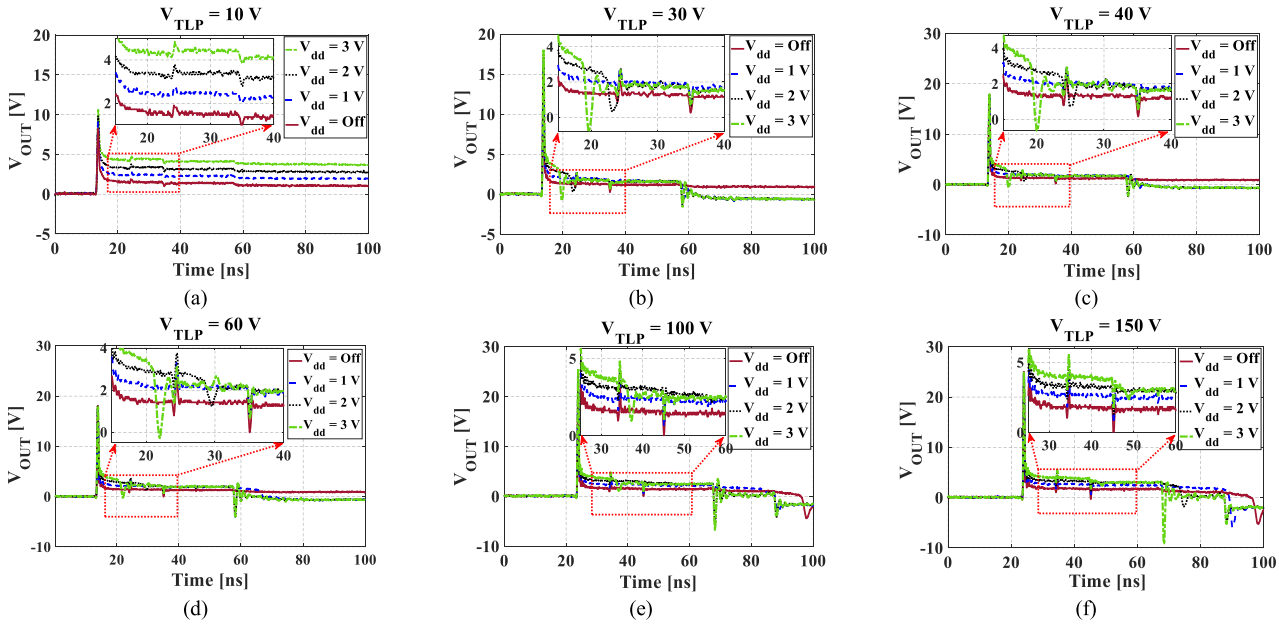

Fig. 16. Measured voltage data for the ESD protection circuit with varying $V_{\rm dd}$. (a) $V_{\rm TLP} = 10$ V. (b) $V_{\rm TLP} = 30$ V. (c) $V_{\rm TLP} = 40$ V. (d) $V_{\rm TLP} = 60$ V. (e) $V_{\rm TLP} = 100$ V. (f) $V_{\rm TLP} = 150$ V. 40 ns wide TLP pulses were applied for each case.

the transmission line (and inductor) between them. The starting point of the oscillation often corresponds with a large dip in the voltage waveform, which we have considered to be the moment when the TVS diode turns on and its current increases. For this test, this moment happened around ∼6 ns as can be seen in Fig. 14(b). The results show that the SEED simulation does a reasonable, but not perfect job of reconstructing the first peak, reconstructs the transition between the first peak and quasi static region with moderate error, and the on-state clamped voltage region with near zero error. The imperfect modeling of the coaxial cables and RF connectors, the parasitic components and insertion loss of the PCB, and the limited measurement accuracy contribute to the discrepancies between the measurement and simulation. Although the ringing in the waveforms is due to the nature of the oscillation inside the short-circuit transmission line, a portion of the ringing in the simulation is caused by the solver instabilities and setting-dependent items in ADS tool.

Fig. 14 shows two peaks relatively close together at the beginning of the voltage response waveform. The two peaks are related to conductivity modulation and to inductive overshoot. These peaks occur on different time scales. The first peak, before current begins to flow, is associated with conductivity modulation. Once current begins to flow a second peak occurs associated with inductive overshoot. This overshoot is related to the *Ldi/dt* voltage drop across the diode. At some TLP voltage levels, the scale of the conductivity modulation peak reaches that of the inductive modulation and the peaks merge. At higher TLP voltage levels the inductive overshoot dominates, resulting in a higher peak.

C. Effect of Rise Time Filters

To characterize the effect of a long rise-time pulse on the diode turn-ON, the circuit shown in Fig. 1 with the source represented

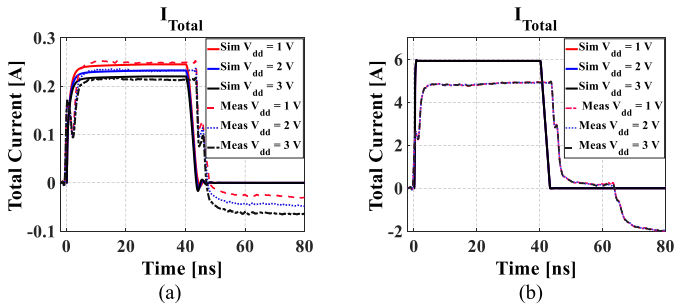

Fig. 17. Measured current into USB board when varying $V_{\rm dd}$. (a) $V_{\rm TLP} = 10$ V. (b) $V_{\rm TLP} = 150$ V. 40 ns wide TLP pulses were applied for each case.

by the TLP model, $R = 0.5\ \Omega$, $L = 0$ nH, and the trace as a 50-Ω transmission line with $D = 0.5$ ns, was subjected to a TLP pulse filtered with an 80 MHz low-pass filter. Fig. 15(a) and (b) shows the results when no low-pass filter was used. For the 10 V TLP voltage, the off-chip diode did not turn ON and all of the current flows to the on-chip USB IC. For the 40 V TLP voltage, the TVS diode turns ON when $V_{\rm dd} \geq 1$ V. The fact that the TVS diode turned on is even more obvious when Vdd ≥ 2 V and the diode snaps back to make a large dip in the voltage waveform. Once the TVS diode turns on, the curve does not show any dependence on $V_{\rm dd}$. In this case, when there are two protection paths, the on-chip diode will often begin to conduct before the TVS diode. The TVS does not turn-ON until a short time later, if at all. As a result, the initial peak in the voltage is mainly a result of conductivity modulation in the on-chip diode, which is less dependent on the size of the pulse and gives roughly the same peak value for both cases, 8.8 and 9.3 V in Fig. 15(a) and (b), respectively. Once inductive overshoot begins to dominate, the size of the peak changes more dramatically with TLP size. Fig. 15(c) and (d) shows the cases when the TLP system was

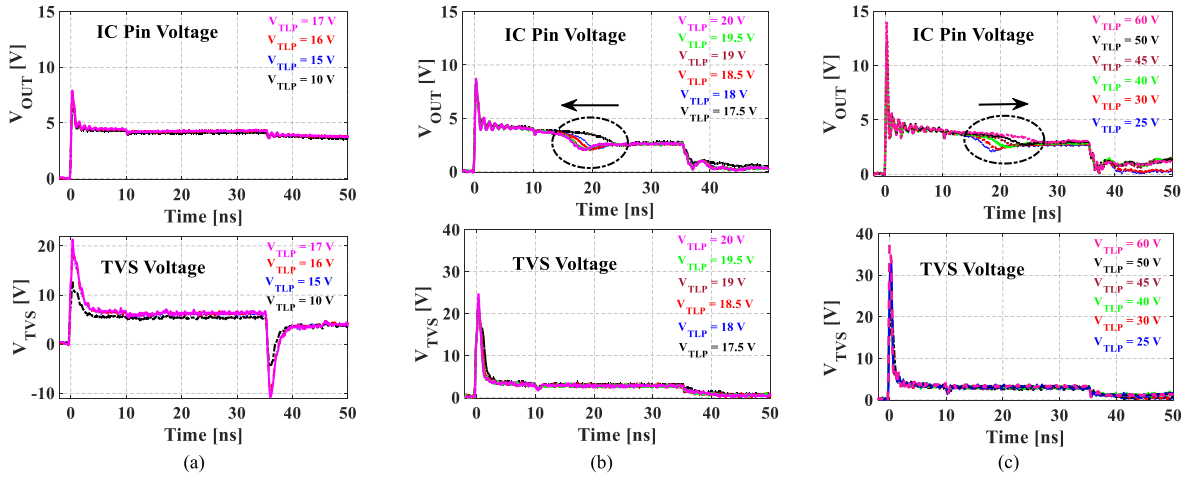

Fig. 18. Measured voltage data ($V_{\rm OUT}$ and $V_{\rm TVS}$) for the ESD protection circuit when $V_{\rm dd} = 3$ V, $R = 3\ \Omega$, $L = 27$ nH, and $D = 1$ ns. (a) Low-level TLP voltage (TVS is turned-OFF). (b) Mid-level TLP voltage (shortly after TVS turns ON). (c) High-level TLP voltage (long after TVS turns ON). The arrow indicates the movement of transition behavior with increasing TLP voltage. 35 ns wide TLP pulses were applied for each case.

filtered with an 80 MHz rise-time filter. Adding this filter reduces the peak of the voltage waveform and has a significant impact on results when the circuit is excited by a 40 volt TLP voltage and 30 ns pulsewidth as shown in Fig. 15(d). By slowing the rise time of the filter, the voltage peak at the TVS is significantly reduced, and the quasi-static voltage is not sufficient to turn ON the TVS over the time of the pulse. The quasi-static voltage (and current) seen by the on-chip diode is therefore much larger for a slow rise-time pulse than for a fast rise-time pulse. The output voltage in this case is directly related to $V_{\rm dd}$, since the on-chip diode discharges to the $V_{\rm dd}$ rail. A one volt increase in $V_{\rm dd}$ is roughly equivalent to a 40 V TLP voltage increase when the TVS diode does not turn ON. As is clear in Fig. 15(d), the TLP pulse ends at 30 ns. Since the TVS diode was turned-OFF in this case [as well as in Fig. 15(a) and (c)], the TLP current is discharged through the on-chip diodes and the $V_{\rm dd}$ rail which leads to a reverse recovery behavior after the TLP pulse ends until the stored energy is completely dissipated. This causes the pulse duration to last longer than 30 ns.

D. Transition Behavior by Varying TLP Voltages

Additional cases were considered to characterize race conditions between the on-chip and off-chip diodes. The circuit in Fig. 1 was implemented with $R = 2.6\ \Omega$, L = 27 nH, and $D =$ 0.5 ns, and subjected to 40 ns wide TLP pulses. Fig. 16 shows the waveform on $V_{\rm OUT}$ for 10, 30, 40, 60, 100, and 150 V TLP excitations with varying $V_{\rm dd}$ voltages. For low TLP voltages, the off-chip TVS diode does not turn on and the current flows to the on-chip diode. The direct dependence of $V_{\rm out}$ on the $V_{\rm dd}$ in Fig. 16(a) confirms this situation.

The TVS diode also does not turn on for the initial 10 ns of the pulse for TLP settings lower than 60 V. Despite cable reflections which impact the waveforms in certain moments, the effect of changing $V_{\rm dd}$ on the turn-ON time for the TVS diode was still observed for larger TLP settings. The ringing behavior and reverse recovery ramp-up are also important during the device forward-biased operation when the source pulse ends.

The total current into the USB port, as captured by a CT1 current probe, is shown in Fig. 17 and compared with the simulation results. Simulations match measurements reasonably well for low TLP voltages and yield acceptable results for high TLP voltages. For a low voltage TLP setting, the effect of $V_{\rm dd}$ is obvious in the total current measurement, as illustrated in Fig. 17(a) for $V_{\rm TLP} = 10$ V, indicating that only the on-chip diode turned ON. By increasing the TLP voltage, the effect of $V_{\rm dd}$ is negligible as presented in Fig. 17(b) for $V_{\rm TLP} = 150$ V. The negative current at 64 ns is caused by the interaction of the reflections from the "short" created by the ESD protection (creating a positive current reflection back toward the TLP) and the "open" at the end of the TLP transmission line (creating a negative reflection back toward the diode).

The waveforms in Fig. 16 show a transition in the trace voltage $V_{\rm OUT}$ that occurs when the system is subjected to larger TLP voltages. This transition occurs from the moment the TVS diode turns ON until the output voltage reaches the on-state voltage clamp. To better characterize the transition behavior for a high-speed USB link, experiments were performed on the circuit in Fig. 1 with $R = 3\ \Omega$, $L = 27$ nH, and $D = 1$ ns.

A 50 Ω transmission line was used in the test setup. A 50 Ω trace with $W = 9.73$ mil was designed and implemented on a FR4 substrate with $\varepsilon_r = 4.3$ and $H = 5$ mil. Compared to the circuit where $R = 2.6\ \Omega$, $L = 27$ nH, and $D = 0.5$ ns, the new circuit has a longer trace length which helps the TVS diode to turn on earlier. The voltages $V_{\rm OUT}$ (seen at the on-chip diode [33]) and $V_{\rm TVS}$ (seen at the off-chip diode [34]) were recorded when $V_{\rm dd} = 3$ V for three different conditions: low-level TLP voltage (TVS is turned OFF); mid-level TLP voltage (shortly after the TVS turns ON); and high-level TLP voltage (long after the TVS turns ON). For low TLP voltages, the off-chip diode remains turned-OFF as shown in Fig. 18(a). When the 17.5 V TLP voltage is exceeded, the off-chip TVS diode turns ON as shown in Fig. 18(b). The time when the TVS turns ON decreases

with voltage until the TLP voltage is 20 V, as shown in the plot. When the TLP voltage exceeds 20 V, the turn-ON time begins increasing with TLP voltage as shown in Fig. 18(c).

IV. Conclusion

Possible race conditions between the on-die and external ESD protection circuits for a USB interface board were investigated through measurements and SEED simulations. An understanding of the characteristics and limitations of the on-die ESD protection circuitry, as well as the trace/package parasitics, is needed to design an off-chip protection circuit for high-speed ICs. The selection of the off-chip diode using only the quasi-static *I–V* curve of the on-die protection circuit may be insufficient to protect against all ESD events. Results show that for "mid-sized" events, it is possible the on-die diode turns ON at a level that exceeds its current-carrying capacity without triggering the off-chip TVS diode. Even when the TVS turns ON, the turn-ON time is longer than for large events which may cause problems for the on-die protection circuitry. The likelihood that the external TVS is not triggered increases with long rise-time events since the voltage drop across intended or parasitic inductance between the TVS and on-chip diode is smaller than for fast rise-time event. The values of the resistance, inductance, and transmission line delay between the on- and off-chip protection circuitry are needed to optimize the TVS selection. The models developed here can be used to help make that selection. Results show that designers should perform tests at mid-range levels using pulses with slow rise-time if they are to ensure proper protection of their circuity in the case of a race condition.

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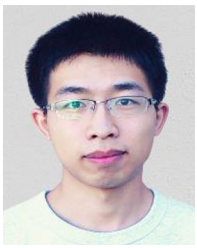

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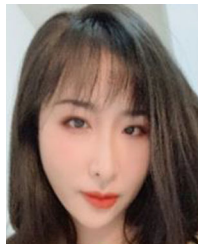

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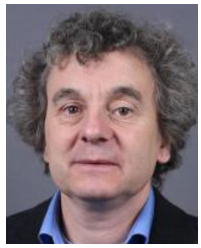

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