A 19 GHz Circular-Geometry Quad-Core Tail-Filtering Class-F VCO with −115 dBc/Hz Phase Noise at 1 MHz Offset in 65-nm CMOS

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***Abstract*—This paper presents a CMOS circular-geometry quad-core voltage-controlled oscillator (VCO) with class-F operation and tail filtering to achieve ultra low phase noise in K band. The use of class-F operation in a circular-geometry multi-core VCO further lowers phase noise but results in new mode ambiguity. We introduce cross-coupled narrow and thin metal traces in the class-F transformer secondary loop to suppress this new mode ambiguity. Also, we extend the circular geometry design to the VCO tail LC filters, reducing the chip area. A proof-of-concept prototype is fabricated in a standard 65 nm CMOS technology. In measurement, the VCO operates from 17.9 to 20.7 GHz. At 19 GHz, the VCO achieves a phase noise of −115 dBc/Hz at 1 MHz offset with a figure of merit (FoM) of −188.4 dBc/Hz.**

***Index Terms*—Class-F, coupled oscillators, harmonic, mm-wave, oscillator, phase noise**

I. Introduction

A voltage-controlled oscillator (VCO) operating near the K-band (18 to 27 GHz) is a key building block for many mm-wave applications [1]–[5]. While a high figure of merit (FoM) (e.g. [2]) or a wide tuning range (e.g. [5]) has been demonstrated, achieving a very low phase noise in CMOS remains challenging. A high clock spectral purity is essential for achieving efficient modulation and high-resolution imaging in mm-wave communication and radar systems [6], [7].

The optimal phase noise of an LC VCO is proportional to its tank inductance. Ideally, one could have an arbitrarily low phase noise without sacrificing the FoM by using a small tank inductance at the expense of large dc current [8]. In practice, there exists a lower bound for the tank inductance. Further reducing the inductance would lead to severe quality factor degradation due to destructive magnetic coupling [9] and/or parasitic losses [8]; this would significantly degrade the VCO FoM. Coupling multiple identical oscillators has been demonstrated as an effective approach to push this limit, achieving low phase noise with high FoM [3]–[5], [7]–[10]. However, the lowest achievable phase noise is still fundamentally bounded by the parasitic losses in passive components and the ever-lowering voltage headroom in nanoscale CMOS technologies.

In this work, we fuse class-F operation [11] and tail filtering [12] with a circular-geometry quad-core VCO [4], [13] for ultra-low phase noise as shown in Fig. 1. The use of class-F operation in a circular-geometry multi-core VCO further lowers phase noise, however, it results in new mode ambiguity. To suppress this new mode ambiguity, we utilize cross-coupled thin metal traces to the circular-geometry class-F transformer primary and secondary loops. Also, we extend the circular geometry design to the VCO tail LC filters, reducing the chip area. A proof-of-concept prototype is fabricated in a standard 65 nm CMOS technology. In measurement, the VCO operates from 17.9 to 20.7 GHz. At 19 GHz, the VCO achieves a phase noise of −115 dBc/Hz at 1 MHz offset with a figure of merit (FoM) of −188.4 dBc/Hz.

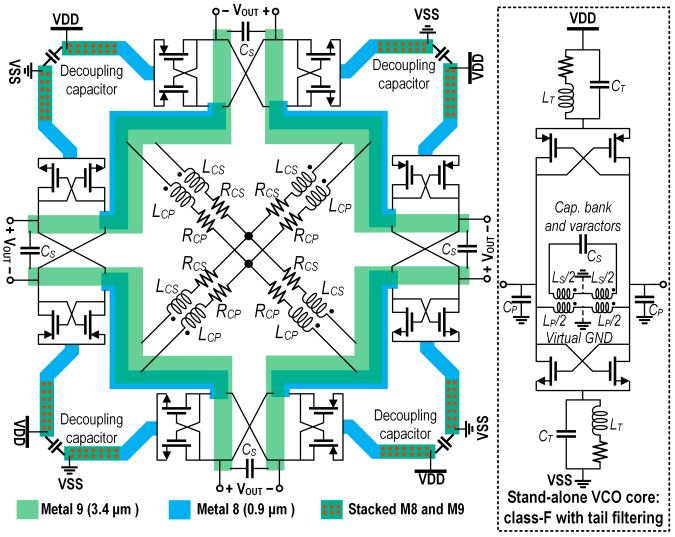

Fig. 1. Proposed CMOS circular-geometry class-F tail-filtering quad-core VCO with windmill-like cross-coupled thin metal traces (modeled as L_{CP}, R_{CP}, L_{CS}, R_{CS}, and magnetic coupling between L_{CP} and L_{CS}) in the center suppressing mode ambiguity.

II. Design Evolution and Considerations

A. Class-F VCO with Second-Harmonic Tail Filtering

Each core of our quad-core oscillator is a class-F VCO with second-harmonic tail filtering as shown in Fig. 1. The class-F operation enforces a pseudo-square voltage waveform through a transformer-based LC tank design. As a result, it lowers the phase noise by an increased fundamental amplitude and

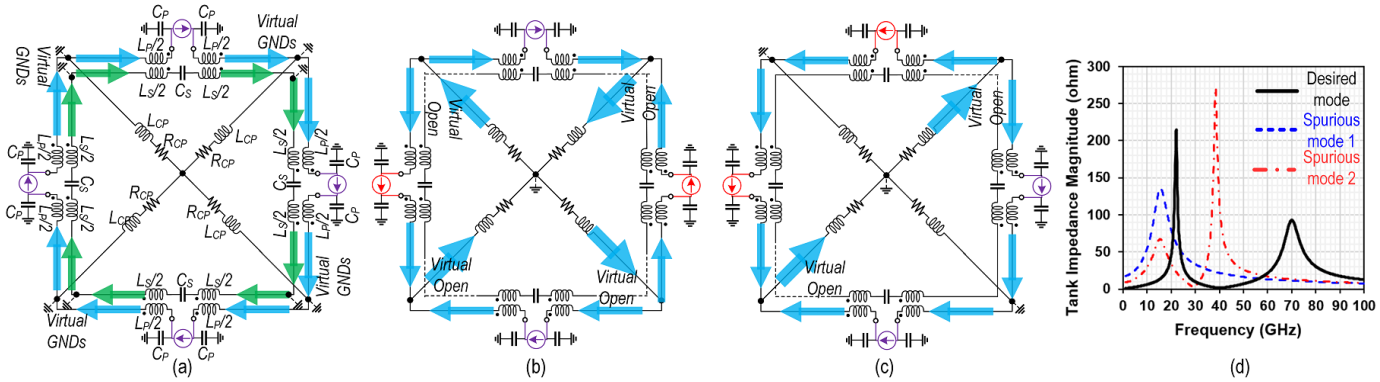

Fig. 2. Mode ambiguity in a circular-geometry quad-core class-F oscillator: current flows in (a) the desired oscillation mode, (b) the spurious mode 1, and (c) the spurious mode 2; (d) simulated differential-mode tank impedance magnitude, showing high-Q spurious modes (L_P=L_S=80 pH, k=0.78, Q_P=Q_S=15 at 20 GHz, C_P=400 fF, C_S=1 pF, L_{CP}=100 pH, and Q_{CP}=3 at 20 GHz).

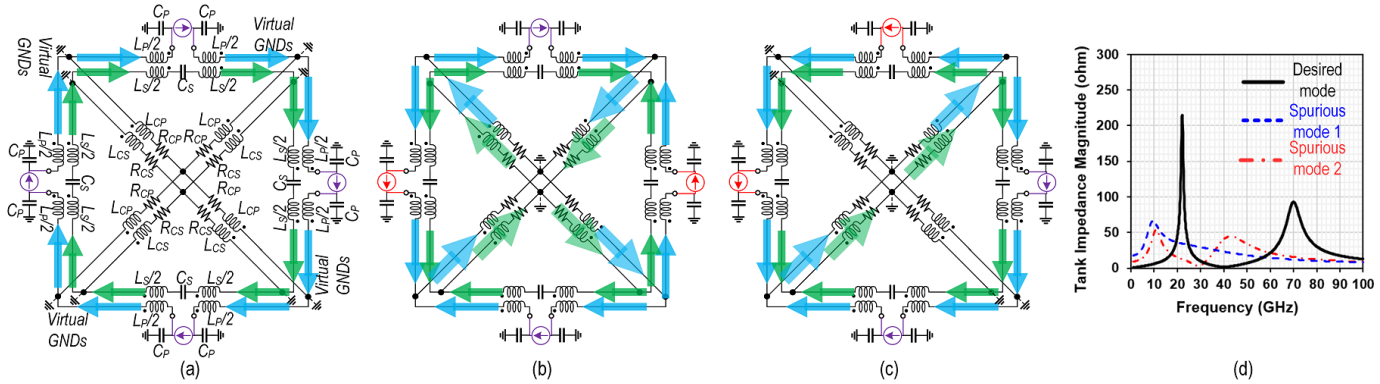

Fig. 3. Introducing cross-coupled metal traces (modeled as L_{CS}, R_{CS}, and magnetic coupling between L_{CP} and L_{CS}) in the transformer secondary loop to suppress mode ambiguity: current flows in (a) the desired oscillation mode, (b) the spurious mode 1, and (c) the spurious mode 2; (d) simulated differential-mode tank impedance magnitude, showing spurious modes with much higher loss (L_P=L_S=80 pH, k=0.78, Q_P=Q_S=15 at 20 GHz, C_P=400 fF, C_S=1 pF, L_{CP}=L_{CS}=100 pH, k_C=0.85, Q_{CP}=3 and Q_{CS}=2 at 20 GHz).

a reduced effective impulse sensitivity function [11]. The tail filtering with a common-mode resonance tuned at the second harmonic improves phase noise by preventing cross-coupled transistors from entering the triode region and by suppressing flicker noise upconversion [12], [14].

Regarding LC VCO cross-coupled transistors, a complementary design is chosen over an NMOS-only one. This is because that an NMOS-only VCO achieves its optimal low phase noise with an output swing approaching $2V_{DD}$, degrading transistor long-term reliability [4].

B. Circular-Geometry Class-F VCO and its Spurious Modes

By splitting the virtual ground nodes at the center of the class-F oscillator transformer and sharing the virtual grounds with the adjacent cores, we arrive at a circular-geometry quad-core class-F VCO as shown in Figs. 1. The circular-geometry design couples multiple oscillators and allows the use of small yet high-Q slab inductors to further lower the phase noise compared to a stand-alone class-F VCO.

Like in a conventional circular-geometry oscillator [4], [13], the splitting of the circular-geometry inductor virtual ground nodes creates the possibility of VCO cores latching at dc. To prevent the dc latching in a circular-geometry oscillator, Aparicio and Hajimiri [13] introduces cross-coupled resistors connecting all the virtual grounds.

The introduction of these dc-latching-prevention resistors creates spurious oscillation modes. Therefore, these resistors need to be designed judiciously such that they are sufficiently lossy to suppress mode ambiguity while not overly resistive causing dc latch [4]. Because of its relatively small resistance, each dc-latching-prevention resistor is implemented as a metal trace which can be modeled as an inductor L_{CP} and a resistor R_{CP} in series.

However, unlike in a conventional circular-geometry VCO, the dc-latching-prevention cross-coupled metal traces alone are no longer enough to avoid mode ambiguity in the circular-geometry class-F oscillator with transformer-based LC tanks.

The circular-geometry transformer-based LC tanks (without cross-coupled transistors and LC tail filters) are shown in Fig. 2 with the dc-latching-prevention cross-coupled metal traces at the transformer primary side (the side connected to cross-coupled transistors and hence prone to dc latching). Three different sets of excitations are used to represent various possible oscillation modes.

In the desired mode [Fig. 2(a)], currents flow clockwise in both the primary and the secondary loops, and the cross-coupled metal traces are invisible as they are shielded by the

virtual grounds created by the oscillation signals.

In the spurious modes [Figs. 2(b)(c)], however, currents are only flowing in the primary loop as the different signal polarities together with the lack of cross-coupled paths create virtual opens in the secondary loop. The absence of transformer lossy secondary loop in the spurious modes boosts the associated tank quality factor as in Fig. 2(d), resulting in mode ambiguity.

C. Suppressing Mode Ambiguity in Class-F Quad-Core VCO

To suppress the aforementioned spurious modes, we introduce cross-coupled metal traces in the transformer secondary loop as in Fig. 3. These traces are modeled as L_{CS}, R_{CS}, and magnetic coupling between L_{CP} and L_{CS}.

In the desired mode as shown in Fig. 3(a), currents still flow clockwise in both the primary and the secondary loops, and neither the cross-coupled metal traces on the primary side nor the newly introduced ones on the secondary side are visible due to the virtual grounds created by the oscillation signals.

In the spurious modes [Figs. 3(b)(c)], with the newly introduced cross-coupled paths, magnetic coupling results in currents in the transformer secondary loop. By making the cross-coupled metal traces thin and narrow, the tank resonance impedance or quality factor in the spurious modes are suppressed and significantly lower compared to those in the desired mode, mitigating the mode ambiguity as in Fig. 3(d).

D. Circular-Geometry Tail Filters Design

Tail filtering is an effective technique to lower phase noise by creating resonance around the second harmonic in the oscillator common-mode path [12]. However, one of the disadvantages of this approach is the added chip area of tail filter inductors. Also, the return paths between the supplies and grounds are parts of the common-mode path but they are difficult to be modeled accurately when supplies and grounds are located far away with each other and when the oscillator operates at beyond 6 GHz high frequencies [15].

In this work, instead of loop inductors, we use slab tail filter inductors (L_T in Fig. 1) which concurrently act as explicit common-mode return paths as shown in Fig. 1. This way, tail inductors come with near-zero added chip area while common-mode return paths are explicitly defined.

III. Implementation

The layout and dimension of the VCO circular-geometry transformer are shown in Fig. 1 and Fig. 4, respectively. The electromagnetic (EM) simulated transformer parameters at each core are L_P=67 pH, L_S=62 pH, k=0.89, Q_P=19, and Q_S=39, both at 20 GHz. The connections between the transformer and the other circuitry, including the cross-coupled transistors, switched-capacitor bank, and varactors, increase overall inductance and lower magnetic coupling and quality factor. The thin and narrow metal traces in the primary and secondary loops have similar inductance compared to transformer inductance ($L_P \approx L_S \approx L_{CP} \approx L_{CS}$, $k \approx k_C$) and are designed to have R_{CP}=5.6 Ω, R_{CS}=25 Ω.

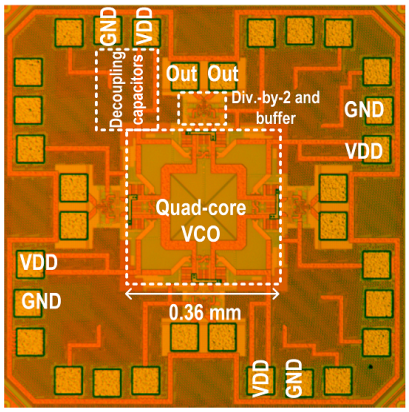

Fig. 4. Die photograph of the quad-core VCO in 65 nm CMOS.

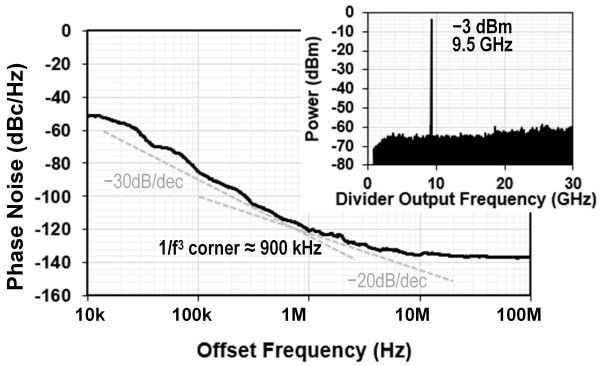

Fig. 5. Measured divider-by-2 output spectrum and phase noise at 9.5 GHz.

Each differential capacitor C_S on the transformer secondary side includes a switched-capacitor bank and a pair of back-to-back varactors. The switched capacitor bank consists of six identical cells. Each unit cell has a on-capacitance of 59 fF and a off-capacitance of 33 fF. The varactor capacitance varies from 45.4 fF to 14 fF when its control voltage changes from 0 to 1 V. Parasitic capacitance from the transformer primary side is used for C_P without any explicit capacitor.

The CMOS cross-coupled pair is designed to ensure that the oscillator has a start-up loop gain of 3. In the layout (see Fig. 1 and Fig. 4), the NMOS and PMOS transistor pairs are arranged in a way that allows one to use thick and wide metal traces to concurrently act as the VCO LC tail filter inductors and the explicit common-mode return paths. The tail inductance L_T is designed to resonance with its parasitic capacitance C_T at around 38 GHz. Due to its relatively low quality factor, the common-mode resonance is sufficiently wideband in our design, and hence does not require dedicated tuning.

IV. Experimental Results

A prototype has been fabricated in a 65 nm CMOS process with one thick top metal. A chip micrograph is shown in Fig. 4 and it occupies a core area of 0.13 mm^2. The chip is packaged and mounted on a Rogers RO4350B printed-circuit board for all measurements. Similar to [2], the VCO is accessed via an on-chip divide-by-2 frequency divider and its output buffer.

Evaluated using a Keysight N9010B EXA signal analyzer, the divider output spectrum and phase noise at 9.5 GHz are plotted in Fig. 5. As can be seen from the output spectrum,

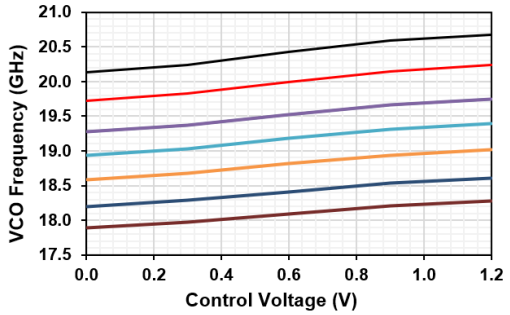

Fig. 6. Measured VCO tuning range (referred from divider-by-2 output).

TABLE I
COMPARISON WITH STATE-OF-THE-ART CMOS OSCILLATORS.

	This work	JSSC 2018 [4]	JSSC 2020 [1]	ISSCC 2019 [2]	CICC 2020 [3]
Topology	Class-F with 2nd-harmonic tail filtering	Class-B with 4th-harmonic tail filtering	Class-C	Multi-resonance tank	Implicit common-mode resonance
Number of Cores	4	4	1	1	2
Frequency (GHz)	19	25	19.5	25.5	27.5
Technology	65 nm	40 nm	28 nm	65 nm	65 nm
TR (%)	16	26	12	16	13
VDD (V)	0.75	0.95	0.9	0.48	0.9
DC power (mW)	16.4	16	20.7	3.8	3.4
PN at 1MHz Offset (dBc/Hz)	−115	−110	−112	−109.3	−105.7
PN at 1MHz Offset referred to 19 GHz (dBc/Hz)	**−115**	**−112.4**	**−112.2**	**−111.9**	**−108.9**
1/f³ Corner Frequency (kHz)	900	500	550	100 to 200	450
FoM (dB)	−188.4	−185.9	−184.6	−191.6	−189.2
Core Area (mm²)	0.13	0.1	0.07	0.08	0.04

TR: Tuning Range PN: Phase Noise

only the desired oscillation mode is sustained. At the divider output, the measured phase noise at 100 kHz and 1 MHz offsets are −86 dBc/Hz and −121 dBc/Hz, respectively. These correspond to VCO phase noise of −81 dBc/Hz and −115 dBc/Hz at 100 kHz and 1 MHz offsets, respectively. At 9.5×2=19 GHz, the VCO draws 21.8 mA from a 0.75 V supply. As depicted in Fig. 6, the VCO operates from 17.9 GHz to 20.7 GHz, corresponding to a 16 % tuning range. The voltage gain varies from 110 MHz/V to nearly 300 MHz/V.

Table I summarizes our measurement results and compares this work with other recent K-band CMOS oscillators. Thanks to the combination of class-F operation and LC tail filtering with a circular geometry quad-core oscillator, we have achieved the lowest phase noise when referred to a 19 GHz carrier while maintaining a competitive FoM, tuning range, and chip area.

V. CONCLUSION

We have demonstrated a ultra-low phase noise CMOS oscillator that fuses class-F operation and tail filtering with a circular-geometry quad-core VCO. The use of class-F operation in a circular-geometry multi-core VCO further lowers phase noise, however, it results in new mode ambiguity. To suppress this new mode ambiguity, we have introduced cross-coupled thin metal traces to the circular-geometry class-F transformer primary and secondary loops. Also, we have extended the circular geometry design to the VCO tail LC filters, resulting in a competitive chip area and well-defined common-mode return paths. Measurements of a proof-of-concept 65 nm CMOS prototype have validated our claims.

ACKNOWLEDGMENT

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