Control and Loss Analysis of a Solid State Transformer Based DC Extreme Fast Charger

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***Abstract*— The increasing demand for electric vehicles, due to advantages such as higher energy efficiency, lower fuel costs, and less vehicle maintenance, is expected to drive the need for electric vehicle charging infrastructure. Due to their reduced size and weight, high power and scalable compact solid state transformers (SST) are growing in popularity. This study presents the total loss analysis and control design for a direct grid connected single-phase SST for a fast charging station. A control strategy to achieve robust current control, DC voltage and power balancing, and power loss minimization (PLM) is implemented for this system. Detailed analyses and simulation results obtained from MATLAB/Simulink are given to prove the effectiveness of the proposed control techniques.**

Keywords—AFE, DAB, ISOP, Power sharing, Power loss, Triple phase shift control.

I. INTRODUCTION

The increasing number of electric vehicles (EV) create a need for more suitable charging infrastructure and an opportunity to develop charging technology to compete against combustion engine vehicles refueling time. The prominent extreme fast-charging (XFC) technology offers a charge time comparable to the time needed to refuel a traditional combustion engine vehicle. The state-of-the-art DC fast-charging stations are connected from the three-phase 480-V low voltage distribution feeder up to 13-kV medium voltage power grid. This connection is usually achieved with the use of a bulky low frequency transformer, which increases the size and cost of the system. To mitigate this bulky low frequency transformer, the power electronics-based SSTs have been introduced to directly interface the medium voltage grid. This configuration provides numerous advantages, including: more control flexibility, lower footprint, better current control, and higher efficiency [1].

To maximize the performance of the SSTs, the efficiency optimization has been a focal point. Numerous analyses have been presented for each major component of the system. In [2], a fundamental duty cycle modulation technique was introduced to decrease the RMS current and improve the efficiency at the wide operating conditions of the dual active bridge (DAB) converter. A digital control method was presented in [3] to decrease the loss of the DAB under light load. A dual control strategy was implemented in [4] for improving the performance of the DAB at both light and heavy loading. A new circuit configuration was proposed in [5] for extending the zero voltage switching (ZVS) range and achieving higher efficiency for the wide operating conditions. However, the size and cost of the converter increased due to the additional half bridge added to the circuit and the maximum efficiency was still under 95%. An optimization and control technique based non-active PLM was introduced in [6] to increase converter efficiency and achieve ZVS. In [7], soft-switching techniques were studied for high power modules of the DAB to minimize converter power loss. A power loss modulation was presented and analyzed in [8], using the dual-phase-shift control strategy in order to increase the overall efficiency of the system. The extended-phase-shift control strategy was implemented in [9] to mitigate the issue of circulating power and improve the efficiency of the converter. Reactive power elimination was formulated in [10] based on the dual-phase-shift method to decrease the peak current, suppress the reactive power component, and reduce the output capacitance of the converter. RMS current minimization-based triple-phase-shift (TPS) control was presented in [11] for an input series output parallel (ISOP) DAB converter to improve the performance and increase system efficiency. In order to complete the loss formulation of the DAB converter, the high frequency transformer losses should be taken into consideration. A loss prediction model for non-sinusoidal signals was introduced in [12] based on Steinmetz variables to formulate the core loss for ferrite core materials.

In grid-connected inverters and active front-end (AFE) circuits, an effective filter is required in order to decrease the ripple of the output current and current harmonics injected from the grid. To this end, an L-filter, which is a first order filter, was introduced. Although the filter is simple, it had a few disadvantages, including poor harmonic attenuation and dynamic performance, high voltage drops across the inductor, and bulkiness [13]. The higher-order filters, such as LCL, LCL-LC, LLCL, and trap-filter, present excellent performance with compact size. Due to its simplicity and high performance, the LCL filter has attracted high attention in both academia and industry. The power quality indices dictate the component size of the LCL filter. The inverter side and grid side inductors and the capacitor size are determined based on the desired output current ripple, the attenuation capability at high frequencies, and the maximum generated reactive power at fundamental frequency [14]. When designing the LCL filter, resonance poses a challenge, as it can harm the system. Either passive and active damping methods, which are based on using resistor/resistors, or a control method can attenuate this issue and increase system robustness and stability [15]. The design process is iterative and requires consideration of the resonant frequency, the voltage drop, the maximum output current ripple, minimization of the total harmonics distortion (THD) and the damping method [16]-[18]. Among the methods proposed, [17] was chosen for the LCL filter design, as it offers a systematic design methodology that meets industrial requirements and limits THD to a specific value.

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Designing the cascaded H-bridge multilevel (CHBML) AFE converter to maximize the efficiency of the SST is dependent upon the control algorithm applied. A loss analysis was presented in [19] for a CHBML inverter to study its benefit in large scale PV systems. In [20], a loss comparison analysis was studied to present a methodology for selecting the number of cells that can be used in a cascaded H-bridge.

In this study, a power stage which is compose of a CHBML AFE and an ISOP DAB DC-DC converter is proposed for extreme fast charging stations. While advanced control schemes are proposed for power converter stages, the total loss of the system is minimized. The loss analysis was performed, and the loss was broken down into three main sections: the LCL filter losses, the AFE losses, and the DAB converter losses. In addition, an optimization study was performed to minimize the DAB converter losses. The performance of the system was validated with analytical results and MATLAB/Simulink simulation results.

II. DC Fast Charger Converter Modeling

Fig. 1 shows a single-phase SST. Its configuration consists of a CHBML-AFE converter and a modular ISOP DAB DC–DC converter with high-frequency transformers. The system is connected to the utility grid through the LCL filter. The CHBML-AFE and the LCL filter provide interconnection between the utility grid and the regulated DC link. Input AC current and DC link regulation are designed to maintain high power quality and low THD. The isolated ISOP DC-DC converter interfaces the battery energy storage unit or the electrical vehicles, and provides compact, integrated and galvanic isolated nodes for the loads. In order to guarantee optimum system operation, the governing equations of the SST are formulated to implement the control and perform the loss analyses. Equations (1)-(5) model the CHBML-AFE with LCL filter, and equations (6)-(7) describe the average power transfer and the RMS current of the ISOP DAB with TPS method.

$$L_g \frac{di_2}{dt} + r_g i_g = v_g - v_{c_f} \tag{1}$$

$$L_i \frac{di_1}{dt} + r_i i_i = v_{c_f} - (V_{H_1} + V_{H_2} + V_{H_3}) \tag{2}$$

$$C_f \frac{dv_{c_f}}{dt} = i_c = i_g - i_i \tag{3}$$

$$\begin{cases} V_{H_1} = uV_{o_1} \\ V_{H_2} = uV_{o_2} \\ V_{H_3} = uV_{o_3} \end{cases} \tag{4}$$

$$V_{0_1} = V_{0_2} = V_{0_3} = V_d \tag{5}$$

$$P_{ave} = \frac{N_{cell} V_1 V_2 \left(-D_1^2 + D_1 D_2 + D_1 \Phi - D_1 - D_2^2 + D_2 - \Phi^2 + \Phi\right)}{(4Lf_s)} \tag{6}$$

$$I_{rms} = \frac{N_{cell}\sqrt{3}}{3} \frac{\left(\begin{matrix} 4V_1V_2\left(\begin{matrix} 3D_1\left(D_1D_2 + D_1\Phi - D_1 - D_2^2 + D_2 + \Phi - \Phi^2\right) \\ +3(D_2^3 - D_2^2 - \Phi^2) + 2(\Phi^3 - D_1^3) + 1 \end{matrix}\right) \\ +2V_1^2(3D_1^2 - 2D_1^3 - 1) \\ +2V_2^2\left(2(D_2^3 - \Phi^3) - 6(D_2^2\Phi + D_2\Phi^2 - D_2\Phi) + 3(\Phi^2 + D_2^2) - 1\right) \end{matrix} \right)^{\frac{1}{2}}}{4Lf_s} \tag{7}$$

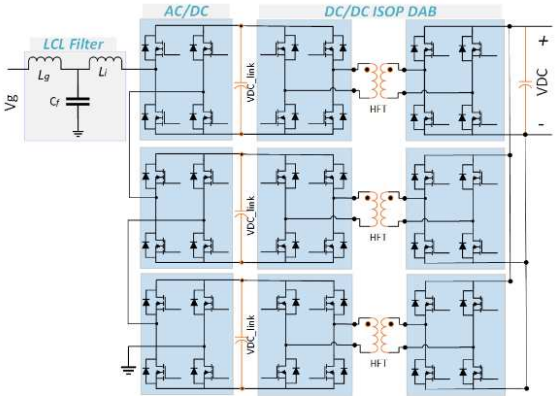


Fig. 1 The single-phase SST

I. DC Fast Charger Converter Loss Analysis

In order to ensure the highest efficiency of the system, even under light load conditions, the total power loss for the major passive and active components is analyzed for the LCL filter, CHBML-AFE and the ISOP DAB. Analytical expressions of the DAB converter under TPS control for PLM in different operating zones are formulated. The particle swam optimization (PSO) and the Lagrange Multiplier (LM) were used in order to obtain either the numeric value or a closed form expression for the optimal duty cycles that enable the DAB converter to operate with minimized power loss for each power zone.

A. AFE Converter Loss Analysis

The CHBML-AFE power losses are formulated based on the conduction and switching losses. Conduction losses in power MOSFET can be formulated using the MOSFET-approximated drain-source on-state resistance. The conduction loss of the anti-parallel diode is also formulated to obtain the total conduction losses. R_{DS} is the on-state resistance and V_{do} is the diode voltage drop. Taking into consideration the inverter side inductance current oscillation and the switching operation mode, the conduction and switching power losses are obtained, as in (8) and (9) [21] and [22].

$$P_{con-AFE} = 2N_{cell}(R_{DS} I_{rms}^2 + V_{do} i_{ave}) \tag{8}$$

$$P_{sw-AFE} = N_{cell} f_s \left(2E_{ON}\left(\left|i_{ave} - \frac{\Delta i_b}{2}\right|, V_d\right) + 2E_{OFF}\left(\left|i_{ave} + \frac{\Delta i_b}{2}\right|, V_d\right) + 2Q_{rr}\left(\left|i_{ave} - \frac{\Delta i_b}{2}\right|, V_d\right).V_d.f_{sw}\right) \tag{9}$$

E_{on}, E_{OFF}, Q_{rr}, V_d, f_{sw}, and N_{cell} are the turn-on and turn-off energy of the selected semiconductor, the reverse recovery charge of the diode, the capacitor voltage of each cell, the switching frequency, and the number of cells, respectively. Δi_b can be calculated as follows:

$$\Delta i_b(u) = \frac{uV_{dc}}{N_{cell} L_b}\left(\frac{1}{N_{cells}} - u\right) \tag{10}$$

where L_b is the summation of the grid side and inverter inductances. The maximum current ripple can be found at $u=0.5/N_{cell}$ as:

$$\Delta i_{b,max} = \frac{V_{dc}}{4{N_{cell}}^2 L_b f_{sw}} \tag{11}$$

u is the modulation index. The complete derivation can be found in [23]. Δu_i is the correction from the voltage balancing.

$$u = \frac{1}{N_{cell}V_d}\left(\frac{L_i di_i^*}{dt} + r_i i_i^* + V_{cf}^*\right) + K_\alpha V_d x_1 - K_\beta x_3 + \Delta u_i \quad (12)$$

B. LCL Filter Loss Analysis

The filter power losses are formulated based on the copper and core losses of the inductors, and the ESR loss of the capacitor. (13) defines the copper loss:

$$P_{cu-filter} = R_{cu-LCL}.I_{rms}^2 \quad (13)$$

where $R_{cu\text{-}LCL}$ is the summation of the grid side and inverter winding resistances. The filter core loss of each inductor of the LCL filter is calculated based on the Steinmetz Equation as:

$$P_{core-filter} = K_c.f_{sw}{}^x.\left(\frac{L\Delta i_{pp}}{2N_L A_e}\right)^y.V_e \quad (14)$$

where K_c, x, and y are the parameters of the chosen magnetic material. L, A_e, and V_e are the inductance, the effective cross-section of the air, and the volume of the magnetic core, respectively. N_L is the number of inductor turns. The ESR loss is formulated in (15). ic is derived from (3).

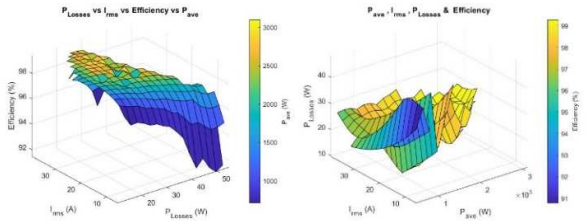
$$P_{ESR} = R_{esr}i_c^2 \quad (15)$$

The total loss of the AC-DC power stage can be computed as the summation of the CHBML-AFE losses and the filter losses, as formulated in (16).

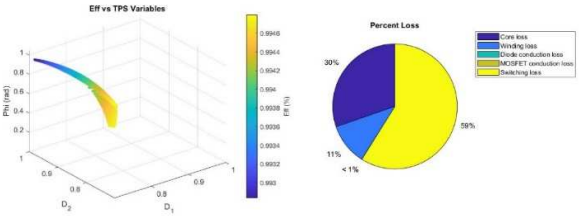
$$P_{loss_{AC-DC}} = P_{con-AFE} + P_{sw-AFE} + P_{cu-filter} + P_{core-filter} + P_{ESR} \quad (16)$$

C. DAB Converter Loss Analysis

To formulate the total power loss of the DAB using the TPS control modulation scheme, three operating zones are defined as zone 1 ($0 \le D_2 \le D_3 \le D_1 \le 1$), zone 2 ($0 \le D_2 \le D_1 \le D_3 \le 1$), and zone 3 ($0 \le D_1 \le D_2 \le D_3 \le 1$), which correspond to low, medium and high power regions, respectively [24]. The DAB converter total loss expression is formulated in terms of the losses of the semiconductor devices (conduction and switching losses) and the high frequency transformer losses (winding and core losses). There are two operational modes in which the DAB can operate: hard-switching and soft-switching. Establishment of the ZVS constraint occurs when the zero crossing of i_l is within the time interval where V_1 and V_2 have opposite polarities. Under soft-switching operation, turn-off losses are calculated. Under hard-switching operation, both turn-off and turn-on losses are calculated. The four considered loss equations for zone 3 for the DAB converter are formulated in (16)-(19); for the other zones of operation refer to [24].



(a) (b)



(c) (d)

Fig. 2 Optimization trajectory and theoretical results. (a)-(b) loss and efficiency for any given average power, (c) optimal control variables, (d) loss breakdown in the DAB.

$$P_{sw} = N_{cells}\frac{\begin{matrix}V_1 t_f|V_1 - V_2 + \Phi V_2 + D_1V_1 - 2D_2V_1 - D_2V_2| \\ + V_2 t_f|V_1 - V_2 + \Phi V_2 - D_1V_1 + D_2V_2|\end{matrix}}{8L} \quad (17)$$

$$P_{cond} = N_{cell}\frac{\begin{matrix}12V_f L f_s\begin{pmatrix}|(\Phi-1)(V_1(\Phi-D_1)+D_2V_2)| \\ +D_1|-V_1(D_2+D_1)+V_2(2\Phi+D_2-2D_1-2)| \\ +D_2|(V_2(D_1-D_2)+V_1(D_1-\Phi)| \\ +\Phi|(V_2(1+D_2-\Phi)+V_1(\Phi-D_1+D_2-1))|\end{pmatrix} \\ +R_{ds}V_1^2(2D_1^3-3D_1^2+1)+R_{ds}V_2^2(2(D_2-\Phi)^3-3(D_2+\Phi)^2+1) \\ +2R_{ds}V_1V_2\left(2(D_1^3-D_2^3-\Phi^3)+3D_1(D_2^2-D_1D_2+\Phi^2-D_1\Phi)+3(D_1-D_2)^2\right. \\ \left.+3\Phi(\Phi-D_1)-1\right)\end{matrix}}{24L^2f_s^3} \quad (18)$$

$$P_{core} = N_{cell}K_i(2B_m)^{\theta-\Upsilon}\left(\begin{pmatrix}\frac{T_s}{2} \\ -\frac{\Phi T_s}{2}\end{pmatrix}(B_m f_s)^\Upsilon\begin{pmatrix}2^\Upsilon \\ +4^\Upsilon\end{pmatrix}+\begin{pmatrix}\frac{D_2T_s}{2} \\ -\frac{D_1T_s}{2}\end{pmatrix}\left(\begin{pmatrix}\left(\frac{2B_m}{\frac{D_2T_s}{2}+\frac{T_s}{2}}\right)^\Upsilon \\ +\left(\frac{4B_m f_s}{D_2}\right)^\Upsilon\end{pmatrix}+\begin{pmatrix}\frac{\Phi T_s}{2} \\ -\frac{D_2T_s}{2}\end{pmatrix}\begin{pmatrix}\Upsilon \\ +\left(\frac{4B_m f_s}{\Phi}\right)^\Upsilon\end{pmatrix}\right)\right) \quad (19)$$

$$P_{winding} = N_{cell}R_{ac}I_{rms}^2 \quad (20)$$

D. DAB Optimization Trajectories

To achieve the highest efficiency for the DAB converter, the objective function for the optimization process is formulated, as in (21), where the total loss is the sum of the four loss components, as defined in (17)–(20), for any given average power. Two optimization methods are defined to optimize the efficiency of the DAB. The LM is used to obtain the closed form expressions, as formulated in (22) and (23), and the off line PSO is used to obtain a look-up table (LUT) for the optimal control variables that optimize the efficiency. The optimal trajectories for the TPS variables, D_1, D_2, and φ, are shown in Fig. 2(c). Fig. 2(a) and (b) show the trend in loss and efficiency based on the average power transfer for the DAB converter. Fig. 2(d) demonstrates the percentage of loss that occurs for each component of the converter, where the switching loss constitutes the major source of loss in the system.

$$\eta_{DAB} = \frac{P_{ave}}{P_{ave}+P_{loss}} \quad (21)$$

$$D_1 = 2\Phi + \frac{24D_2 - 24D_2{}^2 + 4K\left(6D_2{}^2 - 6D_2 + 1\right) - 4}{2\sqrt{\begin{matrix}K^2\left(6D_2 - 6D_2{}^2 - 1\right) \\ +2K\left(6D_2{}^2 - 6D_2 + 1\right) - 8D_2 + 4 \\ +8D_2(1-D_2)\end{matrix}}} - 1 \quad (22)$$

$$D_2 = \frac{2D_1(4+K^2-6K)+\Phi(6K-K^2-4)+(2K-2)^2 \pm \sqrt{2}K\sqrt{\begin{matrix}K^2(-3(2D_1-\Phi)^2-6D_1+3\Phi+1)\\+K[12D_1-6\Phi-1+6(2D_1-\Phi)^2]\\+8D_1(2\Phi-2D_1-1)+4\Phi(1-\Phi)\end{matrix}}}{5(7K^2-10K+4)} \quad (23)$$

II. Control Structure

The proposed control scheme for the CHBML-AFE contains three main parts: the generation of the grid current reference, the modified Lyapunov Function (LF)-based control method, and the output bus voltage balancing control. The grid reference current is obtained by summing the output voltages and dividing that result by the number of DC buses present in the CHBML-AFE to obtain the average DC voltage value. This average voltage is taken as the reference value and is regulated by the PI controller. By multiplying the output of the PI controller and the unit sine wave, which is synchronized with the grid voltage and frequency and generated by the PLL unit, the reference signal for the grid current is generated. This reference current is then fed to the proportional resonant (PR) controller block to produce the final reference for the modified LF control block. A conventional LF-based controller is modified with additional capacitor voltage feedback. Details on the controller design can be found in [23]. In addition to the LF- based control with an additional capacitor voltage loop and PR controller, a voltage balance controller is also applied to balance the cell voltages of the CHBML-AFE. The goal of this voltage balance controller is to remove possible unbalanced voltage conditions for situations where mismatched parameters occur or different loads are applied to the cells of CHBML-AFE. A PI controller regulates the output DC voltage of each cell. The PI output is multiplied by the reference sine wave (the output of the PLL) to generate the perturbed duty cycles. These are added to the switching control, which is generated by the modified LF block [23].

The optimal closed loop control for the ISOP DAB converter is shown in Fig. 4. This figure depicts both the buck and boost operation modes of the ISOP DAB converter. The voltage PI controller generates the initial phase-shift φ_i. In order to estimate the average power transferred from the primary to the secondary bridge, φ_i is applied in the optimal control variable generation block. The operating zone is then determined according to the estimated average power. The optimal D_{1opt} and D_{2opt} are calculated either from (21) and (22) or are chosen from the PSO LUT for the other operating zones [24].

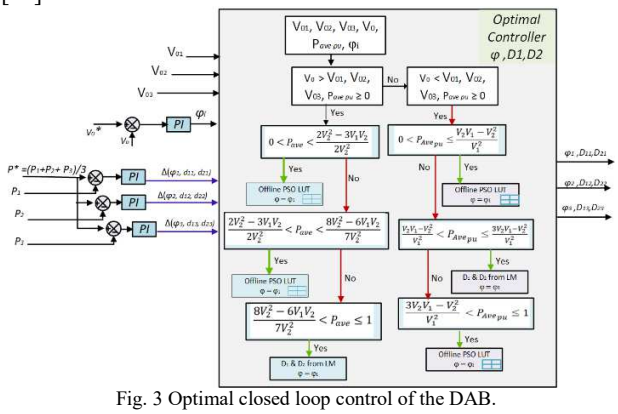


Fig. 3 Optimal closed loop control of the DAB.

III. Simulation Results

In this study, a single-phase three-cell SST was simulated in MATLAB/Simulink to validate the proposed control schemes. Table I contains the parameters of the system. The design of the proposed configuration utilizes 277V grid voltage and generates 170V DC bus voltage per module to establish the DC-link for the ISOP DAB converter, which in turn generates 400V output. To validate the proposed strategy, different power loadings are introduced.

TABLE I
System Parameters

Symbol	Value
Grid voltage amplitude, V_g	277V RMS
Inverter side inductance, L_1	0.8mH
Filter capacitance, C	10μF
Grid side inductance, L_2	0.5mH
Inductor resistors, r_1 and r_2	0.08Ω, 0.05Ω
DC link voltage, V_{dc}	170V
Grid frequency, f_g	60Hz
AFE switching frequency, f_{sw}	10kHz
DAB output voltage (V)	400
DAB frequency (kHz)	50
Power modules	CCS050M12CM2

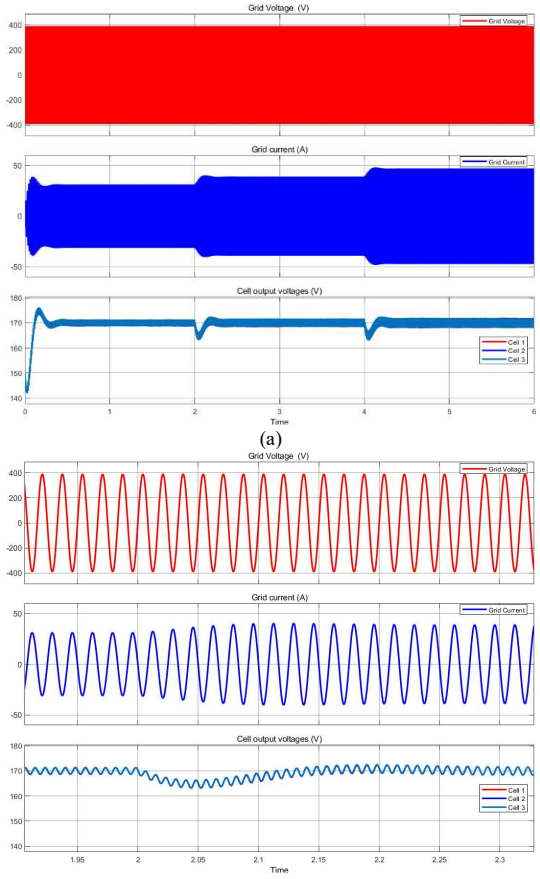


Fig. 4 The grid voltage and current, and the three DC bus voltages. (a) zoomed out version (b) zoomed in version.

At t=2s and t=4s, a step load was introduced to test the performance of the CHBML-AFE. It can be seen that the DC output voltages are maintained at the desired level. The converter has a fast response during transient time with limited

undershoot and maintains sinusoidal currents, which is in phase with grid voltage even during the transient time. Fig. 4(a) shows the grid voltage and current and the three DC bus voltages. Fig. 4(b) shows a zoomed in version of (a) during the transient time of 2s. The THD is 1.60% for the lowest power operation (0-2s), as seen in Fig. 5, and is 0.8% for the other two power levels.

Fig. 6 – Fig. 8 show the performance of a single DAB converter in the ISOP system. The TPS control can be seen in the shape of the primary and secondary voltages of the high frequency transformer from Fig. 6 for the highest power region. This figure also shows the tracking accuracy of the DAB converter output voltage. In order to validate the efficiency technique for the DAB converter, the single-phase shift (SPS) method is compared to the TPS method. Fig. 7 and Fig. 8 show these two cases. In Fig. 7, the TPS method is used; Fig. 8 shows the performance of the DAB under the SPS method. For the same power level and voltage rating, it can be seen that the applied control strategy provides higher efficiency, as expected, from the analytical results from Fig. 2(a) and (b).

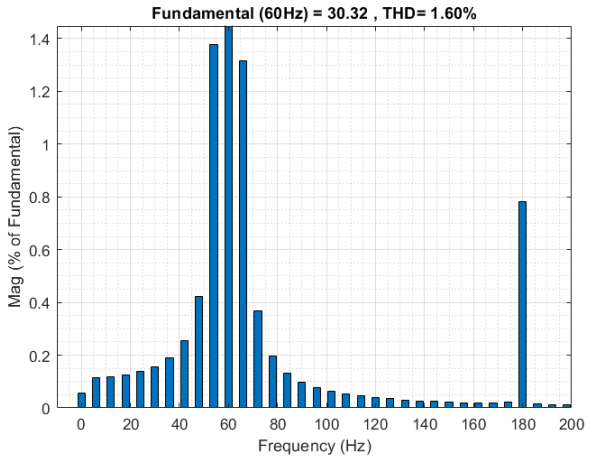


Fig. 5 The grid current THD spectrum.

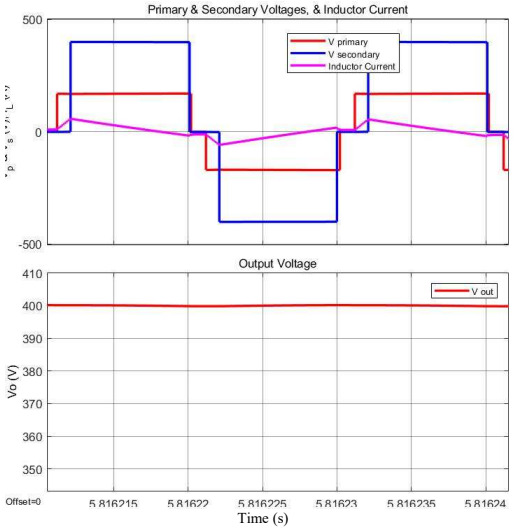


Fig. 6 Primary and secondary voltages of the transformer, leakage current and output voltage of the DAB.

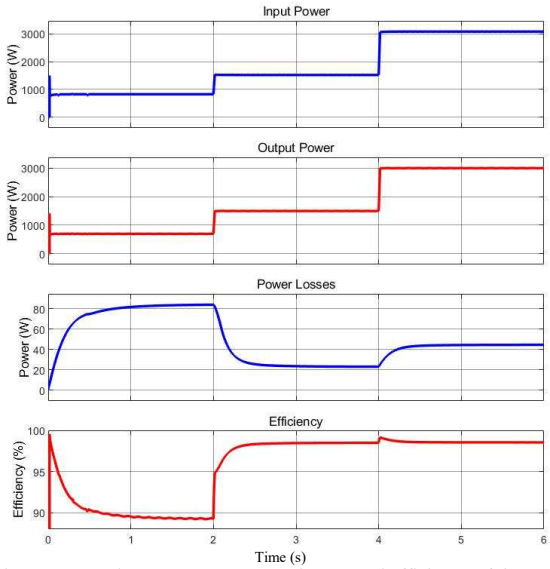


Fig. 7 Input and output power, power losses, and efficiency of the DAB under TPS control.

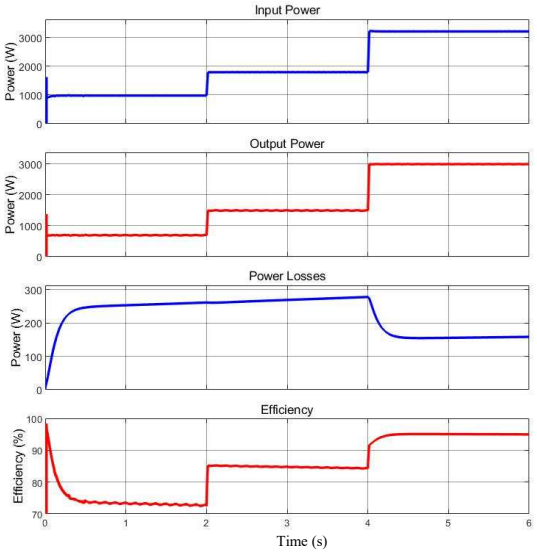
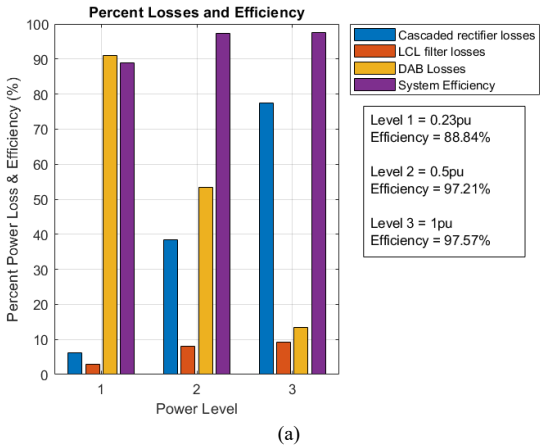
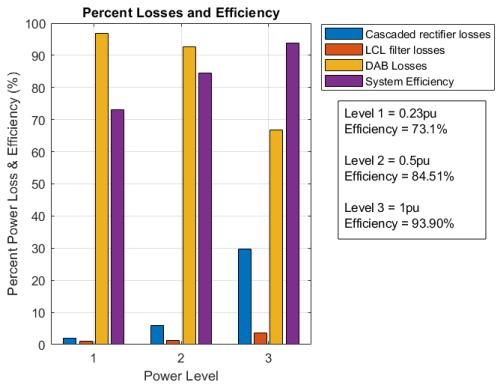


Fig. 8 Input and output power, power losses, and efficiency of the DAB under SPS control.



(a)



(b)

Fig. 9 Loss breakdown of the system (a) optimized system (b) non-optimized system.

IV. Conclusion

This paper has presented a control scheme and loss analysis for an extreme fast charger converter. The modified LF-based controller is applied for the CHBML-AFE. The TPS technique is employed in the ISOP DAB DC-DC converter. An optimization method is applied using the TPS modulation strategy in order to minimize the total power loss of the ISOP DAB. The employed control method provides low THD, even at low power, and keeps the grid current sinusoidal and in phase with the grid voltage. The efficiency of the system is greatly improved compared to the SPS method, especially at low loads. The loss breakdown of the system is also presented.

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