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# A Control Scheme for a DC Extreme Fast Charger with RMS Current Minimization

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***Abstract*—In this study, a power converter topology and control schemes for the power converter stages are proposed for a DC extreme fast charger. The proposed system is composed of a cascaded H-bridge (CHB) converter as the active front end (AFE), and an input series output parallel (ISOP), which includes three parallel connected dual active bridge (DAB) cells. A modified Lyapunov Function (LF) based control strategy is applied to obtain high current control response for the AFE. An additional controller to remove the voltage unbalances among the H-bridges is also presented. Additionally, the triple phase-shift (TPS) control method is applied for the ISOP DAB converter. A Lagrange Multiplier (LM) based optimization study is performed to minimize the RMS current of the transformer. The performance of the proposed converter topology and control strategies is validated with MATLAB/Simulink simulations.**

***Keywords—Lyapunov Function, current control, ISOP, triple phase-shift, dual active bridge, current minimization, Lagrange Multiplier***

## I. INTRODUCTION

The recent research, development, and commercialization of electric vehicles (EV) is an important step toward the goal of creating sustainable, smart cities with little to no pollution. New standards for EV manufactures will require them to overcome many challenges, including the development of a high performance battery and a suitable EV charger, while keeping vehicle costs to a minimum.

An EV charger can be in the form of an on-board charger or an off-board charger. On board chargers are mainly used as home chargers and only provide charging power under 100kW [2]. The main disadvantage of these EV chargers is their long charging time. The off-board chargers, which are typically DC system based, overcome this obstacle and have the capability to fully charge an EV battery in less than 30 minutes. However, in order to have a practical ultra-fast EV charger located in a rural area, a strong grid is required. Typically, the ultra-fast EV charger is composed of a filter, an AC-DC rectification, a power factor correction (PFC), and a DC-DC converter, into which PFC may be integrated.

Recently, AC-DC converters with bidirectional power flow capability have been attractive in both industry and academia. Three-phase voltage source converters (VSC) and multilevel neutral point clamped (NPC) converters with LCL filter based AFE converter topologies are one of the widely used candidates that can operate with high power factor in bidirectional power flow manner. The EV charger must isolate the battery and the power grid to prevent any ground fault impact on either side. In order to achieve galvanic isolation between the grid and the EV battery, the system can be configured as the following: a line frequency transformer, an AC-DC rectification stage, and a non-isolated DC-DC converter, which can be a buck converter, a boost converter or an interleaved converter design. Using a high-frequency transformer embedded into the isolated DC-DC converter stage is another option. Phase-shifted full bridge (PSFB) converters and resonant converters, such as series resonant converters and LLC resonant converters, are the most common topologies used for unidirectional isolated DC-DC converter stages. For bidirectional isolated DC-DC converter topologies, DAB converters and bidirectional resonant converters are the most commonly used. For higher power application, DAB and resonant topologies can be connected in series and parallel [1].

The main purpose of the AC-DC rectification stage with the PFC is to regulate the DC voltage and provide high power factor. The control scheme includes a voltage outer loop and a current inner loop. A three-phase VSC based rectifier is widely used in industry due to its bidirectional power flow, low voltage distortion, near unity power factor, and DC voltage control capabilities [3]. However, this method needs two line-voltage sensors, two phase-current sensors and a DC-link voltage sensor. Therefore, the total cost is high. Sensorless control methods, such as direct power control and model predictive control (MPC), have been proposed to decrease the cost and increase the robustness to disturbances [4]–[7]. Although active and passive methods can be used for PFC, the passive methods have a larger size, volume and weight, and a limited PFC performance, especially for variable load conditions [8]. Conversely, active PFC methods can control DC voltage and offer a high power factor over a wide operating range. For the unidirectional power flow, a diode rectifier is connected to a boost, buck or buck-boost converter. The main disadvantage of these PFCs is high power loss. The bridgeless PFC can address this issue by reducing the number of semiconductor components in the line current path [9]. However, the bridgeless PFC has higher common mode noise.

For a high/medium voltage AC to low voltage DC system, the cascaded multilevel converter is widely used. One of the main challenges in this topology is to balance the floating capacitor (output) voltage for stable operation of the whole system. Several methods, including self-balancing control [10], zero/negative sequence voltage injection [11], selective harmonic elimination by PWM [12], selective harmonic elimination by MPC [13], and space voltage vector adjustment [14], have been presented to address this issue. Although each method has advantages and disadvantages, different considerations, such as complexity, dynamic performance,

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effect on switching frequency, applicability, and computation burden, must be taken into account when selecting or proposing a new method.

The DC-DC converter control is made of a double closed loop to control battery voltage and current to provide appropriate charging characteristics. Different control methods, including PI control, fuzzy logic control, sliding mode control, and MPC, can be applied to regulate the DC-DC converter stage. Controllers can be evaluated and selected based on simplicity, transient and steady-state performance, robustness, and ease of implementation [15].

The basic control method for the DAB converter is the single-phase-shift (SPS) control, where both primary and secondary duty cycle are equal to 0.5 and the phase-shift is adjusted to control the power flow direction and magnitude. SPS is simple and provides fast dynamic response. However, zero voltage switching (ZVS) does not exist under light load conditions. When there is a voltage mismatch, circulating power occurs and the RMS current increases. These lead to high power loss and low efficiency. The dual-phase-shift (DPS) control addresses some of these issues by adding an inner phase-shift as an additional control parameter. In [16], one optimization problem is solved by providing soft-switching in the full operating range to reduce switching frequency. In [17], optimized parameters of the DPS method are obtained to reduce reactive power and current stress in the DAB converter. However, this method cannot completely minimize the current stress. The universal phase-shift control method is proposed to address the current stress issue [18]. Generally, the DPS method has suboptimal operation modes [15]. In order to provide ZVS under light load, a TPS, including inner primary phase-shift, inner secondary phase-shift, and outer phase-shift, has been proposed [19]. TPS has a higher degree of freedom for the DAB converter to reach multiple different objectives, such as minimum current stress [20], minimum RMS inductor current [21], minimum circulation power [22], and ZVS over a wide operating range [23]. However, finding the optimal modulation is a complex task and requires effective optimization tools to determine the global optimum value.

In this study, a power converter topology is presented for DC extreme fast EV charging systems. The proposed system is composed of an AC-DC rectifier and a DC-DC converter. To provide galvanic isolation without increasing the size and cost or decreasing the efficiency, the isolated DAB converter is used for the DC-DC converter stage. The CHB is used for the AFE stage to enable direct connection to the medium voltage grid. A modified LF based control strategy is applied to obtain high reference current tracking performance in both transient and steady state, and obtain unity power factor. Additionally, a DC voltage balance controller is used to remove the voltage unbalances resulting from non-equal load conditions. The TPS is applied to control the DAB converter. Since different values of the three control variables can provide the same operation condition, the control variables are determined to minimize the transformer current by using the LM optimization method. Thus, the circulation current related losses are reduced and efficiency is improved. The power balance control scheme is also employed to remove any power unbalances between the parallel

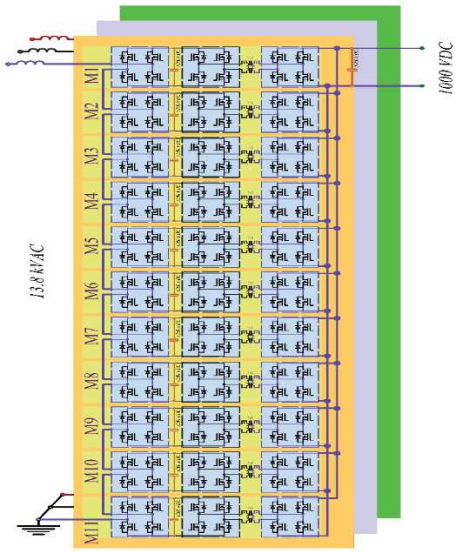



Fig. 1. The SST converter architecture.

connected DAB cells. The simulation results show that the proposed control schemes can achieve the design objectives. The AFE draws sinusoidal currents in phase with the grid voltage phase and frequency. The current THD is obtained as 3.05% and 0.85% for low and rated power conditions, respectively. The TPS control method with the proposed optimization scheme also provides significant reduction in the transformer current, especially at low load and medium power level. The DC voltage and power unbalances are also eliminated.

## II. DC Fast Charger Converter Modeling

Fig. 1 shows the configuration of the proposed three-phase fast charging system design based on the solid state transformer (SST) concept. The topology consists of a cascaded multi-level AFE rectifier and a modular ISOP DAB DC–DC converter with high-frequency transformers. A scaled down version of this system is considered for analysis and verification. The scaled down converter is connected to the utility grid through an LCL filter. The LCL filter is used to provide filtering and to reduce the THD. The AFE establishes the DC link interface for the ISOP DAB converter. The input AC current and DC link voltage controllers are designed to maintain high power quality and low THD performance. The isolated ISOP DAB DC-DC converter establishes the output DC bus for the battery based energy storage unit or EVs and provides compact, integrated and galvanic isolated connections for the loads. To study the optimum performance of the system, the governing equations of the scaled down single phase SST are obtained to implement the control and analyze both the AC current and the RMS current of the DAB. Equations (1)-(5) model the AFE with LCL filter and equations (6)-(16) describe the average power transfer and the RMS current of the ISOP DAB under TPS method for different feasible operating regions. Detailed derivations for these equations can be found in [24] - [26].

$$L_g \frac{di_2}{dt} + r_g i_2 = v_g - v_{c_f} \quad (1)$$

$$L_i \frac{di_1}{dt} + r_i i_1 = v_{c_f} - (V_{H_1} + V_{H_2} + V_{H_3}) \quad (2)$$

$$C_f \frac{dv_{c_f}}{dt} = i_c = i_2 - i_1 \tag{3}$$

$$\begin{cases} V_{H_1} = uV_{o_1} \\ V_{H_2} = uV_{o_2} \\ V_{H_3} = uV_{o_3} \end{cases} \tag{4}$$

$$V_{0_1} = V_{0_2} = V_{0_3} = V_d \tag{5}$$

$$P_{aveFront} = N_{cell} \frac{V_1 V_2}{8LF} 2D_1 D_2 \tag{6}$$

$$P_{aveRight} = N_{cell} \frac{V_1 V_2}{8LF} 2D_2 \varphi \tag{7}$$

$$P_{aveLeft} = N_{cell} \frac{V_1 V_2}{8LF} 2D_1 \varphi \tag{8}$$

$$P_{aveMiddle} = N_{cell} \frac{V_1 V_2}{8LF} \begin{pmatrix} -\frac{1}{2}(D_1 - D_2)^2 \\ +\varphi(D_1 + D_2 - \frac{1}{2}\varphi) \end{pmatrix} \tag{9}$$

$$P_{aveRear} = N_{cell} \frac{V_1 V_2}{8LF} \begin{pmatrix} -(D_1^2 + D_2^2) - 2 \\ +2(D_1 + D_2) + \varphi(2 - \varphi) \end{pmatrix} \tag{10}$$

$$I_{com} = \frac{V_1}{V_2}\left(\frac{3}{2}D_1^2 - D_1^3\right) + \frac{V_2}{V_1}\left(\frac{3}{2}D_2^2 - D_2^3\right) \tag{11}$$

$$I_{rmsFront} = N_{cell} \frac{\sqrt{V_1 V_2}}{2\sqrt{2}\,LF}\left(I_{com} + 3D_1 D_2(\varphi - 1)\right)^{\frac{1}{2}} \tag{12}$$

$$I_{rmsRight} = N_{cell} \frac{\sqrt{V_1 V_2}}{2\sqrt{2}\,LF} \begin{pmatrix} I_{com} + \frac{1}{2}D_2^3 + \frac{3}{2}D_1^2 D_2 \\ +\frac{3}{2}D_2\varphi^2 - 3D_1 D_2 \end{pmatrix}^{\frac{1}{2}} \tag{13}$$

$$I_{rmsLeft} = N_{cell} \frac{\sqrt{V_1 V_2}}{2\sqrt{2}\,LF} \begin{pmatrix} I_{com} + \frac{1}{2}D_1^3 + \frac{3}{2}D_1 D_2^2 \\ +\frac{3}{2}D_1\varphi^2 - 3D_1 D_2 \end{pmatrix}^{\frac{1}{2}} \tag{14}$$

$$I_{rmsMiddle} = N_{cell} \frac{\sqrt{V_1 V_2}}{2\sqrt{2}\,LF} \begin{pmatrix} I_{com} + \frac{1}{4}(D_1^3 + D_2^3) + \frac{3}{4}D_1 D_2(D_1 + D_2) \\ -3D_1 D_2 + \frac{3}{2}D_1 D_2\varphi - \frac{3}{4}(D_1^2 + D_2^2)\varphi \\ +\frac{3}{4}(D_1 + D_2)\varphi^2 - \frac{1}{4}\varphi^3 \end{pmatrix}^{\frac{1}{2}} \tag{15}$$

$$I_{rmsRear} = N_{cell} \frac{\sqrt{V_1 V_2}}{2\sqrt{2}\,LF} \begin{pmatrix} I_{com} + \frac{3}{2}(D_1^2 + D_2^2) \\ -3(D_1 + D_2) + 3(D_1 + D_2)\varphi \\ -\frac{3}{2}(D_1^2 + D_2^2)\varphi - 3\varphi\frac{3}{2}\varphi^2 - \frac{1}{2}\varphi^3 + 2 \end{pmatrix}^{\frac{1}{2}} \tag{16}$$

## III. Derivation and Analysis Of the DC Fast Charger Control

Two control methods have been implemented for the proposed system to achieve the optimum operation. The modified LF based control strategy was utilized for the AFE stage to achieve a robust current control performance [24]. To decrease the loss and heat generated by the circulating current of the DAB converter, an RMS current minimization based TPS scheme was studied and implemented for the DC-DC converter stage [25].

### *A. AFE Converter Control*

When the energy supplied by the power source is equivalent to the total energy consumed by the load and the active rectifier components, Lyapunov's control technique requires that the state variables $(x_1, x_2, x_3)$ (given in Eq. 17) at the equilibrium point be zero. According to this stipulation, an energy function $(V(x))$ can be formulated to analyze the stability of the system, as in (18).

$$\begin{cases} x_1 = i_1 - i_1^* = 0 \\ x_2 = i_2 - i_2^* = 0 \\ x_3 = V_{cf} - V_{cf}^* = 0 \end{cases} \tag{17}$$

$$V(x) = \frac{1}{2}(L_1 x_1^2 + L_2 x_2^2 + C x_3^2) \tag{18}$$

The global asymptotically stable equilibrium point is achieved when $V(0) = 0, V(x) > 0, V(x) \to \infty \; and \; \dot{V}(x) < 0$. The time derivative of (18) must be obtained, as in (19), in order to test the last condition and the global stability of the inverter about its equilibrium point if the perturbed control input is chosen, as in (20).

$$\dot{V}(x) = x_1 L_1 \dot{x_1} + x_2 L_2 \dot{x_2} + x_3 C_f \dot{x_3} \tag{19}$$

$$\Delta u = K_\alpha V_d x_1 \tag{20}$$

The overall control input expression can be written as (21):

$$u = U_0 + \Delta u = \frac{1}{3V_d}\left(\frac{L_1' di_1^*}{dt} + r_1' i_1^* + V_{cf}^*\right) + K_\alpha V_d x_1 \tag{21}$$

The control rule given in (21) provides a globally asymptotically stable operation. However, it does not provide the desired damping to damp the oscillations caused by the complex conjugate poles of the LCL filter. Therefore, the conventional LF based control scheme is modified with a capacitor voltage error ($x_3$) feedback. The final control rule can be written as (22):

$$u = U_0 + \Delta u = \frac{1}{3V_d}\left(\frac{L_1' di_1^*}{dt} + r_1' i_1^* + V_{cf}^*\right) + K_\alpha V_d x_1 - k_\beta x_3 \tag{22}$$

In this study, a PR controller, given in (23), is used to generate the inverter reference current. In (23), $K_p$ is the proportional gain while $K_r$ is the resonant gain. $\omega$ is the resonant frequency and $\omega_c$ is the cutoff frequency. The PR regulator output represents the inverter current reference and can be formulated using the Laplace Domain, as in (24).

$$G_{PR}(s) = K_p + \frac{2 * K_r w_c s}{s^2 + 2w_c s + w^2} \tag{23}$$

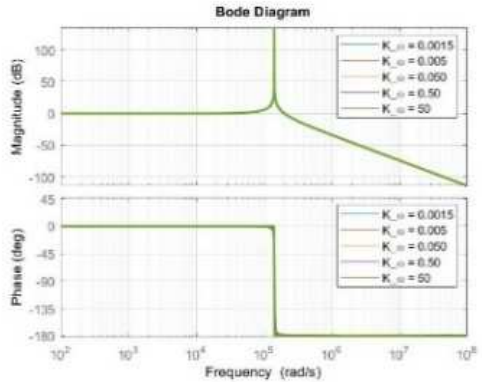
$$I_1^*(s) = [I_2^*(s) - I_2(s)] G_{PR}(s) \tag{24}$$

A closed-loop transfer function, which links the reference to the measured grid utility, is formulated in the frequency domain in order to predict the behavior of the AFE converter with the LCL filter, as in (25).

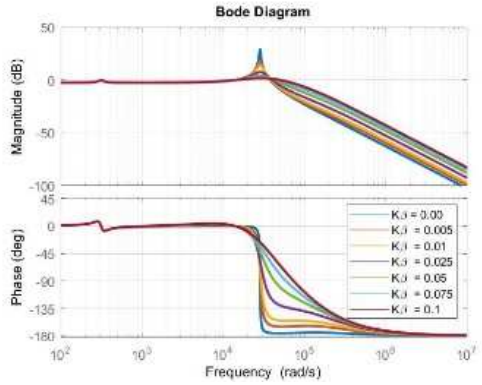
$$TF(s) = \frac{I_1(s)}{I_1^*(s)} = \frac{bs^3 + es^2 + gs + d\omega^2}{Ds^5 + Fs^4 + Gs^3 + Hs^2 + Ls + M} \tag{25}$$

where

$$\begin{cases} A = L_1 + L_2(1 + 3K_\beta V_o) \\ B = 2\omega_c L_1'(K_p + K_r) \\ D = C_f L_1 L_2 \\ E = 3K_\alpha V_o^2 C_f L_2 \\ F = E + 2D\omega_c \\ G = 2E\omega_c + A + D\omega^2 + L_1' K_p \\ H = 3K_\alpha V_o^2 + \omega^2 E + 2A\omega_c + B \\ I = 6K_\alpha V_o^2 \omega_c + (A + L_1' K_p)\omega^2 \\ J = 3K_\alpha V_o^2 \omega^2 \\ L = I + d + f \\ M = J + d\omega^2 \end{cases} \quad \begin{cases} a = L_2'(1 + 3K_\beta V_0) \\ b = a + L_1' K_p \\ d = 3K_p K_\alpha V_o^2 \\ e = d + 2w_c(b + L_1' K_r) \\ f = 3K_r K_\alpha V_o^2 \\ f = 3K_r K_\alpha V_o^2 \\ g = b\omega^2 + 2\omega_c(d + f) \end{cases}$$




(a)




(b)

Fig. 2. The magnitude and phase responses of proposed system. (a) without capacitor voltage loop ($K_\beta$=0), (b) with capacitor voltage loop ($K_\alpha$= 0.050, $K_\beta \neq$ 0).

To minimize the number of parameters and simplify the obtained transfer function, the filter inductor resistances, $r_1$ and $r_2$, are omitted. Substituting the final switching control obtained in (22) into (2) gives rise to the expression of (25).

The effectiveness of the proposed voltage feedback loop which is added to the conventional LF based control scheme is investigated. Fig. 2(a) and (b) show the frequency response of the proposed controller when there is a 10% deviation in all three component values of the LCL parameters with and without the capacitor voltage loop, respectively, at the same time. It can be observed in Fig. 2 (a) that although different $K_\alpha$ were used in the control scheme, which does not contain the added capacitor voltage loop ($K_\beta$=0), the resonance of the LCL filter cannot be damped. However, the desired resonance damping can be obtained when the additional capacitor voltage loop is enabled, as depicted in Fig. 2(b). Additionally, when both control methods are used, it can be noted that there is no steady-state error (0 dB magnitude at 60 Hz) or phase-shift (0° phase at 60 Hz) in the utility current.

### *B. DAB RMS Current Minimization Scheme*

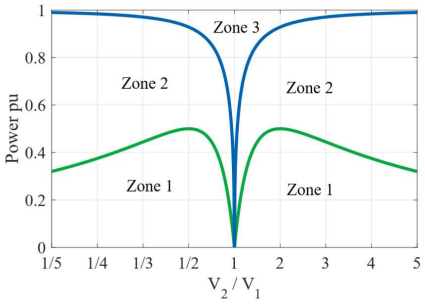
The high circulating current in the DAB only contributes to degradation of the performance of the converter. Therefore, the RMS current minimization for any given average power becomes the key objective to mitigate this issue. The RMS currents are formulated in (12) – (16). The three control variables are $D_1$, $D_2$, and $\varphi$. The objective function, $f$, is the RMS current. The constraint, $g$, is the average power. $\delta D_1$, $\delta D_2$ and $\delta\varphi$ are the incremented variations to compensate for power mismatch among each module of the ISOP. The LM function is formulated in (26).

$$\Lambda(D_1, D_2, \varphi, \lambda) = f(D_1, D_2, \varphi) + \lambda g(D_1, D_2, \varphi) \tag{26}$$

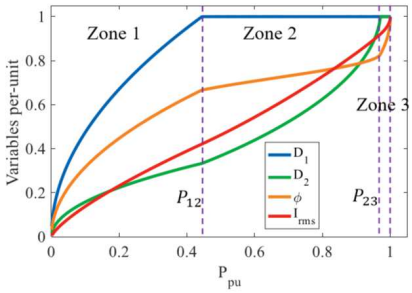
The optimum solution is described by a set of equations of the gradient of the LM for the DAB, as written in (27).

$$\nabla\Lambda = 0 \rightarrow \begin{cases} \frac{\partial \Lambda}{\partial D_1} = 0 \\ \frac{\partial \Lambda}{\partial D_2} = 0 \\ \frac{\partial \Lambda}{\partial \varphi} = 0 \end{cases} \tag{27}$$

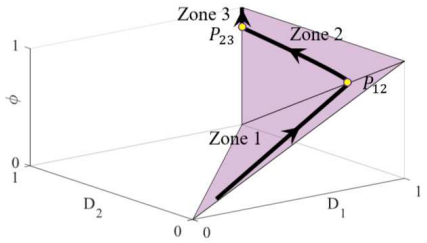
In the case of a well-balanced DAB module, the augmented variations are equal to zero. There are five regions, as defined in [25], and each has its own $f$, $g$, and $\Lambda$.




(a)




(b)




(c)

Fig. 3. (a) Optimal zones of operation, (b) the optimal per-unit values for $D_1$, $D_2$ and $\varphi$, (c) the optimal trajectory of $D_1$, $D_2$ and $\varphi$.

Fig. 3(a) shows the three regions on the optimal trajectory. These zones are analyzed and the relation of each region and boundary between them is formulated [25]. The first region corresponds to the low power region, where $D_1$ and $D_2 \leq 1$. When the DAB output voltage is greater than the input voltage, $V_2 > V_1$, the optimal trajectory falls on $-D_1 + D_2 + \varphi = 0$.

According on the LM optimization for a single module, $V_1D_1 = V_2D_2$ is obtained.

$$\varphi = D_1 - D_2 \tag{28}$$

$$\varphi = D_1 - \frac{V_1}{V_2} D_1 \tag{29}$$

$$D_{1z1} = \frac{V_2}{V_2 - V_1} \varphi \tag{30}$$

$$D_{2z1} = \frac{V_1}{V_2 - V_1} \varphi \tag{31}$$

The trajectory is on the borderline of the right and middle regions. The power equation of either of them can be used. The per-unit power is shown in (32).

$$P_{z1} = 2D_2\varphi \rightarrow P_{z1} = \frac{2V_1}{V_2 - V_1} \varphi^2 \tag{32}$$

This zone terminates when $D_1 = 1$ which means $\varphi = \frac{V_2 - V_1}{V_2}$. Substituting this $\varphi$ into (32) yields $P_{12}$, the power at the boundary of zones 1 and 2, as given in (33).

$$P_{12} = 2V_1 \frac{V_2 - V_1}{V_2^2} \tag{33}$$

Fig. 3(a) shows the three operating regions for the DAB, where zone 1 represents the low power region, zone 2 the medium power region, and zone 3 the high power region. Fig. 3(b) demonstrates the different values in per-unit that the TPS variables can have for each power region. Fig. 3(c) shows the optimal trajectory for TPS variables for each zones.

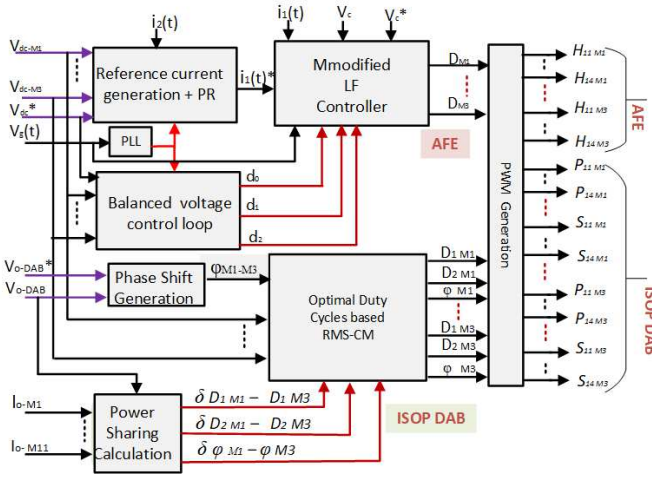



Fig. 4. Control structure of the fast charger.

## C. Control Structure

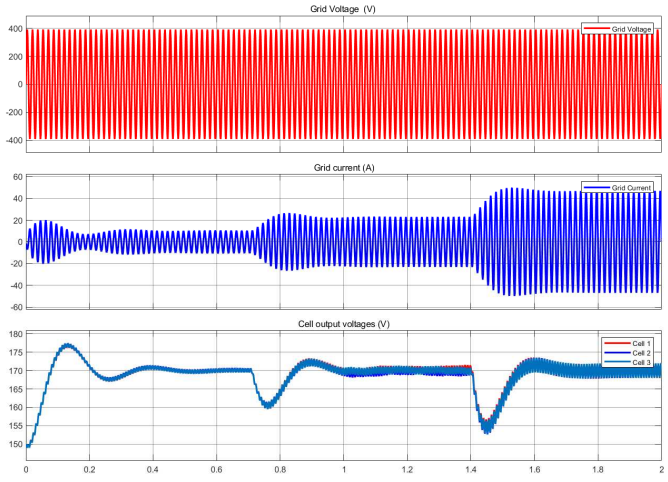
Fig. 4 shows the overall control structure for a single-phase three cell scaled down version of the proposed system. The AFE is controlled by using the modified LF based control approach. The overall AFE controller consists of three main control blocks. The first step is to generate the reference current, as formulated in (24). The average DC bus value of the AFE is controlled by a PI regulator. The output of the PI is multiplied by the reference sine wave obtained from the PLL block to generate the $i_2(t)$ current reference. The final grid current reference is obtained by applying the current error to the proportional resonant controller. The reference current is then fed to the modified LF controller implemented, as in (22), to obtain the final modulation index for the converter. In order to mitigate the effect of unbalanced loading and parameter mismatching, the balanced voltage control loop is added. The augmented duty ratio from this block is added to the LF control block to adjust the final switching function.

To achieve the optimum performance of the ISOP DAB converter, the RMS current minimization is formulated. Additionally, a power sharing method is used to compensate for power unbalances in the DAB converters. Similar to the AFE, three main control components are implemented for the ISOP DAB. The initial phase-shift of the DAB converter is calculated through a PI controller. The power sharing calculation component computes the incremented TPS variables for the power mismatch. The output of both the phase-shift generation and power sharing calculation blocks are fed to the optimization process to finally compute the optimal TPS variables that minimize the RMS current for any given power. Equations (29), (30) and (31) show the calculations for the optimal TPS variables for the low power zone. Detailed description and implementation can be found in [24] for the AFE and [25] for the DAB converter.

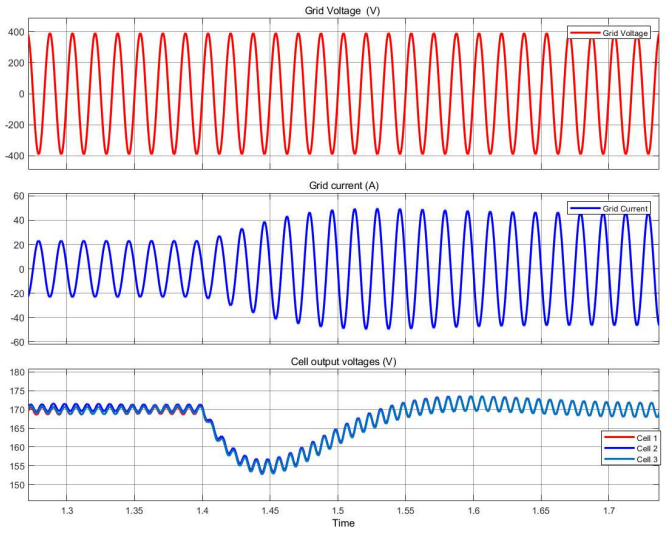
## IV. Simulation Results

To validate the proposed control structure, simulations were carried out using the MATLAB/Simulink software. A single-phase, three module converter was used to verify the presented algorithm. The dynamics of the fast charger for the worst case scenario are discussed and presented. The converter was tested for all three power regions, as discussed in the controller section.

Fig. 5 shows the grid voltage and current and the three DC bus voltages of the AFE. The tracking performance of the DC bus voltages and grid current can be seen for all three regions for both steady state and transient operation. In zone 1, which is the low power region, the system was loaded at 23% (0s-0.7s). In zone 2, the medium power region, a step load was applied to bring the converter total power to 50% (0.7s-1.4s). In the last scenario, a 50% load step up was added to bring the system at full capacity (1.4s – 2s). The goal of this test is to ensure that under the worst condition, the DC bus voltage is

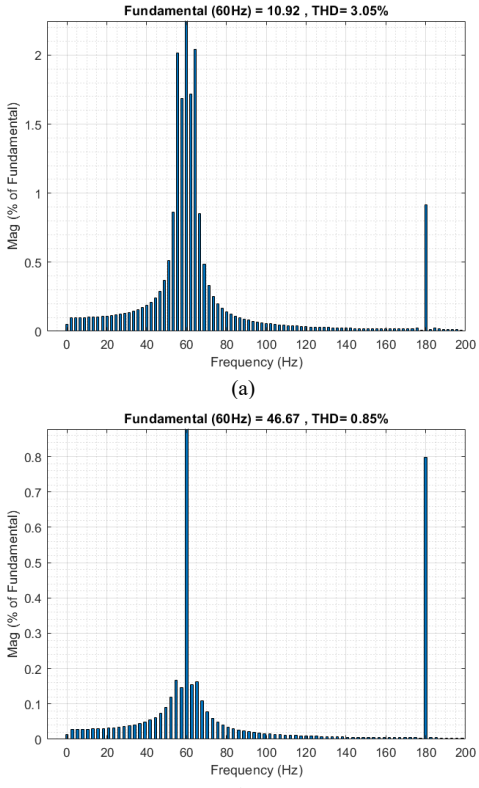



(a)




(b)

Fig. 5. (a) Grid voltage and current, and the three DC bus voltages of the AFE. (b) Expanded view of (a) at 50% load step.



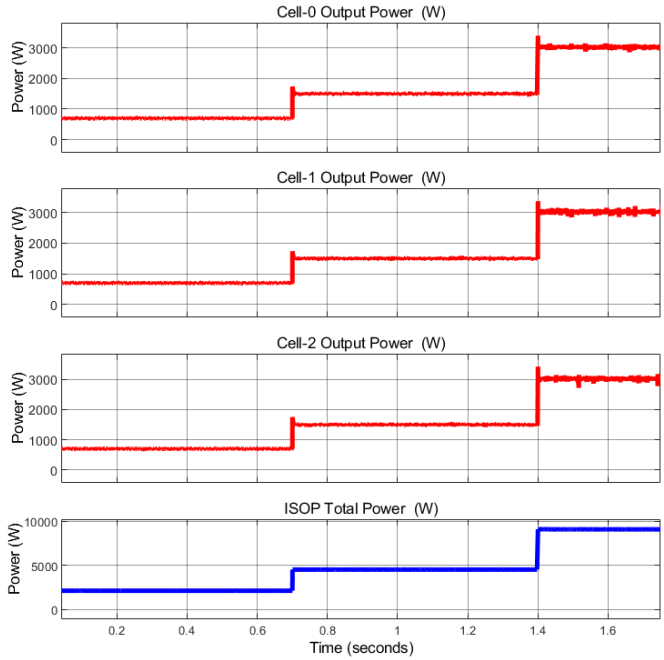

(a)

(b)

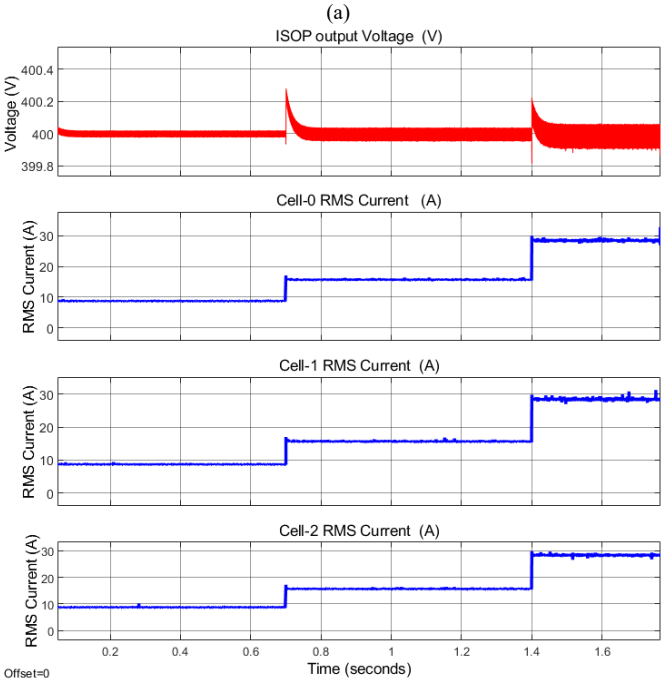
Fig. 6. (a) Grid current THD for the low power region (b) Grid current THD for the high power region.

limited by 10% over/undershoot and the grid current is maintained sinusoidal and in phase with the grid voltage. As seen in Fig. 5(a) and (b), during load steps the control provides robust voltage and current performance. Fig. 5(b) is an expanded view of Fig. 5(a) at 50% load step. To further prove the performance of the control strategy, the THD of the grid current is measured for the low and high power regions. At low power, the THD is low (3.05%). The results are shown in Fig. 6(a) and (b).

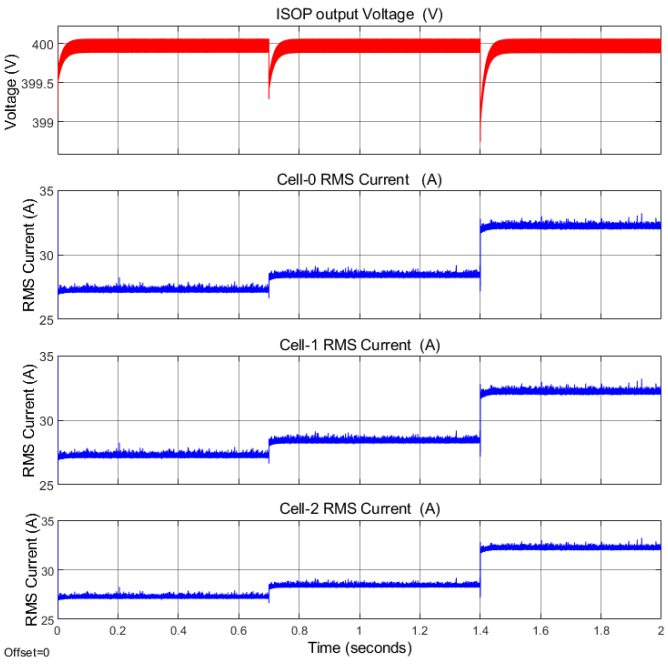
In the following figures, the performance of the ISOP DAB converter is presented. There are three principal goals that are accomplished in this section: the performance of the RMS current minimization, the power sharing, and DC output voltage regulation. In order to study and validate the RMS current minimization, two control methods were applied and their performances were compared for the same power levels. Fig. 7 (a) – (c) demontraste these three operating zones. Fig. 7(a) shows the power regions for 23%, 50% and 100% power rated.




(a)



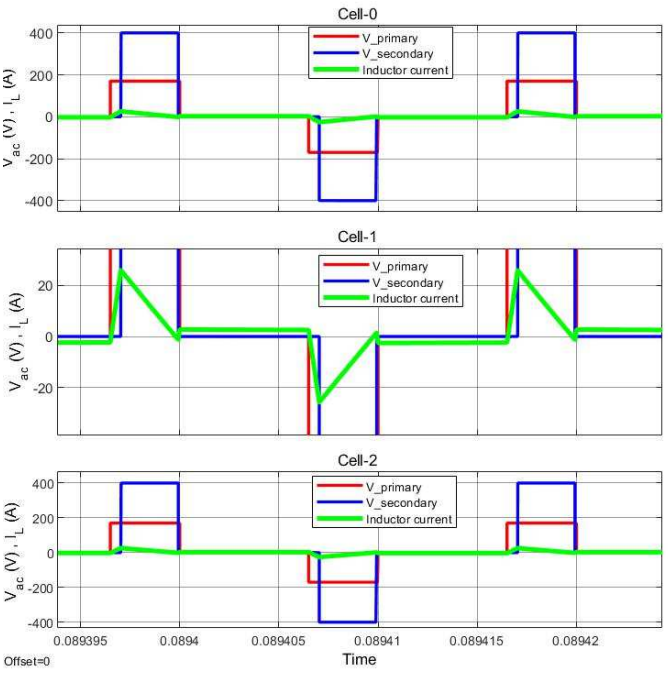

(b)



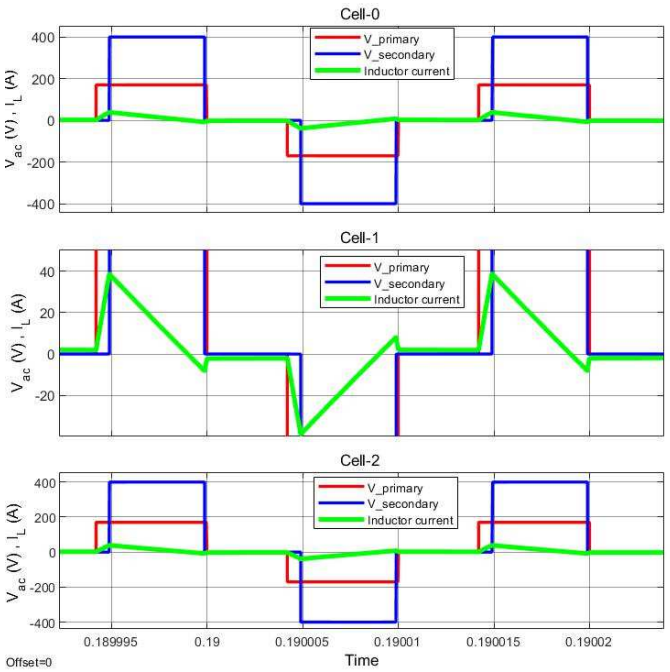

(c)

Fig. 7. (a) Average and total power transfer for the ISOP (b) output DC voltage and the RMS current under TPS (c) output DC voltage and the RMS current under SPS.

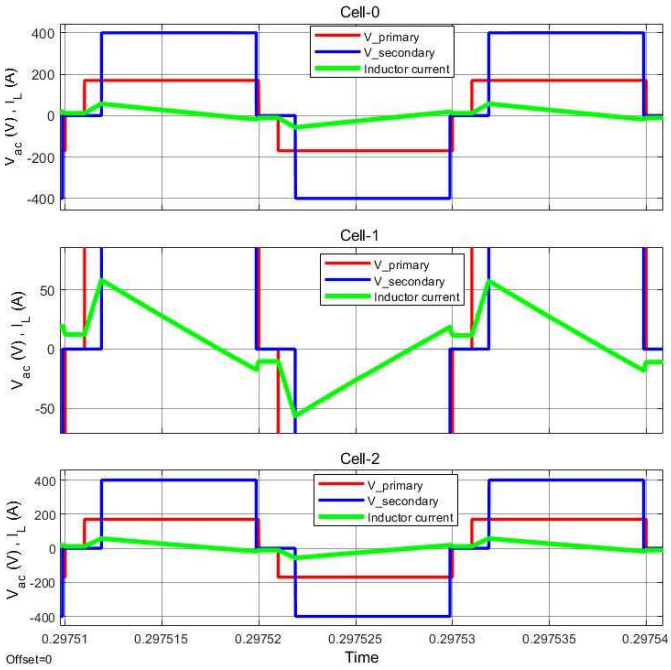
The TPS method was compared to the SPS method to evaluate the RMS current minimization algorithm. In Fig. 7(b), the TPS method was used to minimize the RMS current, while in (c) the traditional SPS method was used. It can be seen that for the same power level the TPS provide better performance. The RMS current is decreased by 19.7A at low power zone, 14A at the medium power zone, and 3A at the high power zone. Therefore, from the comparison between the SPS and the TPS,




(a)




(b)




(c)

Fig. 8. Primary and secondary voltages , and primary current of the transformer under TPS control (a) low power region, zone 1 (b) medium power region zone 2 (c) high power region zone 3.

one can see that the applied RMS current minization based TPS technique improves the converter performance while transfering the same power. It can be noticed that the converter shares the same power level between each cell of the ISOP. Ultimately, the goal of the output voltage is to reflect any load step effects on the AFE side to maintain a stiff output DC voltage. As seen in Fig. 7(b) and (c), the over/undershoot of the output of the converter is less than 1% during the load steps. This improves the voltage regulation. Fig. 8(a)–(c) shows the

primary and secondary voltages and primary current of the high frequency transformer for each cell of the ISOP under TPS control at all three regions.

## V. Conclusion

This paper presents the control strategy for the AFE and ISOP DAB converter to achieve robust current control performance, DC bus voltage balancing for the AFE, and RMS current minimization and power sharing for the ISOP DAB converter. Controller expressions are formulated for both parts of the system. Simulation results demonstrate the performance of the modified LF based current control and the TPS based RMS current minimization method. The employed control for the AFE provides low THD, even at low power operation, and maintains high tracking accuracy for the output DC link voltages, even under the worst condition. TPS method with the proposed optimization decreases the RMS current by a wide margin, especially at low power, thus increasing the efficiency of the converter. Additionally, the load power is shared equally between the cells of the ISOP and the output voltage of the ISOP sees little disturbance during transient.

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