A TCAD Simulation Study of Three-Independent-Gate Field-Effect Transistors at the 10-nm Node

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***Abstract*— Three-independent-gate FETs (TIGFETs) are Schottky-barrier-based devices, which can be reconfigured to be either n- or p-type allowing for innovative compact logic gate implementations. In this article, we present an aggressively scaled 10-nm gate-all-around silicon–germanium nanowire TIGFET device evaluated with Synopsys Sentaurus Poisson-based Technology Computer-Aided Design (TCAD) simulations at a 0.7-V nominal supply voltage as typically used at this technology node. The operation of the TIGFET device is described in detail, with particular care given to the majority current contributions for each operating mode. When considering a silicon–germanium channel, the maximum TCAD-simulated current drive is 880.20 and 806.58 μA/μm for n- and p-type operation, respectively, thus making TIGFET devices competitive with FinFET technology at the 10-nm node. These simulations are verified using device physics calculations. Further simulations of the carrier densities for each of the TIGFET-operating configurations are performed to confirm that the simulated device is operating as intended.**

***Index Terms*— Reconfigurable transistors, silicon nanowire transistor, silicon–germanium nanowire transistor, Technology Computer-Aided Design (TCAD) simulations, three-independent-gate FETs (TIGFETs).**

I. Introduction

THE conventional drive in the semiconductor industry has been based on the improvement of device performance and the scaling of these devices, as exemplified by Moore's scaling "law," which pushes for the doubling of transistors in a given integrated circuit every two years. However, as the physical sizing limits of contemporary manufacturable transistors are being reached, Moore's law is coming to an end and innovations on standard MOSFET such as the trigate FinFET are necessary to extend these devices to the sub-5-nm node. Examples of such innovations include the use of novel geometries (gate-all-around designs [1]), nonplanar device structures such as carbon nanotubes [2], high-mobility channel materials (strained silicon-germanium [3], and 2-D materials [4] such as graphene [5] and molybdenum disulfide [6]), and high-κ dielectrics [7]. Although effective, all of these innovations have generally been used to extend the standard FinFET technology. Of greater interest are completely novel technologies (which can be combined with any or multiple of the ideas listed above) with exciting switching characteristics such as tunneling FETs [8], ferroelectric FETs [9], and spintronics-based devices [10], all of which have been demonstrated for applications in both logic and memory. Our focus is on a similarly novel-switching device, which doubles as a dopant-free technology solution.

Standard FETs are made from semiconductors which have ambipolarity in their carriers. This means that the conduction of holes and electrons occurs simultaneously in these devices and so doping is required to select whether the device conducts primarily holes (as in a p-type device) or electrons (as in an n-type device). However, doping at the 10-nm node and below is becoming increasingly uncontrollable and undesirable [11]. Rather, by exploiting this ambipolar property of semiconductors instead of suppressing it, we can create reconfigurable devices that have the capability to alternate between n- and p-type behaviors after fabrication. Devices built based on this principle bring an additional boost to scaling because of their ability to enhance system functionality by simplifying logic gate implementations [12], [13].

Reconfigurable FETs (RFETs) have been demonstrated using silicon [14], germanium [15], and 2-D channel materials including graphene [16], molybdenum ditelluride [17], and tungsten diselenide [18]. The three independent-gate FET (TIGFET) is an experimentally demonstrated multiple independent-gate reconfigurable device [14], [19] whose dual-switching ability originates from electrostatic modulation of Schottky barriers at the source and drain contacts using additional gate terminals called polarity gates (PG). This work focuses on simulations based on TIGFET devices composed of silicon and silicon–germanium materials.

This article introduces TCAD simulations performed using Synopsys Sentaurus [20] for 10-nm-gate TIGFET silicon nanowire [21] and silicon–germanium nanowire devices. These device simulations are designed using the industry standard supply voltage V_{DD} of 0.7 V so as to verify their potential for integration alongside contemporary devices [22]. Using

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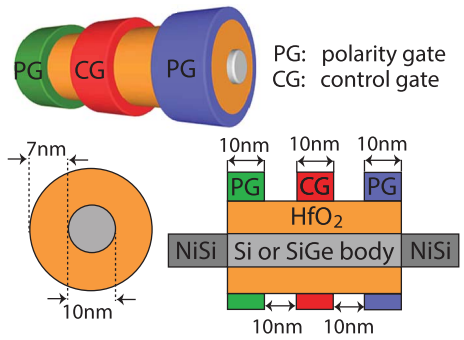

Fig. 1. Structure of the designed device with 10 nm gate lengths and gate spacings. The total channel length is 50 nm.

the industry standard supply voltage also allows for a fair assessment of TIGFET device performance at the 10-nm node. The maximum TCAD-simulated current drive for the silicon nanowire design at the 0.7-V supply voltage is 115.63 and 108.02 μA/μm for n- and p-type operation, respectively. To boost the current drive of the TIGFET devices while maintaining the low supply voltage, a silicon–germanium nanowire was simulated. This current boost is enabled by the increased effective mobility of the silicon–germanium carriers and the strain added to the lattice by the introduction of the germanium atoms [3]. This resulted in current drives of 880.20 μA/μm for n-type operation and 806.58 μA/μm for p-type operation, which are approximately 8$\times$ higher than the current drives in the silicon nanowire simulations. The trade-off is that the silicon nanowire configuration is able to achieve extremely low off current I_{OFF} thanks to the cut-off provided by the Schottky barrier, whereas the silicon–germanium nanowire configuration has slightly higher I_{OFF} values. Our silicon–germanium nanowire TIGFET is competitive with contemporary FinFET technology, which has similar ON and OFF currents to those seen in our simulations [22].

The rest of this article is organized as follows: Section II discusses the operation and theory of the TIGFET device; Section III provides an overview of the TCAD simulations for the silicon nanowire device and discusses the validity of the results using device physics calculations and carrier density simulations; Section IV introduces a silicon–germanium nanowire TIGFET simulation for higher current drive; finally, Section V discusses the significance of and contribution provided by this work.

II. TIGFET Operation

A. Device Overview

A TIGFET device requires a channel made of a semiconductor material, metallic source and drain contacts, and three gate electrodes: the control gate (CG) and two symmetric PGs at the source and drain to act as electrostatic doping means at the Schottky barrier interfaces. The device structure is illustrated in Fig. 1.

Though aggressive, the 10-nm gate spacings are viable as previously reported TIGFET fabrication routes have relied heavily on self-aligned gating techniques [14].

The standard fabrication process for a TIGFET device is compatible with modern silicon FinFET processes. The fabrication for a device similar to the one simulated in this study would include nanowire formation by a deep reactive ion etch (DRIE) Bosch process (note that this can be modified for a multiple-nanowire stack as seen in [14]), PG patterning, and self-aligned CG patterning, all of which are steps commonly used in standard silicon processing. Repeated oxidation and etching have been previously used in RFETs to round and thin the nanowire, and the addition of omega-shaped top gate stacks using titanium, titanium-nitride, and platinum has been shown to cause strain leading to elevated carrier mobility [15]. After the gates have been formed, nitride spacers are used for isolation and a nickel layer is deposited, patterned, and annealed to form nickel silicide (NiSi) contacts at the source, drain, and gate contacts. This top-down process enables large-scale fabrication concurrent to standard FinFET processing with no transfer procedures required. Further details with regard to TIGFET device fabrication can be found in [14], [15], and [18].

Standard reconfigurable devices are capable only of device polarity reconfiguration based on the applied PG bias [14], whereas TIGFETs have demonstrated two additional operation modes: the dynamic control of the threshold voltage [19], and the dynamic control of the subthreshold slope beyond the thermal limit [23]. Nevertheless, this work focuses only on the polarity reconfiguration aspect of TIGFETs.

Fig. 2(a) shows a band diagram of combined n- and p-type operation at equilibrium assuming both PGs are set to the same values. As seen in the band diagrams, the chosen PG voltages determine which carriers will dominate in the channel: if the PGs are increased to the supply voltage (V_{DD}), the device will be n-type (electron) carrier-dominated, as seen in Fig. 2(b) and (c), whereas if the PGs are grounded (0 V), the device will be p-type (hole) carrier-dominated, as seen in Fig. 2(d) and (e). The state of the CG determines whether the selected carriers will pass through, thus effectively turning the device ON or OFF. Note that both n- and p-type carriers are allowed through to form the channel if the CG polarity is at the same drive as the PG polarities, as seen in Fig. 2(c) and (d).

B. Circuit Design Benefits of the TIGFET

TIGFETs are functionality enhanced devices at the circuit level and provide multiple benefits because of their elevated switching capabilities and compact gate designs. This is because of a single TIGFET's ability to emulate two series transistors, as seen in Fig. 3. The resulting compact logic gates include a two-input NAND from three TIGFET devices [Fig. 3(b)] instead of four CMOS devices, and a three-input XOR from four TIGFET devices [Fig. 3(c)] instead of 12 CMOS devices. Fig. 3(c) shows that a two-input XOR, three-input XOR, and three-input majority gate can all be made from the same four TIGFET transistors by adjusting the terminal voltages [13]. Another circuit improvement is the increased switching speed of the gates when compared to a CMOS inverter of the same technology because of fewer series transistors being required to implement the same logic functions. This results in potential improvements in not only

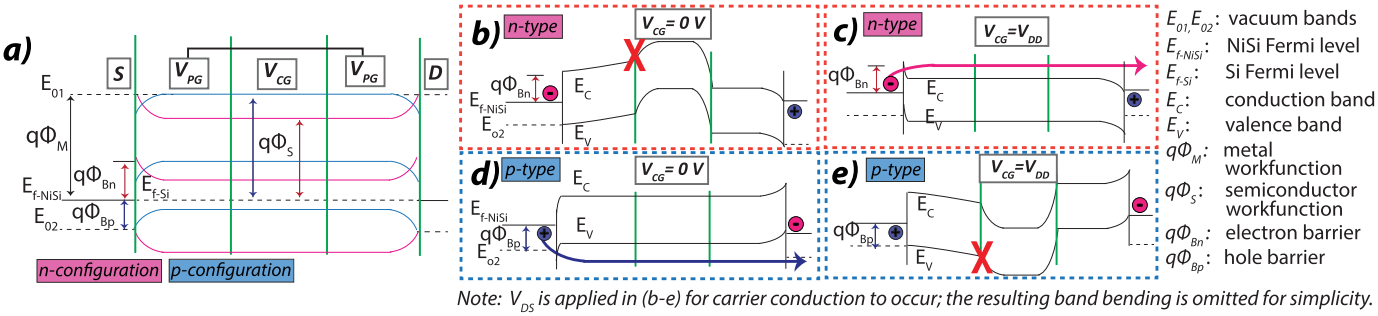

Fig. 2. (a) Band diagram assuming the same bias for both PGs (pink lines correspond to n-type operation, $V_{PG} = V_{DD}$; blue bands correspond to p-type operation, $V_{PG} = 0$ V) at equilibrium (no V_{GS} applied). (b) For the n-configuration, when $V_{CG} = 0$ V the OFF condition occurs, blocking the electron-carrier flow. (c) For the n-configuration, when $V_{CG} = V_{DD}$ the ON condition occurs, allowing the electron-carrier flow. (d) For the p-configuration, when $V_{CG} = 0$ V the ON condition occurs, allowing the hole-carrier flow. (e) For the p-configuration, when $V_{CG} = V_{DD}$ the OFF condition occurs, blocking the hole-carrier flow.

delay but also power consumption [24]. Thus, TIGFET-based logic gates require fewer transistors than their CMOS counterpart, and are overall more expression rich and efficient at the circuit level.

C. Current Transport Calculations

The two primary forms of current transport at a metal semiconductor junction (that is, a Schottky barrier) are thermionic emission (TE) and field emission (FE). The former refers to thermal transport where only carriers with energy greater than the potential barrier seen at the barrier height (ϕ_B) can make it into the channel and contribute to the ON-current. The latter refers to carriers being able to tunnel through the potential barrier into the channel. Other less significant current transport into the channel can be caused by diffusion of majority carriers into the space charge region, recombination in the space charge region, and minority carrier injection from metal to semiconductor [25].

In this article, we consider a simplified approximation of the current drive. A more thorough analytical solution for TIGFET current conduction is seen in [26]. Our solution assumes the operating temperature to be 300 K and ignores extreme temperature effects, although an increased temperature implies increased thermal emission because of the presence of more excited carriers. Fixed charges or charged traps are presumed negligible in comparison to the effects expected from the voltage drops from the gate voltage (V_G) and source-to-drain voltage (V_{DS}).

To start, we calculate the barrier height during the OFF-state (ϕ_{Bpo}) as follows:

$$\phi_{Bpo} = E_g - q(\phi_m - \chi). \tag{1}$$

Next, for the TE-based solution, we take into account the image-force lowering potential

$$\Delta\phi_p = \sqrt{\frac{q \cdot \overrightarrow{E_{TE}}}{4\pi \cdot \epsilon_s}} \tag{2}$$

where $\overrightarrow{E_{TE}}$ is the maximum TE-limited electric field, so that the effective barrier height for the TE solution becomes

$$\phi_{Bp-TE} = \phi_{Bp0} - \Delta\phi_p + \phi_t. \tag{3}$$

The Schottky barrier thickness during this OFF-state operation is too large for significant tunneling, thus the primary current transport method in the OFF-state is TE [27]. This means that only the carriers with enough energy to exceed the potential barrier will enter the channel and contribute to the device current drive. The equation for the current drive assuming TE is

$$J_{TE} = \left(\frac{4\pi \cdot q \cdot m^{*2}}{h^3}\right) \cdot T^2 \cdot \exp\left(\frac{-q \cdot \phi_{Bp-TE}}{kT}\right) \cdot \exp\left(\frac{-q \cdot V_{APP}}{kT}\right) \tag{4}$$

which requires first solving for the maximum electric field, $\overrightarrow{E_{TE}} = ((q \cdot N_A \cdot W_D)/\epsilon_s)$, and using this to solve for the depletion width $W_D = (((2 \cdot \epsilon_s)/(q \cdot N_A))(\Phi_{bi} - V_{APP} - ((2 \cdot kT)/q)))^{1/2}$. The applied voltage is $V_{APP} = a \cdot V_G + b \cdot V_{DS}$, where a and b are coupling factors used to resolve the fact that these two external sources do not contribute equally to band-bending [28].

If we consider an applied gate bias as when the Schottky junctions are in the ON-state, however, there is enough band bending to change the barrier heights. This diffusion potential, V_{eff}, is equal to the change in the flatband voltage, V_{FB}, and refers to the upward bending of the energy bands

$$V_{eff} = V_{FB} = (\phi_m - \phi_s). \tag{5}$$

The effective barrier height for the FE-based solution includes gate biasing and does not consider TE-induced barrier-lowering effects

$$\phi_{Bp-FE} = \phi_{Bp0} + V_{eff}. \tag{6}$$

When the applied gate voltage V_G is smaller than the flatband voltage, the conduction band will increase, thus increasing the barrier height and lowering current drive. Meanwhile, with the applied gate voltage increased beyond the flatband voltage, the conduction band will decrease and current drive will increase with the dominant current transport method as TE. As this gate voltage is increased further, the barrier will be thinned and FE tunneling becomes dominant through this barrier. Thus, in ON-state, a TIGFET behaves as a regular Schottky junction device for which FE is the dominant transport mechanism because of the thinning of the barrier with applied gate bias.

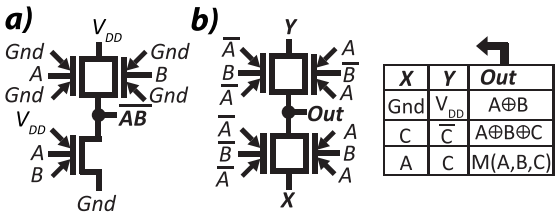

Fig. 3. TIGFET equivalent circuit designs for (a) two-input NAND gate, and (b) two-input XOR gate, three-input XOR gate, and three-input MAJ gate.

To mirror our TCAD simulation, in the tunneling scenario, we approximate the barrier as a triangular potential well using the Wentzel–Kramers–Brillouin (WKB) approximation [25]

$$\Theta = \exp\left(\frac{-4}{3}\frac{\sqrt{2\cdot q\cdot m^*}}{\hbar}\cdot\frac{\phi_{\mathrm{Bp-FE}}^{3/2}}{\overrightarrow{E_{\mathrm{FE}}}}\right). \tag{7}$$

The relevant electric field is recalculated as $\overrightarrow{E_{\mathrm{FE}}} = (\phi_{\mathrm{Bp-FE}}/L)$, where L = the source-to-drain distance, 50 nm. Note that in the tunneling solution, this electric field reflects the local band-bending with its dependence on ϕ_{Bp}, so the band-bending is still taken care of.

The tunneling current is then calculated as a product of the carrier charge q, average carrier velocity v_R, and density, where the carrier density consists of the tunneling probability Θ multiplied by the number of available carriers, n

$$J_{\mathrm{FE}} = q\cdot v_R\cdot n\cdot\Theta. \tag{8}$$

We then use the thermionic current drive equation (4), and the tunneling current drive equation (8), to analytically estimate the p-type current drives in a silicon TIGFET operating in different modes assuming a diameter of 10 nm. This is done using the values in Table I. Recall that TE is the primary current transport method during OFF-state operation; thus, we solve the thermionic current drive equation for the OFF-state operation and we get $J_{\mathrm{TE}} = 0.02\ \mu\mathrm{A}/\mu\mathrm{m}$. Meanwhile, for ON-state operation, we solve the tunneling current drive equation and we get $J_{\mathrm{FE}} = 302\ \mu\mathrm{A}/\mu\mathrm{m}$. Note that these equations calculate the theoretical current limits of a single Schottky barrier.

III. Silicon Nanowire Simulations

A. Simulation Packages

This section develops the assumptions made in the Synopsys Sentaurus TCAD simulations. Synopsys Sentaurus supports the basic and compound semiconductors used in industry, including the silicon and silicon–germanium materials of interest in this work [20]. In this section, we consider the simulation packages necessary for the successful simulation of the TIGFET device. The standard axis-aligned Sentaurus mesh is used, with some added boundaries. Specifically, the refinement window is set to consider the current flow only under the oxide where the channel will be formed, and the standard 0.25-nm-fine cuboid mesh is converted to a mixed-element hybrid mesh to fully encompass the cylindrical nature of the nanowire.

TABLE I
Device Physics Assumptions [25]

	Silicon-nanowire	Silicon 70%-Germanium 30%-nanowire
Semiconductor electron affinity, χ_s	4.05 eV	4.00 eV
Semiconductor bandgap, E_g	1.12 eV	0.997 eV
Semiconductor doping density, N_A	$1\cdot10^{16}$ cm^{-3}	$1\cdot10^{14}$ cm^{-3}
Semiconductor intrinsic concentration, n_i	$9.65\cdot10^{9}$ cm^{-3}	$2.4\cdot10^{13}$ cm^{-3}
Semiconductor workfunction, ϕ_s	4.52 eV	4.64 eV
Semiconductor permittivity, ϵ_s	11.9	16
Electron effective tunneling mass, $m^*_{t,e}$	0.126	0.086
Hole effective tunneling mass, $m^*_{t,h}$	0.094	0.045
Metal workfunction, ϕ_m	4.755 eV	4.85 eV

The source and drain contacts are formed using the automatic circuit contact function, which assumes fully silicided ohmic contacts. As explained in Section II-C, the main component to the current flow at the Schottky junctions in OFF-state is thermal conduction, which can be approximated using the Fermi physics package and Schockley–Read–Hall recombination. Both minority and majority carrier bulk mobilities are considered using the Philips unified mobility model, which describes the temperature dependence of the mobility, as well as considers electron–hole scattering, impurity clustering, and screening of ionized impurities by charge carriers [29]. Mobility degradation is considered with respect to the electric field perpendicular to the semiconductor interface using the Enormal package. Bandgap narrowing effects are considered using the Old Slotboom model with additional contributions included with the effective intrinsic density model. To account for band-to-band tunneling (BTBT), which is dominant in the Schottky junctions in ON-state operation, the WKB approximation is used.

Table I contains all the starting assumptions for the simulations that follow.

B. Silicon Nanowire Structure

Similar to demonstrated devices, the Schottky barrier in the TCAD simulations was created by a nickel silicide (NiSi)-to- silicon (Si) contact. NiSi is a midgap metal and can thus provide symmetric switching between n- and p-type carriers. The nanowire configuration was chosen because of its superior electrostatic control over the channel when compared to FinFET technology at the same node [2]. The gate-all-around configuration used in this simulation is standard for nanowire designs [14] and provides increased gate control [1]. A 5-nm hafnium dioxide (HfO_2) layer was used as the gate dielectric; this corresponds to an equivalent oxide thickness (EOT) of approximately 0.8 nm.

Modifications specific to the silicon nanowire structure were made for the purpose of shifting the n- and p-type current

drive symmetry and include elevating the p-type body doping to 10^{16} cm^{-3} and using strained ⟨001⟩ silicon. The latter modification has been used in fabricated RFETs through repeated oxidation steps and omega-shaped gate stacks, and has resulted in a maximum 1.5-GPa compressive lateral strain [30]. The corresponding effective masses used in our simulations are reasonable compared to what is expected sub-50 nm in a typical strained device; these are reported in Table I. To get these values, we modified the effective tunneling masses of standard silicon devices [25] through strain assumptions reported in [31], which show strained silicon has a mobility enhancement of 1.5–1.7× over unstrained silicon. The Si and NiSi workfunctions are optimized to obtain symmetric switching characteristics [32]; the optimal NiSi workfunction is 4.755 eV, and the corresponding silicon semiconductor workfunction is 4.52 eV; these workfunction values are in the realm of what is physically feasible for NiSi and Si, respectively, [25], [33].

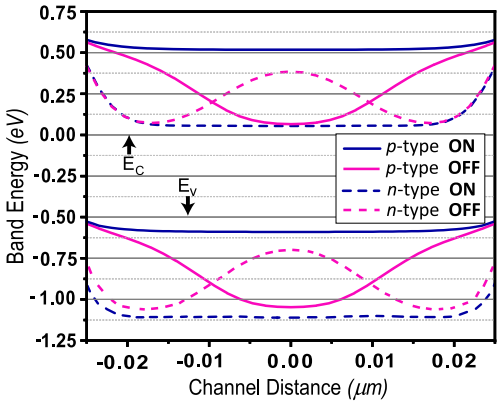

Fig. 4. Conduction (E_C) and valence (E_V) band energies for different configurations. Solid lines reflect p-type in the ON-state showing hole conduction through the channel and in the OFF-state showing blocked current flow. Dashed lines reflect n-type in the ON-state showing electron conduction through the channel and in the OFF-state showing blocked current flow.

C. Carrier Densities and Conduction Band Energies of the Simulations

The conduction and valence band energies are simulated for each of the operating configurations seen in Fig. 2 to verify that the TIGFET simulation is working as intended. The results are seen in Fig. 4. The current flow interruption at the CG (which corresponds to a channel distance of 0 μm) is seen for both n-type (dashed lines) and p-type (solid lines) configurations when the devices are in the OFF states. This matches the theoretical band diagrams in Fig. 2(b)–(e) and confirms that the simulation is functioning as expected. We also note that the conduction band is higher for the p-type configuration, which makes sense because the conduction band is where the p-type carriers are located, and the reverse is true for the n-type carriers in the n-type configuration and the valence band.

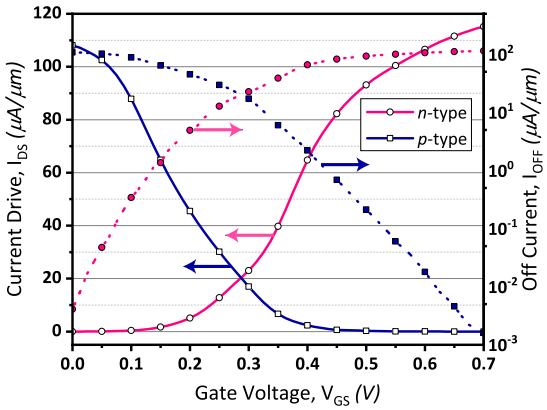

Fig. 5. I_{DS}–V_{GS} characteristics of the simulated device at $V_{DD} = 0.7$ V. The linear scale results show the maximum ON-current and the log-scale results show the minimum OFF-current; the arrows on the curves point to the corresponding axis.

D. Silicon Nanowire Simulation Results

Fig. 5 shows the symmetric maximum current drives achieved at the maximum supply drive of $V_{DD} = 0.7$ V for n- and p-configurations. The maximum current drive for n-type operation is 115.63 μA/μm and for p-type is 108.02 μA/μm. Thanks to the Schottky barrier cutoff, I_{OFF} is extremely low at 4.1 and 1.6 nA/μm for n- and p-type operation, respectively. The 6% asymmetry between n- and p-type operation seen in this simulation is an improvement over the previously published 22-nm TIGFET circuit model [19], which exhibited approximately 10% asymmetry.

The maximum calculated current drive from Section II-B of 302 μA/μm is approximately 2× the simulated maximum current drive for these devices. This difference is because of the calculation's assumption of a single Schottky barrier, whereas the simulated TIGFET device consists of not one but two Schottky barriers: one at each PG. This means that in a TIGFET the carriers will have to travel further and through more barriers than this equation can account for, and thus their carrier mobility is expected to decrease as well. That said, this theoretical solution still provides an estimate that is on the same scale as our simulations which confirms their validity.

For further validation, we consider that the cross section of our simulated nanowire (calculated as 5 nm$^2 \cdot \pi$) is 4× smaller than the cross section of an RFET fabricated in [14] (10 nm$^2 \cdot \pi$), which achieved a maximum current drive of 127 μA/μm using a supply voltage of 4 V. Thus, for a cross-sectional area 4× smaller and a supply voltage 5.7× smaller, we were able to achieve similar current drives in our simulations compared to these fabricated devices. We attribute this discrepancy to our assumptions of perfect operating conditions as well as the fact that the device from [14] is volume-wise 28× larger than our simulation so there is significantly more current degradation in the much wider channel. This comparison helps to endorse our simulated approximation of the current drive.

Fig. 6 shows the current drive as a function of drain voltage for the n- and p-configurations.

Symmetric characteristics are seen for both n- and p-type carriers, with the switching centered around

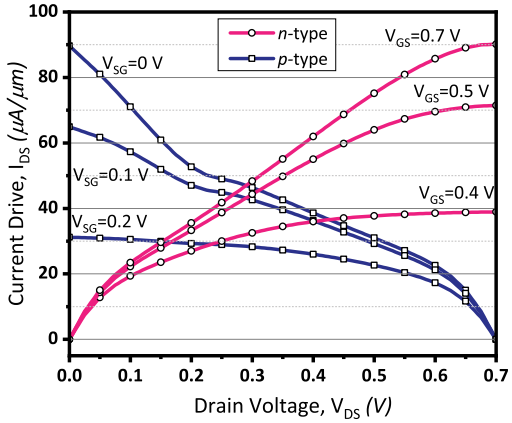

Fig. 6. I_{DS}–V_{DS} characteristics of the simulated silicon nanowire device. Punchthrough effects are seen for the PMOS curves at $V_{SD} = 0$, 0.1 V.

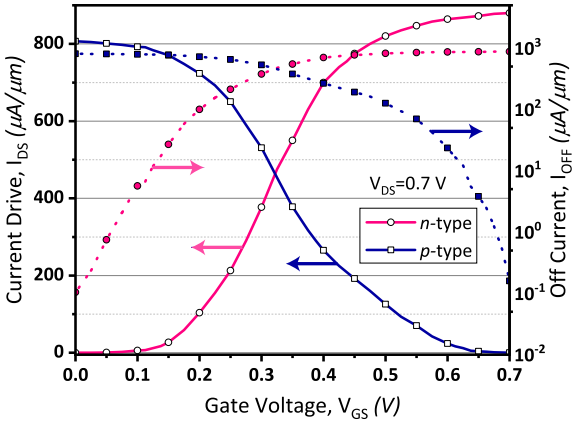

Fig. 7. $I_{DS} - V_{GS}$ characteristics of the silicon–germanium nanowire device at $V_{DD} = 0.7$ V. The linear scale results show the maximum ON-current and the log-scale results show the minimum OFF-current; the arrows on the curves point to the corresponding axis.

$V_{DS} = 0.3$ V. Saturation is seen for all n-type configuration and punchthrough is seen for the device biased p-type at $V_{sg} = 0$ and 0.1 V. This phenomenon occurs in short-channel devices such as this simulation because of the simulated depletion regions of the source and drain reaching each other during high-bias ON-state operation; this in turn lowers the potential and facilitates current flow near the surface of the device.

IV. Higher Current Drive Simulations

A. Silicon–Germanium Nanowire Structure

Next, we consider a 10-nm silicon–germanium nanowire TIGFET TCAD simulation as a higher current alternative to the silicon nanowire. As seen in Table I, the effective masses of both n- and p-type carriers is significantly smaller in silicon–germanium than in silicon, allowing for a higher current drive in transistors built from silicon–germanium. This phenomenon has been exploited extensively in novel devices [3]. Note that a silicon–germanium-based device would require a different metallic contact than NiSi to form the proper Schottky barrier. For simplicity, in these simulations we assume a silicon–germanium nanowire device, which allows for the silicon atoms in the silicon–germanium channel and NiSi metallic regions to interact with each other.

The general structure of the silicon–germanium nanowire device is the same as that of the silicon nanowire design, as seen in Fig. 1. That is, the device is still a gate-all-around nanowire with a 5-nm HfO_2 gate dielectric. The body material is changed from Si to silicon–germanium (SiGe) with a $Si_{0.70}Ge_{0.30}$ concentration, as 30% Ge in a SiGe composition results in a sweet spot of heightened hole and electron mobility [34]. The hole mobility is enhanced by a factor of 1.8× and the electron mobility by a factor of 2.2× compared to the silicon mobilities. Using these estimates, we set our electron and hole effective tunneling masses in the SiGe simulation to $0.086m_0$ and $0.045m_0$ respectively. The body doping is p-type and set to 10^{14} cm^{-3}. The metal and semiconducting workfunctions used are 4.85 and 4.64 eV, respectively, and are close to the values used for the silicon model to favor the NiSi–SiGe contact.

B. Silicon–Germanium Nanowire Simulation Results

As seen in Fig. 7, the maximum current drive achieved with this simulation is 880.20 μA/μm for n-type operation and 806.58 μA/μm for p-type operation. The trade-off for the 8× drive current improvement over the silicon-based simulations are off current values of 104.26 nA/μm for n-type, and 159.12 nA/μm for p-type operation. Although higher than for our silicon simulation, these are still in the same range as the 30-nA/μm I_{OFF} reported by Intel for their 10-nm FinFET technology [22]. The simulated silicon–germanium -nanowire TIGFET current drive is also on the same scale as Intel's reported FinFET technology of 1550 μA/μm [22].

V. Conclusion

This work presents a TCAD simulation for a silicon nanowire gate-all-around TIGFET device with an aggressively scaled 10-nm gate length and gate spacings. A similarly structured novel 10-nm-gate silicon–germanium-based TIGFET simulation is also presented as a solution for designs requiring higher current drive. The supply voltage used in these simulations is the industry standard of 0.7 V to allow for a fair comparison to contemporary 10-nm node FinFET designs which are run at this voltage. The real benefit to TIGFET devices is through their ability for smart circuit designs, which use fewer transistors for the same logic gates as the equivalent FinFET designs. This article has established that the TIGFET is a promising alternative device at the 10-nm node, especially when considering their circuit benefits. The maximum current drives extracted from the resulting I–V characteristics match up well with device physics calculations for the expected Schottky barrier current drive. The silicon nanowire design resulted in extremely low I_{OFF} values thanks to the Schottky barrier cut-off. The silicon–germanium nanowire had slightly higher I_{OFF} values because of the higher mobility of the active carriers, a trade-off for the 8× higher current drive. The silicon nanowire device would work well in applications requiring low I_{OFF}, where high I_{ON} is not as important as in low-power applications, and the silicon–germanium nanowire

device would fare well as an alternative or supplement to contemporary FinFET devices.

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