

Parasitic Capacitance Analysis of Three-Independent-Gate Field-Effect Transistors

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Abstract—*Three-Independent-Gate Field-Effect Transistors* (TIGFETs) are a promising alternative technology that aims to replace or complement CMOS at advanced technology nodes. In this paper, we extracted the parasitic and intrinsic capacitances of a silicon-nanowire TIGFET device using three-dimensional numerical simulations in an attempt to accurately compare its capacitances and, consequently, circuit-level performances to CMOS at comparable nodes. Analytical models of the parasitic capacitances of a TIGFET transistor were derived using techniques such as the equivalent Schwarz-Christoffel transformation and standard cylindrical capacitors and show close agreement with numerical simulations. The maximum capacitance of a TIGFET transistor is $2\times$ larger than for a 15 nm CMOS *High Performance* (HP) device due to the TIGFET's two additional gated contacts, but this is countered by its ability for multiple modes of operation which reduces the effective switching capacitance per device. A TIGFET transistor sees, on average, only a 30% increase in total capacitance compared to a CMOS HP device. Additionally, the TIGFET's increased device functionality can be used to modify the circuit-level architecture of a TIGFET-based design to mitigate the performance impact of its larger device-level capacitance. This combination of a TIGFET's (1) multiple modes of operation, and (2) circuit-level architecture lead to enhanced system performance. In particular, we show that at the 15 nm technology node TIGFET technology has 18% lower energy-delay product for a fan-out of 4 and higher when using 1-bit full-adder logic circuit than for the equivalent node CMOS HP.

Index Terms—Gate All-Around, Parasitic Capacitance, Silicon Nanowire FET, Schwarz-Christoffel transformation, Three-Independent-Gate Field-Effect Transistor.

I. INTRODUCTION

Innovative fabrication advances in *Complementary Metal-Oxide-Semiconductor* (CMOS) *Field-Effect Transistors* (FETs) have led to remarkable chip-level performances. In the early days of CMOS engineering, Dennard's scaling theory stated that by scaling the *Channel Length* (L_g), *Supply Voltage* (V_{DD}), *ON-current* (I_{ON}), and *Intrinsic Capacitance* (C_{int}) by the same factor, the number of MOSFET transistors that could fit on the same die area could be increased exponentially while the power consumption would stay the same. The benefits of Dennard's scaling defined standards down to the 100 nm regime, followed by alternative innovations such as the use of high-mobility channel materials, high- κ dielectrics, and nonplanar structures, all of which helped the continuation of feature size scaling to the 30 nm technology node. Below

this node, however, scaling of the gate length became less effective as the leakage current increased exponentially. The simultaneous difficulty in gate length scaling and increase in contact density in contemporary CMOS designs has led to an unforeseen increase in the *Parasitic Capacitance* (C_{par}) contribution due to fringing field effects. In fact, below the 20 nm node, the parasitic capacitance dominates over the channel capacitance – highlighting the importance of developing novel device structures with lower device parasitics rather than focusing solely on the enhancement of channel transport properties [1].

The parasitic capacitance at advanced nodes (sub-20 nm) is a severe limiter to circuit-level performances. The dimensional scaling influence on the parasitic capacitance of *Silicon Nanowire* (Si-NW)-based [2, 3] and planar double-gate [4, 5] MOSFET devices have been previously studied using analytical models and *Three-Dimensional* (3-D) simulations. As expected, larger parasitic capacitance is observed at lower technology nodes and parasitic contributions increase for devices with nanowire channel configurations due to the smaller gate-to-channel capacitance contribution. These studies have, however, thus far been limited to standard MOSFET technologies.

Research for alternative technologies that allow for performance enhancement at advanced technology nodes is in high demand. A promising candidate is the *Three-Independent Gate FET* (TIGFET) device which is a Schottky-barrier-based FET with two additional gate terminals on the semiconducting channel between the metallic source and drain regions which modulate the Schottky barriers in these regions [6]. This unique device structure allows for exclusive characteristics not seen in standard MOSFET devices. In particular, these abilities include: (1) the dynamic reconfiguration of the polarity of the device (that is, the ability to choose if the channel carrier is effectively *n*-type or *p*-type) based on selective biasing of the Schottky gates [7], (2) the dynamic control of the threshold voltage (V_t) due to the dual switching mechanism of thermally-assisted tunneling through Schottky barriers or carrier transport similar to that in conventional MOSFETs [6], and (3) the dynamic control of the subthreshold slope due to a positive feedback induced by weak impact ionization [8]. While the TIGFET's independent control of its three gates allow for complex device-level operations and novel circuit-level architectures [9–15]), the trade-off is that the two additional contacted gates required for the TIGFET's functionality boost will lead to an increase in the total device capacitance in comparison to a standard one-gate CMOS device. Thus, there is a need to study the TIGFETs' device- and circuit-level capacitance in order to identify its capability at advanced technology nodes.

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In this paper, parasitic and intrinsic capacitances of a Si-NW based TIGFET device are extracted using 3-D numerical simulations and analytical models and presented using equivalent Schwarz-Christoffel transformations and standard cylindrical capacitor derivations. The capacitance components are analyzed for *Outer Fringe Capacitance* (C_{of}), *sidewall capacitance* (C_{side}), *Inner Fringe Capacitance* (C_{if}), *Overlap Capacitance* (C_{ov}), and *Channel Capacitance* (C_{ch}). The models show an exponential increase of C_{of} below the 20 nm, and that the C_{side} of a TIGFET transistor is expected to surpass the gate-to-channel capacitance below the 15 nm node. The benefits of the TIGFET devices are not seen until they are used at the circuit-level when their increased switching capabilities are shown to provide lowered *Energy-Delay Product* (EDP) even with their increased device-level parasitic capacitance. We use our device-level parasitic capacitance simulations to safely extrapolate their circuit-level effects. In particular, we show a 18% lower EDP for a fan-out of 4 and higher when using a TIGFET-based 1-bit full-adder logic circuit, thus alleviating the effects of the TIGFET's increased device-level parasitic capacitance.

The remainder of the paper is organized as follows: Section II discusses background material on TIGFETs and capacitance modeling. Section III highlights the TIGFET capacitance model and shows the results obtained from 3-D electrostatic simulations, Section IV expands these results past single devices to gate-level performance, and the paper is concluded in Section V.

II. BACKGROUND

This section provides the necessary background information to design and analyze Si-NW TIGFET technology, including the device structure, working principle, and design opportunities of the TIGFET. It also includes a brief review of analytic capacitance modeling as generally used for MOSFET devices.

A. The TIGFET as a Device

A TIGFET device is comprised of three MOS gates above a semiconductor channel that lies between metallic source and drain regions. Fig. 1 shows the structure of a SiNW TIGFET. The metal-semiconductor-metal structure creates Schottky barriers near the source and drain junctions. The MOS gates near these regions, called the *Polarity Gate at the Source* (PG_S) and the *Polarity Gate at the Drain* (PG_D), modulate the barrier's thickness in order to allow either electrons or holes to flow through the channel as the primary carriers, thus enabling device reconfigurability. The center MOS gate is called the *Control Gate* (CG) and generates a potential barrier that limits the flow of carriers, in a manner similar to a standard MOS gate. TIGFET devices have been previously fabricated with a number of geometries and channel materials including single silicon nanowire [16], multiple stacked silicon nanowire [6], silicon fin [8], *Two-Dimensional* (2-D) materials [17–19], and carbon nanotubes [20].

B. Working Principles of TIGFETs

The ability to independently control all three of a TIGFET's gates allows for distinct biasing conditions at the transistor-level. To illustrate this unique characteristic, the energy band diagram along the semiconducting channel (that is, between source and drain) is shown in Fig. 2 with the various biasing conditions. The device is in the ON-state mode when PG_S ,

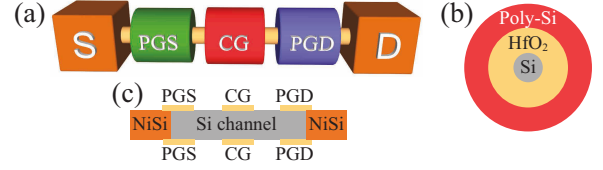


Fig. 1: (a) Sketch of a Si-NW-based TIGFET topology with (b) a vertical cut along the CG region, and (c) a horizontal cut along the channel.

CG , and PG_D are set high – allowing electrons to travel through the channel as majority carriers, as shown in Fig. 2-a. The device will turn OFF when the potential at CG lowers so that the majority carriers cannot pass through the center potential barrier, as shown in Fig. 2-b. The device can alternately be turned OFF by lowering the potential at PG_S , thus restricting the majority carriers tunneling through the Schottky barrier at the source side as shown in Fig. 2-c. Since the probability of tunneling through the Schottky barrier at the source side is lower than the probability of thermionic emission over a potential barrier at the CG region, the latter biasing condition allows for a low-leakage OFF-state operation mode. The bias conditions can also enable holes to become majority carriers, as shown in Fig. 2 (d-f), when PG_S and PG_D are set low.

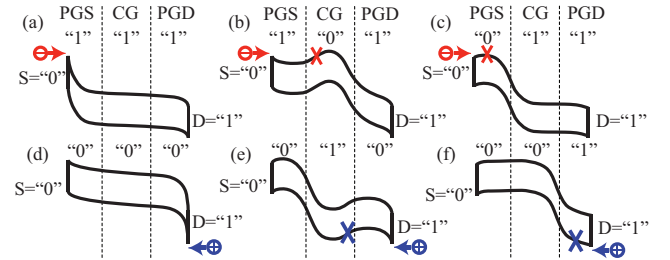


Fig. 2: Band diagrams of a TIGFET device under different bias conditions. *n*-FET in the (a) ON-state and (b) OFF-state, and (c) low-leakage OFF-state. *p*-FET in the (a) ON-state and (b) OFF-state, and (c) low-leakage OFF-state. Notation: “0” = G_{ND} and “1” = V_{DD} .

Fig. 3 shows a comparison between measured results and Synopsys Sentaurus TCAD simulations of the drain current-control gate voltage operation of TIGFET devices [7].

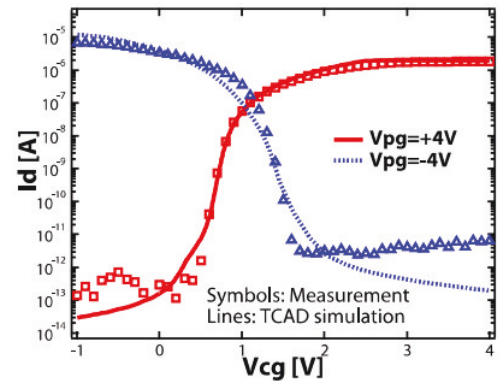


Fig. 3: I_D - V_{CG} of measured and simulated TIGFET devices as reported in [7] which show the reconfigurability of the device.

C. Logic Design Opportunities Offered by the TIGFET

The real benefit to using the functionality-enhanced TIGFET devices is at the gate-level. These benefits have been investigated in literature [9–15] and include the use of TIGFETs in circuit implementations of a dual- V_T inverter, dual- V_T NAND, 4-1 static multiplexer, 6T static random-access memory, true single phase clocking flip-flop, multiplexer, and power-gated differential cascade voltage switch logic. Of particular interest is the fact that a three-input XOR gate and a three-input MAJ gate can be realized using four TIGFET transistors (plus two and three inverters, respectively). These gate implementations are shown in Fig. 4 (b-c), along with the symbol representation of the device in Fig. 4-a. These circuit opportunities are only possible due to the polarity control characteristic of TIGFET technology that allows for higher-level circuit architecture to be designed [15].

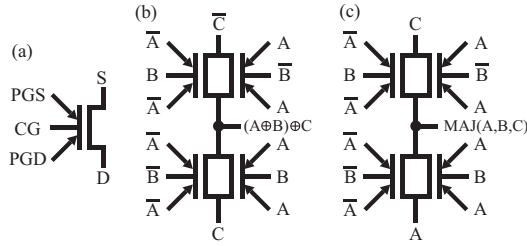


Fig. 4: (a) Symbol representation of a TIGFET device, (b) a three-input TIGFET XOR gate, and (c) a three-input TIGFET MAJ gate.

D. MOSFET Analytical Capacitance Modeling

The parasitic capacitance of a standard MOSFET is no longer negligible and, in fact, dominates over the intrinsic capacitance below the 20 nm node [1]. Due to aggressive scaling trends, the increase in the total capacitance of a device may severely limit circuit-level performances if changes are not proposed. The heightened attention to the parasitic contribution of a MOSFET has led to multiple literature investigations, such as those proposed in [2, 4, 5, 21]. These papers model the various parasitic capacitances using multiple extraction techniques and observed similar results in terms of the increasing capacitance trends in scaled devices.

The parasitic capacitance extraction of transistors in this work is based on the work from [2]. The multiple capacitance contributions of the nanowire-based MOSFET are shown in Fig. 5-a. In this device, the channel region (length L_g and radius r) is fabricated between highly doped source and drain regions (extension length L_{sp} and contact length L_s and L_d for source and drain respectively). The MOS gate contact is placed above the channel with an overlap length of L_{ov} . The metal height H_g is used for all three gates.

III. THE TIGFET CAPACITANCE MODEL

To better understand TIGFETs' technological capabilities, their parasitic and intrinsic capacitances must be extracted. First, we develop the analytical models to solve for the various capacitances of a TIGFET transistor by applying techniques such as the equivalent Schwarz-Christoffel transformation and standard cylindrical capacitors. Second, we use *COMSOL Multiphysics* to validate our model by performing 3-D Poisson electrostatic simulations on a silicon nanowire-based TIGFET

device. In order to establish a baseline comparison, the results obtained from simulations are compared with a CMOS counterpart with similar dimensions and materials.

A. TIGFET-Specific Assumptions

First we examine the structure of a Si-NW-based TIGFET device as shown in Fig. 5. The TIGFET device is similar to the MOSFET device with the exception of two additional MOS contacted gates between the source and drain extensions. Note that there are two overlapping regions between PG_S and the source and between PG_D and the drain. Also the length between the MOS gates, L_{cp} , becomes a distinct length that is fabrication dependent. In this work, the length of the three MOS gates, L_g , and the length between the face-to-face sidewalls between PG_S and the source or PG_D and the drain, L_{sp} , are the same as in the CMOS counterpart.

The effect of a dynamic variation in the gate voltage is not taken into consideration in our simulations and thus is not used to model the transient response of TIGFETs. The simulations performed in this work consider abrupt interfaces between the source extension and channel junctions as is expected due to the nature of the metal-to-semiconductor Schottky junctions where a doping density profile is not needed. However, we do take into consideration that the inner-fringe capacitance is non-existent in the ON-state mode (strong inversion) while the intrinsic capacitance is removed in the OFF-state mode (cutoff mode).

B. The Analytical Expressions

The two additional contacted gates of a TIGFET device lead to additional interactions between the metallic electrodes. This allows for various new capacitance components to be added as shown in Fig. 5-b. The outer fringe capacitance, C_{of} , contains the source-to- PG_S face-to-face and face-to-extension region capacitance C_{of_SPGS} , and the CG -to- PG_S face-to-face capacitance C_{of_CGPG} . The fringe capacitance, C_{if} , contains four total components resulting from the interactions between (1) source and PG_S (C_{if_SPGS}), (2) source and CG (C_{if_SCG}), (3) source and PG_D (C_{if_SPGD}), and (4) CG and PG_D (C_{if_CGPGD}). Lastly, the sidewall capacitance, C_{side} , contains five total components coming from the interactions between (1) source and PG_S (C_{side_SPGS}), (2) source and CG (C_{side_SCG}), (3) source and PG_D (C_{side_SPGD}), (4) PG_S and PG_D (C_{side_PGPG}), and (5) CG and PG_S (C_{side_CGPG}). The intrinsic capacitance, C_{ch} , also increases for a TIGFET device since it now contains the intrinsic capacitance at CG (C_{ch_CG}) and at the polarity gates ($2 \times C_{ch_PG}$).

1) C_{of} : The outer fringe capacitance of a TIGFET device contains the metallic interactions including the face-to-face and face-to-extension regions occurring above the channel region. To simplify the capacitance extraction, the C_{of_SPGS} term is split into two separate components: the capacitance between the face-to-face sidewalls of the gate electrodes (C_{of_gsd}) and the capacitance between the gate electrode and the S-D extension regions (C_{of_geax}), as shown in Fig. 5-b. The C_{of_gsd} component is approximately calculated as follows. Since the oxide layer in our simulations uses a high κ dielectric (HfO_2), the equivalent oxide thickness is high relative to the metal height (H_g) and the non-overlapping fringing fields must be taken into account. The metal height is the length

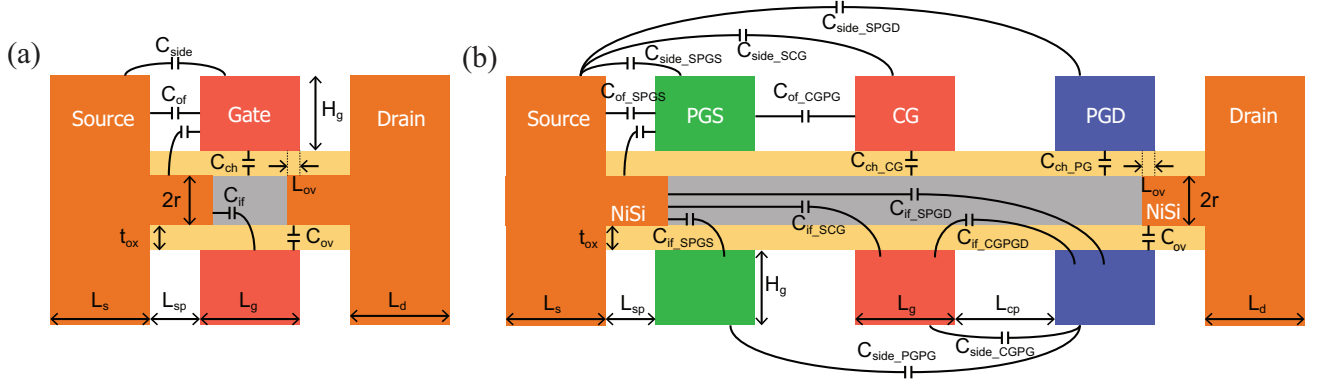


Fig. 5: 2-D cross-sectional view of a nanowire-based (a) MOSFET [2] and (b) TIGFET device with key length parameters and capacitances.

of the contact metal that extends above the channel oxide. A fitting parameter ($M = 1.02$) is added to best match with the theoretical results coming from our *COMSOL* simulations shown later.

$$C_{of_gsd} = M \frac{\epsilon_{ox}(2A_1A_2)}{(A_1 + A_2)L_{sp}}, \quad (1)$$

where

$$A_1 = (2W_g + 2r + 2t_{ox})^2 - \pi(r + t_{ox})^2, \quad (2)$$

$$A_2 = (2W_g + 2r + 2t_{ox})^2 - \pi(r)^2. \quad (3)$$

A_1 and A_2 are the areas of the parallel plates at PG_S and the source, respectively. ϵ_{ox} is the permittivity of the channel oxide, t_{ox} is the thickness of the channel oxide, and W_g is the width of the metallic gates (assumed to be the metal height H_g). The parasitic capacitance between the PG_S (or PG_D) gate and the source (or drain) extension region (C_{of_ge}) for a TIGFET transistor is the same as for the MOSFET device as shown in [2]. The use of high- κ dielectrics does not create additional fringing fields to be accounted for and thus the following analytical expression will match well with *COMSOL* simulations as shown later.

$$C_{of_ge} = 4\epsilon_{ox}\eta \left(L_{sp} - t_{ox} + r \ln \left(\frac{L_{sp}}{t_{ox}} \right) \right) \cdot \sqrt{\frac{2r}{L_{sp} + 2r + t_{ox}}}, \quad (4)$$

where

$$\eta = \epsilon_{ox} \sqrt{\frac{2\pi r \left(\sqrt{H_g^2 + W_g^2} - r - t_{ox} \right)}{|4H_gW_g - \pi(r + t_{ox})^2|}}. \quad (5)$$

The capacitance between the PG_S electrode and the source electrode is calculated as follows:

$$C_{of_SPGS} = C_{of_gsd} + C_{of_ge}. \quad (6)$$

The parasitic capacitance between the face-to-face electrodes CG and PG_S (C_{of_CGPG}) is calculated by taking the area of the overlapping plates into consideration:

$$C_{of_CGPG} = \epsilon_{sp} \frac{(2H_g + 2r + 2t_{ox})^2 - \pi(r + t_{ox})^2}{L_{sp}} \quad (7)$$

where ϵ_{sp} is the permittivity of the spacer and t_{ox} is the thickness of the channel oxide.

2) C_{side} : The sidewall capacitance takes into consideration the electrostatic interactions between the gates at the outer sides of the contacts. The analytical expressions of these capacitances are best derived by using the Schwarz-Christoffel transformation. This technique transforms two planar conductors (fields from the upper half-plane) into a Schwarz-Christoffel rectangular region as shown in Fig. 6(b-c).

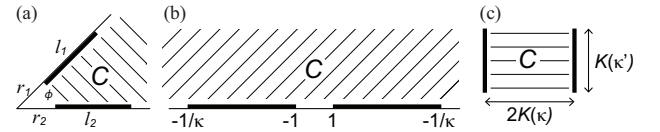


Fig. 6: Geometries to transform (a) two non-parallel plates with unequal lengths and (b) two co-planar plates with equal lengths onto a (c) Schwarz-Christoffel region with two parallel plates.

The capacitance between the two parallel plates in Fig. 6-c can then be calculated:

$$C = W \frac{\epsilon_{ox}K(\kappa')}{2K(\kappa)} \quad (8)$$

where W is the width of the plates, $K(\kappa)$ is the complete elliptic integral, and κ and κ' are the moduli (related by $\kappa^2 + \kappa'^2 = 1$). The expression of $K(\kappa')/K(\kappa)$ is best described in [22] with the least relative error:

$$\frac{K(\kappa')}{K(\kappa)} = \frac{1}{2\pi} \ln \left(2 \frac{\sqrt{1+\kappa'} + \sqrt[4]{4\kappa'}}{\sqrt{1+\kappa'} - \sqrt[4]{4\kappa'}} \right) \quad (9)$$

The different interactions between the sidewalls of a TIGFET transistor include (1) source and PG_S (C_{side_SPGS}), (2) source and CG (C_{side_SCG}), (3) source and PGD (C_{side_SPGD}), (4) PG_S and PGD (C_{side_PGPG}), and (5) CG and PGS (C_{side_CGPG}). Following the Schwarz-Christoffel transformation technique, these capacitance components can be calculated by setting $W = 2H_g + 2t_{ox} + 2r$ and determining the κ values for each case, as follows:

$$\kappa_{side_SPGS} = \frac{L_{cp}}{2L_g + L_{cp}} \quad (10)$$

$$\kappa_{side_SCG} = \frac{L_g + L_{sp} + L_{cp}}{L_g + L_{sp} + L_{cp} + 2L_g} \quad (11)$$

$$\kappa_{side_SPGD} = \frac{L_{cp} + L_g + L_{sp} + L_g + L_{sp}}{L_{cp} + L_g + L_{sp} + L_g + L_{sp} + 2L_g} \quad (12)$$

$$\kappa_{side_CGPG} = \frac{L_{sp}}{2L_g + L_{sp}} \quad (13)$$

$$\kappa_{side_PGPG} = \frac{L_g + 2L_{sp}}{L_g + 2L_{sp} + 2L_g} \quad (14)$$

3) C_{if} : The inner fringe capacitance comes from the overlap interaction between the inner surface of the PG_S , CG , and PG_D electrode and the extension region at source (C_{if_SPGS} , C_{if_SCG} , and C_{if_SPGD} , respectively) as shown in Fig. 5-b. The inner fringe capacitance between the inner surface of the CG and PG_D electrodes, C_{if_CGPGD} , is considered to be negligible due to the strong inversion at the CG . While there exists literature that calculates the inner fringe capacitance of the interaction between source and PG_S [2, 4], there is as of yet no technique for calculating the capacitance between source and CG or source and PG_D . For the latter two capacitance components, an approximation is made to best match realistic *COMSOL* simulations.

We start of by using the Schwarz-Christoffel transformation of two unequal plates at an angle ϕ (with lengths l_1 and l_2 and placed at r_1 and r_2 respectively away from the origin) onto a Schwarz-Christoffel region composed of two parallel plates as shown in Fig. 6(a-c). In this transformation, the κ values can be determined using the following expression [23]

$$\kappa = \sqrt{\frac{2(\beta - \alpha)}{(1 - \alpha)(1 + \beta)}} \quad (15)$$

where

$$\alpha = \frac{-2r_1^{\pi/\phi} + (r_1 + l_1)^{\pi/\phi} - (r_2 + l_2)^{\pi/\phi}}{(r_1 + l_1)^{\pi/\phi} + (r_2 + l_2)^{\pi/\phi}}, \quad (16)$$

$$\beta = \frac{2r_1^{\pi/\phi} + (r_1 + l_1)^{\pi/\phi} - (r_2 + l_2)^{\pi/\phi}}{(r_1 + l_1)^{\pi/\phi} + (r_2 + l_2)^{\pi/\phi}}. \quad (17)$$

By following equation (8) and (9), the inner fringe capacitance components of a TIGFET transistor can be derived using the following geometry parameters:

$$\phi = \pi/2, \quad l_1 = 2r, \quad l_2 = L_g, \quad r_1 = t_{ox}, \quad W = 2\pi r. \quad (18)$$

The geometry parameter r_2 is dependent on the MOS gate that is selected: $r_2 = 0$ for C_{if_SPGS} , $r_2 = L_g + L_{sp}$ for C_{if_SCG} , and $r_2 = 2L_g + 2L_{sp}$ for C_{if_SPGD} . Fitting parameters were added for all three inner fringe capacitance components to best match with the *COMSOL* simulations: $\times 1.07$ for C_{if_SPGS} , $\times 0.85$ for C_{if_SCG} , $\times 0.70$ for C_{if_SPGD} .

4) C_{ov} : The overlap capacitance of a nanowire-based transistor is calculated by using the capacitance of a standard cylindrical capacitor. For the case of a TIGFET transistor, these interactions occur when the source (or drain) extension region overlaps with the PG_S (or PG_D) electrode. The length L_{ov} is assumed to be similar to the nanowire-based MOSFET equivalent device [2].

$$C_{ov} = \frac{2\pi\epsilon_{ox}L_{ov}}{\ln\left(\frac{t_{ox}+r}{r}\right)} \quad (19)$$

5) C_{ch} : The gate-to-channel capacitance of the TIGFET transistor is similarly calculated, except that instead of one as per a standard CMOS transistor, three MOS gates must be taken into account. The overlap lengths at the PG_S and PG_D regions are subtracted.

$$C_{ch} = \frac{2\pi\epsilon_{ox}(3L_g - 2L_{ov})}{\ln\left(\frac{t_{ox}+r}{r}\right)} \quad (20)$$

C. Capacitance Extraction

In this work, *COMSOL Multiphysics* is used to verify the accuracy of the parasitic and intrinsic capacitances of a TIGFET device. In particular, we model each capacitance component separately by solving 3-D electrostatic numerical simulations based on 3-D Poisson equations using the AC/DC module. This simulator solves Laplace's equation for the electric potential using the scalar electric potential as the dependent variable and is valid for sub-10 nm simulations. We use cumulative geometric sections with the electrostatics potential solved for in the air and non-metallic regions. The infinite element domain used for the mesh is spherical and discretization is quadratic. Note that L_{cp} is set to 15 nm and H_g to 10 nm in these simulations.

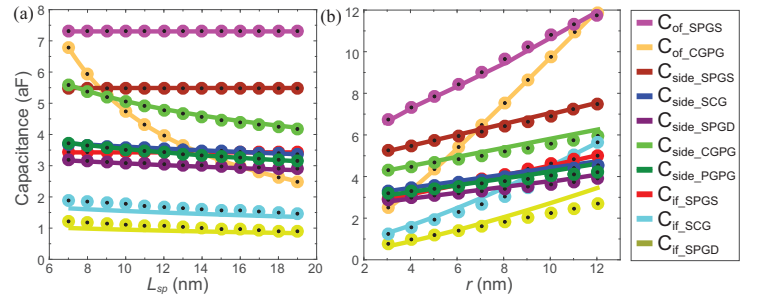


Fig. 7: (a) Spacer length (L_{sp}) sweep and (b) radius (r) sweep showing the various parasitic and intrinsic capacitance components. Solid lines come from analytical equations while the black dots come from *COMSOL* simulations.

As seen in Fig. 7, we have shown excellent agreement between the analytical expressions and the electrostatic numerical simulations for the overlap capacitance (C_{ov}), all outer fringe capacitances C_{if} , all sidewall capacitances C_{side} , and the inner fringe capacitance between source and PG_S C_{if_SPGS} while the variables L_{sp} and r are swept. These length-to-capacitance curves give a more fruitful explanation on how some variables affect the capacitance values. This is beneficial since some of the analytical relationships are not straightforward. The L_{sp} sweep as shown in Fig. 7-a has a small effect on most capacitances (with a tendency to increase when L_{sp} is reduced) except for C_{of_CGPG} and C_{side_CGPG} . As expected, there is an inverse relationship between L_{sp} and C_{of_CGPG} as shown in equation (7) and this accounts for the high rate of change for C_{of_CGPG} . Such a direct relationship with L_{sp} is non-existent in the other capacitance calculations. On the other hand, C_{side_CGPG} shows a linear tendency in this L_{sp} sweep. However, C_{side_CGPG} is expected to exponentially increase as L_{sp} approaches zero.

Meanwhile, as r is decreased in Fig. 7-b, all capacitance values are decreased. As the radius is decreased, all electrodes are decreased and this leads to a tendency to increase all capacitances. We note that C_{of_CGPG} is affected the most by the radius of the nanowire; this is because, as shown in equation (7), there are two quadratics in the numerator involving the radius. This will result in the radius contributing factors of: $(4 - \pi) \cdot r^2$, $8 \cdot H_g \cdot r$, and $(8 - 2\pi) \cdot r \cdot t_{ox}$. The radius is thus expected to grow very quickly compared to the other capacitances which do not contain any quadratic radius diameter elements. As the radius is swept between 4 nm and 5 nm, the analytical expression of C_{of_SPGS} exponentially increases due to the undefined point ($H_g W_g = \pi(r + t_{ox})^2$) as expressed in η in equation (5). Since realistic *COMSOL* simulations expect a linear increase around this point, the domain of validity was improved by fitting a linear curve.

The inner fringe capacitance between source and CG (C_{if_SCG}) has an analytical expression that has a maximum error of 16% while sweeping both L_{sp} and r . The source and PG_D (C_{if_SPGS}) inner fringe capacitance has an analytical expression that has a maximum error of 19% when sweeping L_{sp} and 20% when sweeping r . These differences are mostly a result of using the Schwarz-Christoffel transformation that takes into consideration the fringing fields. A more thorough examination of these inner fringe capacitances can be done. However, we believe that our derivations show an adequate representation of the variable sweeps and does not affect the intent of this paper which is to study the effects of having two additional MOS gates and to analyze the limitations of scaling TIGFET transistors.

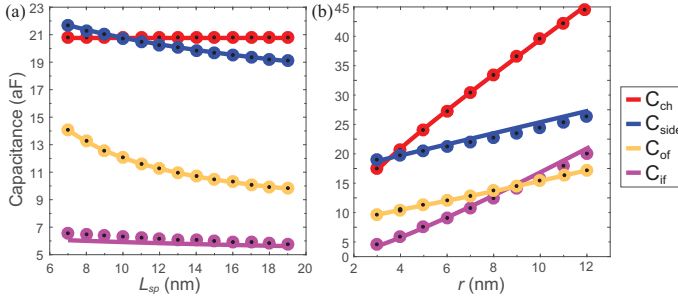


Fig. 8: (a) Spacer length (L_{sp}) sweep and (b) radius (r) sweep showing the combined parasitic and intrinsic capacitances. Solid lines come from analytical equations while the black dots come from *COMSOL* simulations.

The various capacitance contributions are grouped together in Fig. 8 to show the relationships between C_{side} , C_{of} , C_{if} , and gate-to-channel capacitance C_{ch} . The spacer length is swept in Fig. 8-a while the radius is swept in Fig. 8-b. The analytical expressions are identified by black dots and the *COMSOL* simulations are identified by solid lines. As shown in Fig. 8-a, the C_{of} has an inverse relationship with L_{sp} , C_{side} has a linear relationship with L_{sp} , and C_{if} has the smallest percentage contribution to the total capacitance. Meanwhile, in Fig. 8-b, it is clear that C_{of} has the lowest percent change. Note that the analytical expression of C_{of} contains a fitting linear curve between $r = 4$ nm and $r = 5$ nm due to the undefined point which exists in η in equation (5).

As shown in both subfigures, the capacitance of the intrinsic capacitance is larger than the parasitic capacitances except

when L_{sp} decreases past 10 nm or when r decreases past 4 nm.

We expect the sidewall and inner fringe capacitances between the source and CG to be unaffected by the additional PG_S and PG_D of the TIGFET; thus, we consider these values in equivalent CMOS simulations for comparison. First, [2] Fig. 6-f contains inner fringe capacitance results between the source and gate for a similar-dimension MOSFET device simulation which are in the same atto-Farad range as our simulations. Similarly illustrated in [24] Fig. 3, the sidewall capacitance in this study is also within a few atto-Farad range of our simulation. We can therefore safely conclude from these comparisons that our simulation results are probable when fitted against realistic data.

IV. GATE-LEVEL IMPACT STUDY

The two additional MOS contacted gates in a TIGFET device increase the total parasitic capacitance compared to a MOSFET counterpart. However, the designs of integrated circuits with TIGFET devices, as depicted in Fig. 4, are implemented by switching either zero, one, two, or three contacted gates at each clock cycle. The number of switching electrodes leads to different parasitic capacitances and must be taken into consideration when designing circuit-level opportunities. *COMSOL* simulations were performed to estimate the total capacitance contribution per switching mode.

A. Modes of Operation

The four possible switching scenarios of a TIGFET device with their corresponding parasitic capacitance contributions (C_{ch} , C_{ov} , C_{of} , C_{if} , C_{side}) are shown in Fig. 9. The nanowire-based MOSFET device is added for a proper baseline comparison. The TIGFET transistor under the Mode A operation is chosen to represent all three MOS gates set to a constant value. This leads to a zero channel parasitic capacitance contribution and a small component of C_{of} and C_{side} since there are no switching mechanisms required between the three MOS gates. This mode, encountered primarily in the architecture of a 32-bit adder, leads to a $0.61\times$ reduction of parasitic capacitance when compared with the CMOS HP device – predominantly due to the removal of the C_{ch} contribution. Mode B represents the switching of one MOS electrode and results in $1.07\times$ larger parasitic capacitance compared to the CMOS HP device. The parasitic capacitance now includes C_{ch} from the MOS gate, a smaller C_{if} component, when compared to Mode A, since C_{if_SCG} is smaller than C_{if_SPGS} , and a larger C_{of} , when compared to Mode A, since $2 \times C_{of_CGPG} > C_{of_SPGS}$. This mode is used in the pull-up and pull-down networks of an inverter. Mode C contains two switching MOS gates and its parasitic capacitance is shown to be $1.59\times$ larger when compared with the CMOS HP device. This configuration is encountered in the pull-down network of a two-input NAND. Finally, Mode D represents all three MOS electrodes switching with two varying voltages. This configuration is seen in the three-input XOR and three-input MAJ gates that are used in this paper and the TIGFET devices operated in this manner result in $2.01\times$ larger parasitic capacitance than for standard CMOS HP devices.

The distance between MOS gates, L_{cp} , is set to 15 nm and 10 nm and its affect on the parasitic capacitance is shown in Fig. 9. A decrease in L_{cp} predominantly increases C_{of} due

to its inverse effect on C_{of_CGPG} . However, L_{cp} 's largest contribution to the total parasitic capacitance (Mode B) only leads to a 7.5% increase between $L_{cp} = 10$ nm and $L_{cp} = 15$ nm. This is noteworthy because it shows good scaling potential for TIGFET devices.

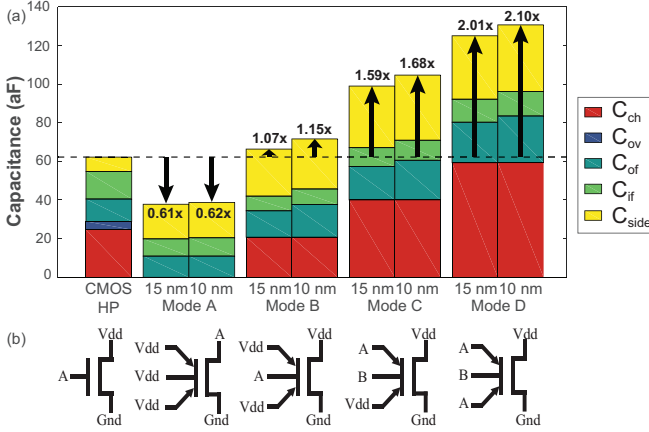


Fig. 9: (a) Intrinsic and parasitic capacitance contributions for the TIGFET device using the multiple modes of operation while L_{cp} parameter is set to 15 nm and 10 nm. The CMOS HP device at the 15 nm technology node is added for comparison, and (b) the respective symbol representations for the different modes of operation.

B. Gate-Level Performance Setup

Now that we have a clear understanding of the operation mode contribution, we consider the actual gate-level performance of TIGFET devices to provide a fair comparison to their CMOS HP counterparts. In particular, we consider the *Energy Delay Product* (EDP) of the gate as a good figure-of-merit.

We start by considering the standard theoretical equations for delay ($t_{int,mode}$) and energy ($E_{int,mode}$) for a single TIGFET transistor as a function of its operation mode. This is based on work seen in [25] and is related to the intrinsic capacitance caused by a single device:

$$t_{int,mode} = \frac{C_{tot,mode} \cdot V_{DD}}{I_{on}}, \quad (21)$$

$$E_{int,mode} = C_{tot,mode} \cdot V_{DD}^2. \quad (22)$$

Recall that the total capacitance of a TIGFET is dependent on the mode of operation, that is to say: how many gates are being switched at once. In this work, we normalize the TIGFET capacitances per mode to the capacitances of a standard CMOS HP device. As seen in Fig. 9, for an L_{cp} of 15 nm, these are as follows: $C_{tot,CMOSHP} = 1$, $C_{tot,modeA} = 0.61$, $C_{tot,modeB} = 1.07$, $C_{tot,modeC} = 1.59$, and $C_{tot,modeD} = 2.01$.

Also of importance for gate-level analysis is the capacitance of the connecting wires. The expressions of delay t_{ic} and energy E_{ic} of a typical length interconnect are taken from [25] to be approximated as follows:

$$t_{ic} = 0.7 \frac{C_{ic} \cdot V_{DD}}{I_{ON}}, \quad (23)$$

$$E_{ic} = 0.5 C_{ic} \cdot V_{DD}^2. \quad (24)$$

where C_{ic} , the capacitance of a wire per length of interconnect, is estimated as five times the pitch [25].

The three fundamental logic gates used for comparison in this work are the inverter, 3-input XOR, and 1-bit full adder. The delay t_{gate} and energy E_{gate} (where the subscript gate is the logic circuit of interest) of each of these are as follow based on the work in [25]:

$$t_{inv1} = 2M_{tinv}t_{int,(b)} + t_{ic}L_{inv} \quad (25)$$

$$E_{inv1} = 2M_{Einv}E_{int,(b)} + E_{ic}L_{inv} \quad (26)$$

$$t_{3XOR} = 2M_{t3XOR}t_{int,(d)} + t_{ic}L_T + t_{inv1} \quad (27)$$

$$E_{3XOR} = \alpha_{3XOR}(M_{ET}E_{int,(d)} + E_{ic}L_T + 3E_{inv1}) \quad (28)$$

$$t_{1bit} = t_{T,(d)} + t_{inv1} + t_{ic}L_{1bit} \quad (29)$$

$$E_{1bit} = \alpha_{3XOR}E_{T,d} + \alpha_{maj3}E_{T,d} + 3E_{inv1}/2 \quad (30)$$

$$+ 2E_{ic}L_{1bit} \quad (31)$$

where the M_{tgate} and M_{Egate} adjustment factors are taken from SPICE simulations using the Arizona compact predictive technology pack [25, 26], the length factor L_{gate} is defined as:

$$L_{gate} = \max(1, \frac{\sqrt{A_{gate}}}{L_{ic}}), \quad (32)$$

which corrects the energy and delay for the interconnect contribution based on the width of the logic circuit in relation to the typical length of an interconnect.

The 1-bit full adder is designed using one XOR gate and one MAJ gate. An activity factor α is calculated to be 3/16 and 1/4 for the 3-input XOR and 3-input MAJ gates respectively. This factor is used to estimate the energy component and is explained further in [27, 28].

C. Fan-out Study for Gate-Level Performance Analysis

Finally, we put all of these separate parts together for a thorough analysis of gate-performance. We do this by considering the area effects of various TIGFET-based and equivalent CMOS HP-based circuits at the 15 nm technology mode. The fan-out-of- n refers to the number of gate inputs driven by one output of a logic gate. It is an optimal way to see the impact of the added gates of the TIGFET device on the gate-level capacitance because increasing the number of inputs, n , increases the capacitive load on the driving gate.

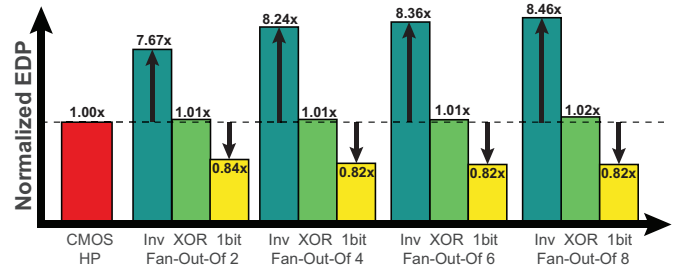


Fig. 10: Normalized EDP versus Fan-out-of- n for the inverter, 3-input XOR, and 1-bit Full Adder at the 15 nm technology node. The CMOS HP device is normalized for each logic gate.

Fig. 10 shows the EDP of a TIGFET-based inverter, 3-input XOR, and 1-bit full adder normalized to CMOS HP device logic as a function of the fan-out. From this figure, we see that the TIGFET-based inverter has a $7.67\times$ higher EDP for a fan-out-of-2 than standard CMOS HP-based circuits, and this increases to $8.46\times$ higher EDP for a fan-out-of-8. A higher

EDP for a TIGFET-based inverter is expected due to the added MOS gates on the single TIGFET device.

However, as discussed in Section II-C, TIGFETs have enhanced switching characteristics due to their polarity control that require fewer TIGFET transistors to realize complex logic gates compared to CMOS. This means that even though the individual TIGFET transistors have larger capacitances on average per device than a CMOS device, a TIGFET-based logic gate can have lower overall capacitance than an equivalent CMOS gate. This is illustrated by the TIGFET-based 3-input XOR logic that has approximately the same EDP as CMOS HP-based 3-input XOR logic consistently with increasing fan-out gates. Indeed, though the individual TIGFETs in a 3-input XOR are operated in Mode D and therefore come with a $2.01 \times$ capacitance increase per device, the TIGFET-based 3-input XOR requires only half the number of transistors required by a CMOS-based 3-input XOR. Thus, the drawbacks of the higher per-device parasitic capacitance is canceled out by the benefit of fewer transistors in the TIGFET-based design.

A 1-bit full adder further compounds the number of transistors in the TIGFET-based design compared to the CMOS design. In this case, the benefits of having fewer transistors outweighs the larger per-device parasitic capacitance, as seen in Fig. 10: the EDP is approximately 18% lower when using TIGFET-based 1-bit full adder logic for fan-out-of-4 and higher. This conclusively shows that TIGFET-based circuits are in fact competitive with standard CMOS HP technology at the same node.

V. CONCLUSION

This paper provides a deep analysis of the capacitance contributions of the TIGFET device and compares it to a standard CMOS device at the equivalent node. It then takes this analysis a step further and considers the capacitances of logic gates comprised of TIGFET-based or CMOS-based device systems. This work is of significant consequence due to the severity of the impact of parasitic capacitance on circuit-level performance, especially at advanced nodes, which had the potential to eliminate TIGFET technology as a viable alternative device at sub-20 nm nodes.

TIGFET devices have the ability for more compact circuit designs due to their increased switching capabilities. The number of gates being switched at each clock cycle leads to different parasitic capacitances: when all three MOS gates of a TIGFET are set to a constant value there is zero channel parasitic capacitance and this results in a 39% reduction in parasitic capacitance compared to a standard CMOS device. Meanwhile, when all three MOS electrodes are switching with two varying voltages, we see a $2.01 \times$ increase in the parasitic capacitance compared to CMOS. Despite potentially higher per-device parasitic capacitance, TIGFET-based designs are shown to have lower EDP at the gate-level if used in compact logic designs. For example, the EDP for a TIGFET-based 1-bit full adder for a fan-out-of-4 and higher is approximately 18% lower due to the TIGFET design requiring only half the number of transistors compared to the equivalent CMOS design.

This work serves to validate the continued study of not only TIGFET devices but all functionality-enhanced alternative devices which may appear at first glance to introduce more device-level parasitics.

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