Applied Physics Letters

Characterization of MOCVD-grown AlSiO gate dielectric on β-Ga_2O_3 (001)

Cite as: Appl. Phys. Lett. **118**, 172102 (2021); https://doi.org/10.1063/5.0048990
Submitted: 28 February 2021 • Accepted: 13 April 2021 • Published Online: 26 April 2021

Zhe (Ashley) Jian, Islam Sayed, Wenjian Liu, et al.

Applied Physics Letters ARTICLE scitation.org/journal/apl

Characterization of MOCVD-grown AlSiO gate dielectric on β-Ga_2O_3 (001)

Cite as: Appl. Phys. Lett. **118**, 172102 (2021); doi: 10.1063/5.0048990
Submitted: 28 February 2021 · Accepted: 13 April 2021 ·
Published Online: 26 April 2021

View Online Export Citation CrossMark

Zhe (Ashley) Jian,[1,a)] Islam Sayed,[2] Wenjian Liu,[2] Subhajit Mohanty,[1] and Elaheh Ahmadi[1,3]

AFFILIATIONS

[1]Department of Electrical and Computer Engineering, University of Michigan, Ann Arbor, Michigan 48109, USA
[2]Department of Electrical and Computer Engineering, University of California, Santa Barbara, Santa Barbara, California 93106, USA
[3]Applied Physics Program, University of Michigan, Ann Arbor, Michigan 48109, USA

[a)]Author to whom correspondence should be addressed: jianzhe@umich.edu

ABSTRACT

The interface and bulk properties of aluminum-silicon-oxide (AlSiO) dielectric grown by metal-organic chemical vapor deposition (MOCVD) on (001) β-Ga_2O_3 were investigated systematically using a deep UV-assisted capacitance–voltage methodology. The improved surface preparation with a combination of UV-ozone and wet chemical treatment reduced near-interface traps resulting in a negligible hysteresis. An average interface state density of $6.63 \times 10^{11}\,cm^{-2}eV^{-1}$ and AlSiO bulk trap density of $4.65 \times 10^{17}\,cm^{-3}eV^{-1}$ were quantified, which is half of that for Al_2O_3 deposited by atomic layer deposition (ALD). A net positive interface fixed charge of $1.56 \times 10^{12}\,cm^{-2}$ was measured. In addition, a high dielectric breakdown field of ~7.8 MV/cm and more effective suppression of gate leakage were achieved on these devices compared with ALD-Al_2O_3 on similar metal-oxide-semiconductor (MOS) structures.

The β-Ga_2O_3 has become a promising semiconductor for high-power applications due to its ultra-wide bandgap (4.9 eV), large Baliga's figure of merit, and availability of melt growth techniques.[1–6] These superior physical properties have led to great advancements on various Ga_2O_3-based devices, including Schottky barrier diodes (SBDs),[7–9] field-effect transistors (FETs),[3,10] metal-oxide-semiconductor FETs (MOSFETs),[11–13] and modulation-doped FETs (MODFETs).[14–16] A β-Ga_2O_3 MOSFET with a record breakdown voltage (BV) over 2.6 kV was demonstrated leading to a Baliga's figure-of-merit of 280 MW/cm^2.[17]

High-quality dielectrics are crucial for enabling high-performance β-Ga_2O_3 FETs especially because achieving p-type doping does not seem feasible for this material system. The material properties of high-quality gate dielectric include high dielectric constant, negligible gate leakage, low density of interface and bulk traps, and large breakdown field. In particular, given the ultra-wide bandgap of Ga_2O_3 of 4.9 eV, there are a relatively limited number of available gate dielectrics to achieve conduction band offsets $\geq$1 eV favored for MOS structures. Currently, Al_2O_3, SiO_2, HfO_2, and their alloys or bilayer combinations are being extensively investigated in metal-oxide-semiconductor capacitors (MOSCAPs) and exploited for Ga_2O_3-based MOSFETs.[17–21] A few studies on novel dielectrics for β-Ga_2O_3 such as ZrO_2, $LaAl_2O_3$, and $(Y_{0.6}Sc_{0.4})_2O_3$ films have been also reported, with each having different advantages over the others.[22–24] Further investigations on developing high-quality dielectric are still needed to improve the gate robustness of Ga_2O_3-based FETs to take advantage of its full potential.

Recently, aluminum silicon oxide (AlSiO) has been proposed as a high-performance and reliable gate dielectric for GaN-based devices.[25–27] Previous studies showed that the alloying of Al_2O_3 with silicon to form AlSiO has the potential to combine the merits of both SiO_2 ($E_g = 9.0$ eV) and Al_2O_3 ($E_g = 6.7$ eV), thus realizing low density of interface traps (D_{it}), high conduction/valence band offset, and high breakdown strength.[26,28] Chan *et al.* reported that AlSiO with a silicon composition up to 25% grown on Ga-polar GaN by metal-organic chemical vapor deposition (MOCVD) demonstrated a lower D_{it} and enhanced reliability compared to Al_2O_3.[25,29] Sayed *et al.* studied the impact of GaN polarity and the effect of varying the Si compositions in AlSiO dielectric on the electrical properties of MOS devices.[28,30] Liu *et al.* developed a systematic methodology to analyze the interfacial and bulk qualities of AlSiO on N-polar GaN using capacitance–voltage (C–V) methods, and showed a low D_{it} value of $4.4 \times 10^{11}\,cm^{-2}eV^{-1}$.[31,32] The same group also demonstrated that the post-metallization annealing of AlSiO/GaN MOSCAPs improved operation stability, reduced near-interface traps, and improved the low-leakage operation range under forward bias from 0–2.6 MV/cm to 0–4 MV/cm.[33] The

promising results of AlSiO as a dielectric for GaN-based devices motivated us to expand its applications to Ga_2O_3.

In this Letter, the electrical properties of AlSiO/β-Ga_2O_3 (001) MOSCAPs were studied. Fixed interface charges and near-interface electron traps were quantified on samples treated with and without UV-ozone using C–V methods. The D_{it} was extracted accurately by accounting for dielectric bulk traps employing deep UV-assisted C–V method and physical models. The leakage characteristics and the breakdown strength were compared with our most optimized results for Al_2O_3 deposited by atomic layer deposition (ALD) on Ga_2O_3 (001).

AlSiO/Ga_2O_3 MOSCAPs were fabricated on a 10 μm-thick lightly Si-doped (6.5×10^{16} cm^{-3}) Ga_2O_3 layer epitaxially grown by halide phase vapor epitaxy (HVPE) on an n+ β-Ga_2O_3 (001) substrate. Three samples were treated with three cycles of UV-ozone and 49% HF dip prior to the deposition of the AlSiO dielectric layer. One sample was treated differently, using only 49% HF, to understand the influence of UV-ozone clean on AlSiO/Ga_2O_3 interface quality. The AlSiO dielectric, with a silicon composition of 40%, was grown by metal organic chemical vapor deposition (MOCVD) in a close coupled showerhead chamber. The AlSiO deposition temperature was 700 °C, and the TMAl, Si_2H_6, and O_2 flows were 3.2 μmol/min, 3.2 μmol/min, and 4.4 mmol/min, respectively. The bandgap (E_g), conduction band offset (E_C), and valence band offset (E_V) of AlSiO (with a silicon composition of 40%) with respect to Ga_2O_3 were estimated to be 7.3 eV, 1.9 eV, and 0.5 eV, respectively.[34–36] AlSiO with various thicknesses (10 nm, 20 nm, and 30 nm) was deposited on three different Ga_2O_3 samples treated by UV-ozone followed by an HF dip. A 30 nm-thick AlSiO dielectric layer was deposited on the sample treated by only dipping in the HF. After the dielectric deposition, the Ohmic contact on the backside of the sample was achieved by chlorine-based dry etching and following Ti/Au (20/200 nm) metal stack deposition. The circular gate contact of Cr/Ti/Au (10/20/200 nm) was then patterned on the front side of the sample. The cross-sectional schematic of a typical MOSCAP structure is shown in Fig. 1.

The thickness of AlSiO layer was measured on co-loaded Si wafers using a Woollam M-2000 ellipsometer. C–V measurements were taken at room temperature using a Keithley 4200 semiconductor parameter analyzer. The frequency and amplitude of AC signals were 1 MHz and 30 mV, respectively. The DC voltage sweep was set with a step voltage of 50 mV and a sweep rate of 0.6 V/s. A 254 nm lamp with an optical power density of 0.13 W/cm^2 was used as the deep UV illumination source to ensure sufficient hole generation.

To investigate the impact of UV-ozone clean on AlSiO/Ga_2O_3 properties, two dual C–V sweeps were conducted on the samples that

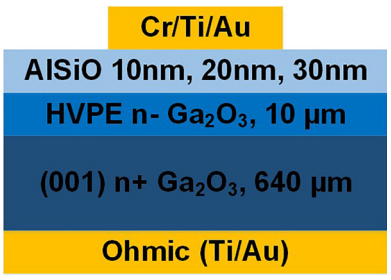

FIG. 1. Cross-sectional schematic of the AlSiO/β-Ga_2O_3 (001) MOSCAP.

were prepared using three cycles of UV-ozone and HF dip. In order to avoid any possible growth run-to-run variations, the two samples were co-loaded during the AlSiO deposition. The thickness of AlSiO on both samples was 30 nm. In the first C–V sweep, the voltage was swept from depletion to accumulation in the dark and then held for a 10 min electrical stress to ensure that all the near-interface slow and fast traps were filled with electrons, then the voltage was swept back to depletion. Then another C–V dual sweep was performed without electrical stress, in which only near-interface fast traps can respond. Note that fast traps can always induce hysteresis, whereas slow traps once filled would behave like fixed charges and can no longer induce any hysteresis. This is because the emission time constant of slow traps is very long by definition. Moreover, in n-type Ga_2O_3, only a few holes are available to recombine with the trapped electrons due to low minority carrier generation rate in wide bandgap materials. Therefore, both near-interface fast and slow traps respond to the first C–V sweep with 10-min stress in accumulation. However, the filled slow traps remain occupied after the first C–V sweep, and only fast traps can respond to the second C–V sweep without the additional stress. The hysteresis for C–V measurement with and without stress were both higher for the sample that did not have the UV-ozone treatment as depicted in Figs. 2(a) and 2(b) and reported in Table I. The corresponding zoom-in C–V sweeps between −1 V and 2 V for AlSiO/Ga_2O_3 MOSCAPs with surface pretreatment of (a) only three cycles of HF and (b) three cycles of UV-ozone and HF are shown in Figs. 2(c) and 2(d), respectively.

The hysteresis ΔV_{FB} is defined to be the voltage shift between forward and reverse sweep at flatband capacitance (C_{FB}). C_{FB} is[37]

$$C_{FB} = \frac{1}{\frac{t}{\epsilon_0 \epsilon_r} + \frac{L_D}{\epsilon_0 \epsilon_s}}, \tag{1}$$

where t is the dielectric thickness, and ϵ_0 and ϵ_r are the vacuum permittivity and relative dielectric constant of AlSiO (measured to be 7.85), respectively. ϵ_s is the relative permittivity of Ga_2O_3. L_D is the Debye length, which could be obtained by the equation[37]

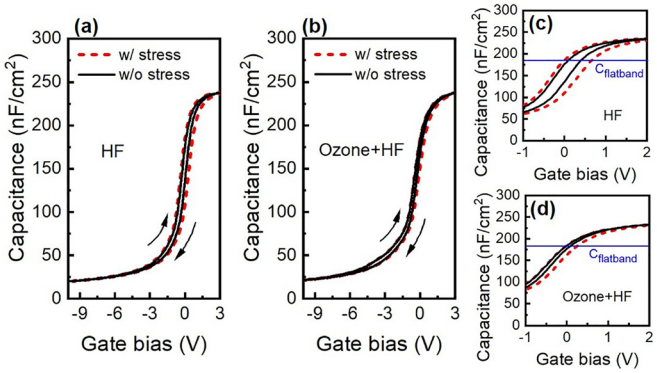

FIG. 2. C–V sweeps of AlSiO/Ga_2O_3 MOSCAPs with surface pretreatment of (a) only three cycles of HF and (b) three cycles of UV-ozone and HF dip. The corresponding zoom-in C–V sweeps between −1 V and 2 V are depicted for (c) only three cycles of HF and (d) three cycles of UV-ozone and HF dip, respectively. The red dotted and black solid lines represent C–V sweeps with and without electrical stress for 10 min at an accumulation field of 1 MV/cm, respectively.

TABLE I. Summary of hysteresis with and without stress ($\Delta V_{FB,\ w/\ stress}$ and $\Delta V_{FB,\ w/o\ stress}$), and calculated near-interface fast and slow traps ($Q_{T,\ fast}$ and $Q_{T,\ slow}$), AlSiO/Ga_2O_3 MOSCAPs with surface treatment of only HF or UV-ozone and HF.

	$\Delta V_{FB,\ w/o\ stress}$ (V)	$\Delta V_{FB,\ w/\ stress}$ (V)	$Q_{T,\ fast}$ (cm^{-2})	$Q_{T,\ slow}$ (cm^{-2})
HF	0.29	0.64	4.2×10^{11}	5.1×10^{11}
HF + UV ozone	0.12	0.31	1.9×10^{11}	3.0×10^{11}

$$L_D = \sqrt{\frac{\epsilon_0 \epsilon_s kT}{N_d q^2}}, \tag{2}$$

where k is the Boltzmann constant, T is the measurement temperature, N_d is the doping of semiconductor ($\sim 6.5 \times 10^{16}\ cm^{-3}$), and q is the electron charge. The density of near-interface traps close to the conduction band edge density Q_T can then be calculated by[32]

$$\Delta V_{FB} = \frac{qQ_T}{C_{OX}} = \frac{qQ_T}{\epsilon_0 \epsilon_r} t. \tag{3}$$

The calculated near-interface slow and fast trap densities are summarized in Table I. A combination of repeated UV-ozone and wet chemical treatment suppressed the fast and slow near-interface traps significantly. This reduction in the density of near-interface traps suggests a cleaner surface with less defects due to the oxidation and removal of surface contaminants by a combination of UV-ozone and HF dip prior to the dielectric deposition.[38] Similar results were found previously on Ga-polar GaN high-electron mobility transistors (HEMTs) with reduced current collapse by ozone oxidation and wet surface treatment before Si_3N_4 passivation.[39]

A series of AlSiO/Ga_2O_3 MOSCAPs with 10 nm-, 20 nm-, and 30 nm-thick AlSiO thicknesses were then fabricated in order to extract density of fixed charge and density of interface states close to the conduction band edge, following the methodology in Ref. 32. A combination of UV-ozone followed by HF dip was employed as surface pretreatment prior to dielectric deposition for all these samples. The ΔV_{FB} values and the linear fit are plotted in Fig. 3(a). The fact that the linear fit passes through the origin confirms that the measured fast/slow traps are at or near the dielectric interface. The fast trap density was extracted to be $2.18 \times 10^{11}\ cm^{-2}$, and the slow trap density excluding the contribution from fast traps was calculated to be $2.73 \times 10^{11}\ cm^{-2}$ from the fitting slope and using Eq. (3).

Assuming negligible charges in the dielectric, the flatband voltage is given by[40]

$$V_{FB} = -\frac{qQ_F}{\epsilon_0 \epsilon_r} t + \Phi_{MS}, \tag{4}$$

where V_{FB} is the flatband voltage, Q_F is the net charge at the AlSiO/Ga_2O_3 interface, and Φ_{MS} is the work function difference between metal and semiconductor. From the V_{FB}-thickness relationship shown in Fig. 3(b), a net positive fixed interface charge of $1.56 \times 10^{12}\ cm^{-2}$ was extracted from the fitting slope using Eq. (4).

To extract the D_{it} more accurately and to account for interface traps significantly below the conduction band edge as well as hole traps in the bulk dielectric, we followed a deep UV-assisted C–V methodology developed by Liu *et al.*[31] based on the work of Swenson and Mishra.[41] First, a 10-min accumulation electric field (1 MV/cm) was applied to the MOSCAPs in the dark to ensure all traps were filled with electrons. The first forward C–V sweep was then measured and identified as ideal dark curve. Then, the devices were biased in depletion and illuminated by 254 nm deep UV for 1 min. After the deep UV illumination, the device was biased in depletion for additional 10 min to allow generated holes to move toward the AlSiO/Ga_2O_3 interface and recombine with trapped electrons. A second forward post-UV C–V profile was then measured and marked as post-UV curve. The band diagrams of AlSiO/Ga_2O_3 MOSCAPs in different UV-assisted

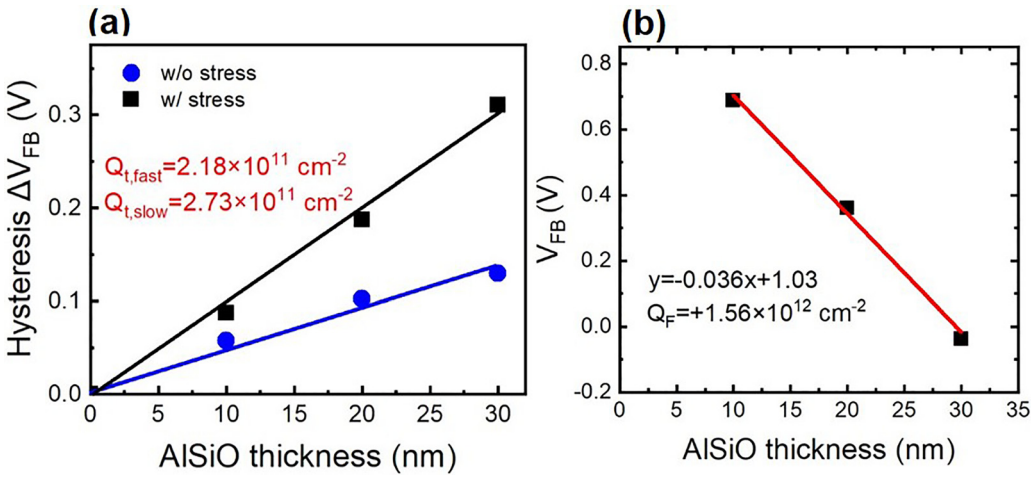

FIG. 3. (a) Hysteresis ΔV_{FB} with and without stress and (b) V_{FB} as a function of AlSiO thickness measured on AlSiO/Ga_2O_3 MOSCAPs.

C–V measurement steps can be found in the supplementary material. Figure 4(a)–4(c) shows the deep UV-assisted C–V characteristics (left) and corresponding trap density (D_t) as a function of energy (right) for the MOSCAPs with 10 nm-, 20 nm-, and 30 nm-thick AlSiO, respectively. In these figures, the ideal dark curve was shifted to match the capacitance value of the post-UV curve in the deep depletion regime. This shift is caused by captured and accumulated holes at the interface and bulk dielectric. The trap density (D_t), which is a combination of interface states and dielectric bulk traps, was calculated using the following relationship:[42]

$$D_t = \frac{C_{ox}}{Aq}\frac{d\Delta V}{d\psi_S} = \frac{dN_{it}}{d\psi_S} + t\frac{dN_{bulk}}{2d\psi_S} = D_{it} + t\frac{n_{bulk}}{2}, \quad (5)$$

where ψ_S is the surface potential and can be calculated from the semiconductor capacitance and doping concentration; D_{it} and n_{bulk} are the density of interface state and bulk trap, respectively. ΔV is the voltage difference between the shifted ideal dark curve and post-UV curve at a given capacitance. Average D_t for various thicknesses of AlSiO was calculated. Fig. 4(d) shows the linear fit of average D_t as a function of AlSiO thickness. An average D_{it} of $6.63 \times 10^{11}\ cm^{-2}eV^{-1}$ and n_{bulk} of $4.65 \times 10^{17}\ cm^{-3}\ eV^{-1}$ were extracted from the y-intercept and slope of the linear fitting to Eq. (5), respectively. This interface state density is approximately half of the D_{it} value that was measured using the same technique on ALD Al_2O_3 deposited on (001) Ga_2O_3 MOSCAPs fabricated by our group.[42] It is worth noting that in UV-assisted C–V measurements, bulk hole traps can be ionized via (i) exciting electrons from the trap to the conduction band and (ii) by generated holes in Ga_2O_3 tunneling and hopping through the traps.

Figure 5 compares the forward breakdown voltage (BV) characteristics of 30-nm AlSiO/Ga_2O_3 MOSCAPs with our previous studies on ALD Al_2O_3/Ga_2O_3(001) MOSCAPs.[42] The avalanche breakdown occurred at ~7.8 MV/cm for both AlSiO and Al_2O_3 dielectrics. An operation range of ~3.7 MV/cm was achieved on AlSiO dielectric beyond which the leakage current was more than the detection limit current level ($\sim 5 \times 10^{-8}$ A/cm^2). This value is larger than the corresponding value (~3.1 MV/cm) that was measured for the ALD-Al_2O_3. At electric fields above 4 MV/cm and below the BV, the AlSiO/Ga_2O_3 MOSCAP exhibited two orders of magnitude lower gate leakage than that of ALD-Al_2O_3/Ga_2O_3 MOSCAPs. This lower leakage current could be attributed to the higher conduction band offsets of AlSiO [ΔE_C (AlSiO) = 1.9 eV, ΔE_C (Al_2O_3) = 1.5 eV],[34,35] reduced field-induced trap generation, and possible reduction of electron hopping from the Ga_2O_3 to the gate metal.[33] The promising results demonstrated in this paper show the potential for using AlSiO as high performance and more reliable gate dielectric for Ga_2O_3-based FETs.

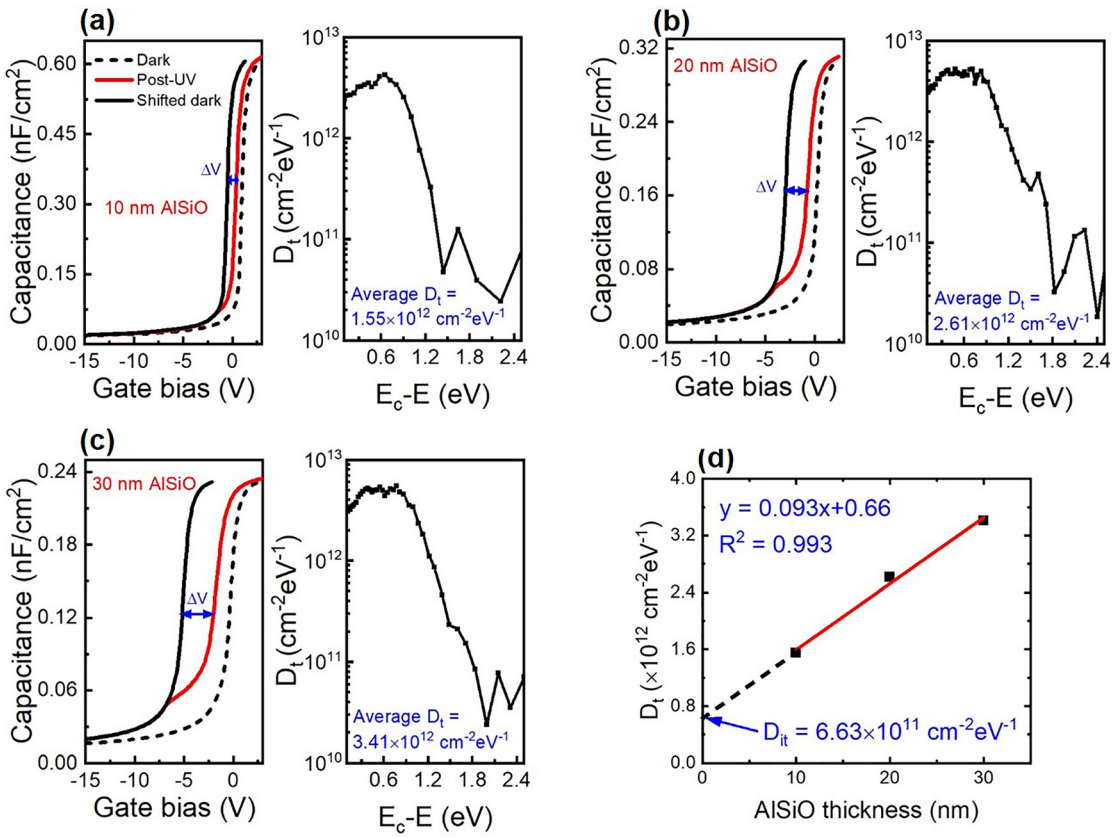

FIG. 4. The measured C–V curves (left) and corresponding D_t profile (right) for (a) 10 nm-, (b) 20 nm-, and (c) 30 nm-thick AlSiO/Ga_2O_3 MOSCAPs. (d) The linear fit of average trap density as a function of AlSiO thickness. The y-axis intercept and slope correspond to the interface density (D_{it}) of $6.63 \times 10^{11}\ cm^{-2}eV^{-1}$ and the bulk trap density (n_{bulk}) of $4.65 \times 10^{17}\ cm^{-3}eV^{-1}$.

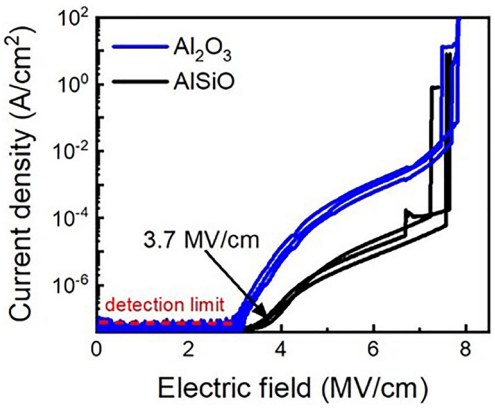

FIG. 5. Forward-bias current–voltage characteristics of ALD-Al_2O_3/Ga_2O_3 and $AlSiO/Ga_2O_3$ MOSCAPs.

In summary, the interface and bulk properties of MOCVD AlSiO deposited on β-Ga_2O_3 were investigated using UV-assisted capacitance–voltage measurements. Negligible C–V hysteresis was achieved by a surface pretreatment that included three cycles of UV-ozone followed by an HF dip. Using deep UV-assisted C–V method, an average interface state density of $6.63 \times 10^{11}\,cm^{-2}\,eV^{-1}$ and a hole trap density in the bulk AlSiO of $4.65 \times 10^{17}\,cm^{-3}\,eV^{-1}$ were quantified, which is half of that measured on ALD Al_2O_3/Ga_2O_3 MOSCAPs. Moreover, MOCVD AlSiO demonstrated more effective suppression of leakage current compared with ALD Al_2O_3 before avalanche breakdown occurred. The negligible hysteresis, low interfacial trap density, low leakage current, and high breakdown electric field achieved on $AlSiO/Ga_2O_3$ MOSCAPs reveal MOCVD AlSiO as a promising gate dielectric for high-performance Ga_2O_3 devices.

See the supplementary material for band diagrams of $AlSiO/Ga_2O_3$ MOSCAPs in UV-assisted C–V measurement.

This work was supported by the Air Force Office of Scientific Research (Program Manager, Dr. Ali Sayir) through program No. FA9550-20-1-0045, the National Science Foundation under Grant No. 2043803, and Office of Naval Research (Program Manager, Dr. Paul Maki) under program No. N00014-20-1-2130. This work was performed in part at the University of Michigan Lurie Nanofabrication Facility, which is supported by the College of Engineering at the University of Michigan.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]R. Roy, V. G. Hill, and E. F. Osborn, J. Am. Chem. Soc. **74**, 719 (1952).
[2]B. J. Baliga, IEEE Electron Device Lett. **10**, 455 (1989).
[3]M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, Appl. Phys. Lett. **100**, 013504 (2012).
[4]E. Ahmadi and Y. Oshima, J. Appl. Phys. **126**, 160901 (2019).
[5]A. Z. Jian, K. Khan, and E. Ahmadi, Int. J. High Speed Electron. Syst. **28**, 1940006 (2019).
[6]H. Aida, K. Nishiguchi, H. Takeda, N. Aota, K. Sunakawa, and Y. Yaguchi, Jpn. J. Appl. Phys., Part 1 **47**, 8506 (2008).
[7]K. Sasaki, M. Higashiwaki, A. Kuramata, T. Masui, and S. Yamakoshi, IEEE Electron Device Lett. **34**, 493 (2013).
[8]M. Higashiwaki, K. Konishi, K. Sasaki, K. Goto, K. Nomura, Q. T. Thieu, R. Togashi, H. Murakami, Y. Kumagai, B. Monemar, A. Koukitu, A. Kuramata, and S. Yamakoshi, Appl. Phys. Lett. **108**, 133503 (2016).
[9]Z. (A.) Jian, S. Mohanty, and E. Ahmadi, Appl. Phys. Lett. **116**, 152104 (2020).
[10]J. F. Mcglone, Z. Xia, Y. Zhang, C. Joishi, S. Lodha, S. Rajan, S. A. Ringel, and A. R. Arehart, IEEE Electron Device Lett. **39**, 1042 (2018).
[11]K. D. Chabak, J. P. McCandless, N. A. Moser, A. J. Green, K. Mahalingam, A. Crespo, N. Hendricks, B. M. Howe, S. E. Tetlak, K. Leedy, R. C. Fitch, D. Wakimoto, K. Sasaki, A. Kuramata, and G. H. Jessen, IEEE Electron Device Lett. **39**, 67 (2018).
[12]M. H. Wong, K. Goto, Y. Morikawa, A. Kuramata, S. Yamakoshi, H. Murakami, Y. Kumagai, and M. Higashiwaki, Appl. Phys. Express **11**, 064102 (2018).
[13]E. Ahmadi, O. S. Koksaldi, S. W. Kaun, Y. Oshima, D. B. Short, U. K. Mishra, and J. S. Speck, Appl. Phys. Express **10**, 041102 (2017).
[14]S. Krishnamoorthy, Z. Xia, C. Joishi, Y. Zhang, J. McGlone, J. Johnson, M. Brenner, A. R. Arehart, J. Hwang, S. Lodha, and S. Rajan, Appl. Phys. Lett. **111**, 023502 (2017).
[15]Y. Zhang, Z. Xia, C. Joishi, and S. Rajan, in *76th Device Research Conference* (IEEE, 2018), pp. 1–2.
[16]E. Ahmadi, O. S. Koksaldi, X. Zheng, T. Mates, Y. Oshima, U. K. Mishra, and J. S. Speck, Appl. Phys. Express **10**, 071101 (2017).
[17]W. Li, K. Nomoto, Z. Hu, T. Nakamura, D. Jena, and H. G. Xing, in *IEEE International Electron Devices Meeting* (IEEE, San Francisco, CA, USA, 2019), pp. 12.4.1–12.4.4.
[18]S. Sharma, K. Zeng, S. Saha, and U. Singisetti, IEEE Electron Device Lett. **41**, 836 (2020).
[19]P. H. Carey, F. Ren, D. C. Hays, B. P. Gila, S. J. Pearton, S. Jang, and A. Kuramata, Jpn. J. Appl. Phys., Part 1 **56**, 071101 (2017).
[20]L. Yuan, H. Zhang, R. Jia, L. Guo, Y. Zhang, and Y. Zhang, Appl. Surf. Sci. **433**, 530 (2018).
[21]H. Dong, W. Mu, Y. Hu, Q. He, B. Fu, H. Xue, Y. Qin, G. Jian, Y. Zhang, S. Long, Z. Jia, H. Lv, Q. Liu, X. Tao, and M. Liu, AIP Adv. **8**, 065215 (2018).
[22]V. D. Wheeler, D. I. Shahin, M. J. Tadjer, and C. R. Eddy, ECS J. Solid State Sci. Technol. **6**, Q3052 (2017).
[23]P. H. Carey, F. Ren, D. C. Hays, B. P. Gila, S. J. Pearton, S. Jang, and A. Kuramata, J. Vac. Sci. Technol. B **35**, 041201 (2017).
[24]H. N. Masten, J. D. Phillips, and R. L. Peterson, IEEE Trans. Electron Devices **66**, 2489 (2019).
[25]S. H. Chan, M. Tahhan, X. Liu, D. Bisi, C. Gupta, O. Koksaldi, H. Li, T. Mates, S. P. DenBaars, S. Keller, and U. K. Mishra, Jpn. J. Appl. Phys., Part 1 **55**, 021501 (2016).
[26]D. Kikuta, K. Itoh, T. Narita, and T. Mori, J. Vac. Sci. Technol. A **35**, 01B122 (2017).
[27]C. Gupta, S. H. Chan, A. Agarwal, N. Hatui, S. Keller, and U. K. Mishra, IEEE Electron Device Lett. **38**, 1575 (2017).
[28]I. Sayed, B. Bonef, W. Liu, S. Chan, J. Georgieva, J. S. Speck, S. Keller, and U. K. Mishra, Appl. Phys. Lett. **115**, 172104 (2019).
[29]S. H. Chan, S. Keller, O. S. Koksaldi, C. Gupta, S. P. DenBaars, and U. K. Mishra, J. Cryst. Growth **464**, 54 (2017).
[30]I. Sayed, W. Liu, J. Georgieva, A. Krishna, S. Keller, and U. K. Mishra, Semicond. Sci. Technol. **35**, 095027 (2020).
[31]W. Liu, I. Sayed, C. Gupta, H. Li, S. Keller, and U. Mishra, Appl. Phys. Lett. **116**, 022104 (2020).
[32]W. Liu, I. Sayed, J. Georgieva, S. Chan, S. Keller, and U. K. Mishra, J. Appl. Phys. **128**, 074101 (2020).
[33]I. Sayed, W. Liu, B. Romanczyk, J. Georgieva, S. Chan, S. Keller, and U. K. Mishra, Appl. Phys. Express **13**, 061010 (2020).
[34]K. Ito, D. Kikuta, T. Narita, K. Kataoka, N. Isomura, K. Kitazumi, and T. Mori, Jpn. J. Appl. Phys., Part 1 **56**, 04CG07 (2017).
[35]Y. W. Huan, S. M. Sun, C. J. Gu, W. J. Liu, S. J. Ding, H. Y. Yu, C. T. Xia, and D. W. Zhang, Nanoscale Res. Lett. **13**, 246 (2018).

[36]M. E. Levinshtein, S. L. Rumyantsev, and M. S. Shur, *Properties of Advanced Semiconductor Materials GaN, AlN, InN, BN, SiC, SiGe* (John Wiley & Sons, Inc.,, 2001).
[37]U. K. Mishra and J. Singh, *Semiconductor Device Physics and Design* (Springer, Dordrecht, The Netherlands, 2007).
[38]K. Fu, H. Fu, X. Huang, H. Chen, T. H. Yang, J. Montes, C. Yang, J. Zhou, and Y. Zhao, IEEE Electron Device Lett. **40**, 1728 (2019).
[39]S. Lin, M. Wang, B. Xie, C. P. Wen, M. Yu, J. Wang, Y. Hao, W. Wu, S. Huang, K. J. Chen, and B. Shen, IEEE Electron Device Lett. **36**, 757 (2015).
[40]T. H. Hung, K. Sasaki, A. Kuramata, D. N. Nath, P. Sung Park, C. Polchinski, and S. Rajan, Appl. Phys. Lett. **104**, 162106 (2014).
[41]B. L. Swenson and U. K. Mishra, J. Appl. Phys. **106**, 064902 (2009).
[42]Z. (A.) Jian, S. Mohanty, and E. Ahmadi, Appl. Phys. Lett. **116**, 242105 (2020).