LETTER

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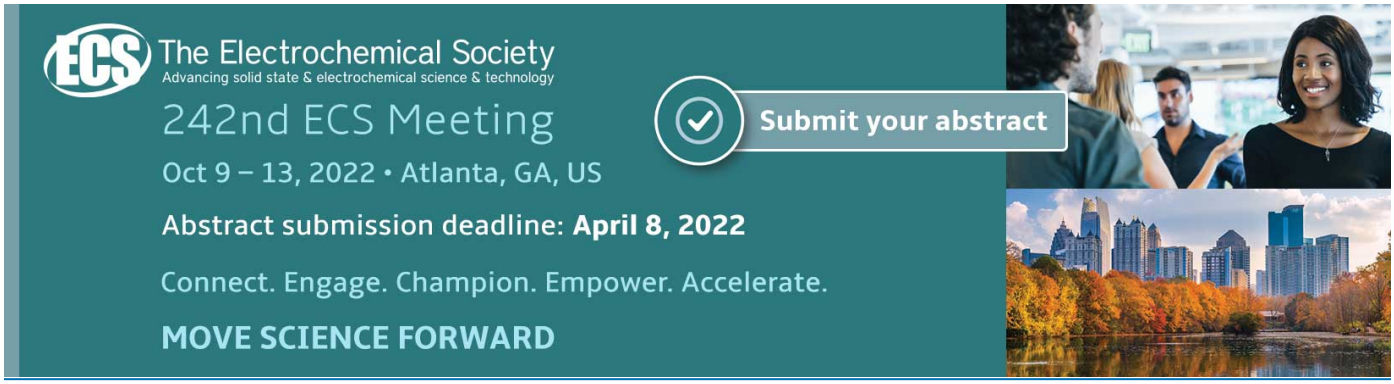

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Letter

Improved operational reliability of MOCVD-grown AlSiO gate dielectric on β-Ga_2O_3 (001) by post-metallization annealing

Zhe Ashley Jian[1,*], Islam Sayed[2], Subhajit Mohanty[1], Wenjian Liu[2] and Elaheh Ahmadi[1,3]

[1] Department of Electrical and Computer Engineering, University of Michigan, Ann Arbor, MI 48109, United States of America

[2] Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, United States of America

[3] Applied Physics Program, University of Michigan, Ann Arbor, MI 48109, United States of America

E-mail: jianzhe@umich.edu

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Abstract

In this work, we studied the impact of post-metallization annealing (PMA) on interfacial and bulk dielectric properties of AlSiO/β-Ga_2O_3 metal–oxide–semiconductor capacitors (MOSCAPs). Annealing at 300 °C improved the reverse operational stability within the test operation range from −10 V to −42 V. The near-interface fast and slow traps were both suppressed by PMA at 300 °C and 350 °C, leading to a negligible flat-band voltage hysteresis. The low gate leakage region was extended from 3.7 MV cm^{-1} to 4 MV cm^{-1} and the breakdown strength was improved from 7.8 MV cm^{-1} to 8.2 MV cm^{-1} for AlSiO/β-Ga_2O_3 MOSCAPs with PMA at 300 °C compared with not-annealed samples. The superior operational reliability demonstrated in this work is useful for future high-performance and reliable MOS-based Ga_2O_3 transistors.

Keywords: β-Ga_2O_3, annealing, reliability, capacitance–voltage (C–V) characteristics, hysteresis

(Some figures may appear in color only in the online journal)

1. Introduction

β-Ga_2O_3 has shown tremendous potential for high power applications due to its ultra-wide bandgap of 4.8 eV, large breakdown field (~8 MV cm^{-1}) and cost-effective melt-grown bulk substrates [1–5]. Rapid progress and breakthroughs have been achieved in various Ga_2O_3-based devices [3, 6, 7]. Enhancement-mode vertical Fin-field effect transistors (Fin-FETs) demonstrated a breakdown voltage (BV) over 2.6 kV and Baliga's figure-of-merit of 280 MW cm^{-2} [8]. Recently, a record high BV of 8.03 kV was achieved on field-plated lateral metal-oxide-semiconductor FETs (MOSFETs) with polymer passivations [9].

The development of high-quality gate dielectrics is critical for enabling high performance and switching capability of β-Ga_2O_3 MOS-based transistors. The gate dielectric should combine the merits of large band offset, low interface states with Ga_2O_3 and preferably a higher breakdown field than underlying semiconductor. Many reliability issues such as threshold voltage variation, pre-mature dielectric breakdown and frequency-dependent dispersion are related to dielectric

* Author to whom any correspondence should be addressed.

degradation which affects the switching performance of high power devices. To date, there have been extensive efforts on investigating the dielectric performance of SiO_2, HfO_2 and Al_2O_3 on β-Ga_2O_3 [9–13] along with a few studies on novel dielectrics such as ZrO_2, $LaAl_2O_3$, and $(Y_{0.6}Sc_{0.4})_2O_3$ [14–16].

Aluminum silicon oxide (AlSiO) has been proposed as a high-quality and reliable gate dielectric for GaN-based devices [17–19]. Alloying of Al_2O_3 with silicon to form amorphous AlSiO has the potential to incorporate the advantages of both SiO_2 ($E_g = 9.0$ eV) and Al_2O_3 ($E_g = 6.7$ eV) thus realizing high band offsets and high breakdown strength [18, 20]. A low interface states (D_{it}) of $\sim 10^{12}$ cm^{-2} eV^{-1} was achieved in AlSiO on Ga-polar GaN using metal–organic chemical vapor deposition (MOCVD) technique and a dielectric lifetime of 20 years for electric fields higher than 3 MV cm^{-1} was predicted by Chan *et al* [17, 21]. Sayed *et al* studied the impact of GaN polarity and the effect of post-metallization annealing (PMA) on the electrical properties of AlSiO/N-polar GaN MOS devices [20, 22, 23]. Annealing in air ambient at 370 °C was reported to reduce the density of near-interface traps by a factor of two from 5.6×10^{11} to 2.6×10^{11} cm^{-2} [23]. Recently, we demonstrated MOCVD-grown AlSiO gate dielectric on (001) β-Ga_2O_3 with negligible hysteresis, low gate leakage, low interfacial trap density of 6.63×10^{11} cm^{-2} eV^{-1}, and high breakdown electric field of $\sim$7.8 MV cm^{-1} [24]. This motivated us to further enhance the electrical properties of AlSiO/Ga_2O_3 MOS capacitors (MOSCAPs) and study its operational reliability for future high power switching applications.

In this work, MOCVD-grown AlSiO/β-Ga_2O_3 (001) MOS structures were fabricated and tested for operational stability. The impact of PMA at different temperatures on forward and reverse flat-band voltage stability was studied. The interfacial and bulk properties of AlSiO on Ga_2O_3 were investigated using deep UV assisted capacitance–voltage (C–V) methodology. In addition, forward gate leakage performance and breakdown strength were compared for samples with or without annealing.

2. Experimental methods

The AlSiO/Ga_2O_3 MOSCAP structures in this study consisted of a 10 μm thick lightly Si-doped ($\sim 6.5 \times 10^{16}$ cm^{-3}) Ga_2O_3 epitaxial layer grown by halide phase vapor epitaxy on an n+ Sn-doped β-Ga_2O_3 (001) substrate. Surface pretreatment of three cycles of UV–ozone and 49% HF dip was performed prior to the deposition of the AlSiO dielectric layer [24]. The AlSiO with various thicknesses (10 nm, 20 nm, and 30 nm), with a silicon composition of $\sim$40%, were grown by MOCVD at 700 °C. The bandgap (E_g), conduction band offset (E_C) and valence band offset (E_V) of AlSiO with respect to Ga_2O_3 were estimated to be 7.3 eV, 1.9 eV and 0.5 eV, respectively [25–27]. After the dielectric deposition, backside ohmic contact was formed by chlorine-based inductively coupled-plasma etching before Ti/Au (20/200 nm) deposition [28]. No rapid thermal annealing was performed. The Cr/Ti/Au (10/20/200 nm) metal stack was deposited on top as gate contact. In the annealing study to improve device performance, the MOSCAPs were then annealed at 300 °C and 350 °C for 30 min in a vacuum chamber ($\sim 8 \times 10^{-5}$ torr).

The thickness of AlSiO layer was analyzed on co-loaded Si wafers using a Woollam M-2000 ellipsometer. C–V and current–voltage (I–V) measurements were taken at room temperature using a Keysight B1500A semiconductor parameter analyzer. The frequency and amplitude of AC signals were set with 1 MHz and 30 mV, respectively. Deep UV assisted C–V characterization was conducted using a deep UV lamp with a wavelength of 254 nm and an optical power density of 0.13 W cm^{-2}.

3. Results and discussion

The impact of PMA on the forward operational reliability of AlSiO/Ga_2O_3 MOSCAPs was explored through step-stress C–V measurements, as depicted in figures 1(a)–(c). The AlSiO thickness was 30 nm for all the tested devices. First, the initial depletion–accumulation ($D > A$) C–V sweep was measured from -15 V to 2 V and considered as a reference curve. Then the MOSCAP was stressed at a forward bias voltage for 10 s, and immediately swept backward from accumulation to depletion ($A > D$). The forward stress voltage was varied from 2 V to 15 V sequentially, which corresponds to electric fields from 0.67 MV cm^{-1} to 5 MV cm^{-1}. The electric field (E_{field}) was calculated by gate bias divided by the dielectric thickness, assuming E_{field} is uniform inside dielectric. Flat-band voltage was calculated at flat-band capacitance of each C–V sweep, following Jian *et al* [24]. The hysteresis (ΔV_{FB}) is the flat-band voltage difference between each $A > D$ curve and the reference $D > A$ curve. The relationship between extracted ΔV_{FB} and forward stress voltage for five devices with and without PMA is shown in figure 1(d) statistically. No significant change of ΔV_{FB} between not-annealed and annealed samples was observed. The ΔV_{FB} increased with increasing the stress voltage on all three samples. Specifically, the ΔV_{FB} increased slightly up to 2 V at the forward stress of 9 V (3 MV cm^{-1}). Beyond the critical stress of 3 MV cm^{-1}, the ΔV_{FB} increased at a higher speed and reached to $\sim$7 V at a forward stress of 5 MV cm^{-1}. This trend of positive flat-band voltage shift suggests the existence of negative charge trapping in the dielectric dependent of the applied DC positive bias under accumulation region. Significant charge trapping occurring at high-field stress suggests electrons tunneling and hopping into the dielectric [29]. Note that the maximum stress field of 5 MV cm^{-1} in our study is approximately four times larger than that applied to the gate in vertical β-Ga_2O_3 FinFET on-state operation [8].

Figures 2(a)–(c) shows typical reverse step-stress results for 30 nm AlSiO/Ga_2O_3 MOSCAPs. The reference $A > D$ curve was swept from 5 V to -10 V. The following $D > A$ C–V sweeps were taken after the gate bias was held at a negative depletion voltage for 3 min and then swept back to 5 V. The reason for non-uniform stress periods for forward and reverse bias is that the semiconductor shared the electric field partially

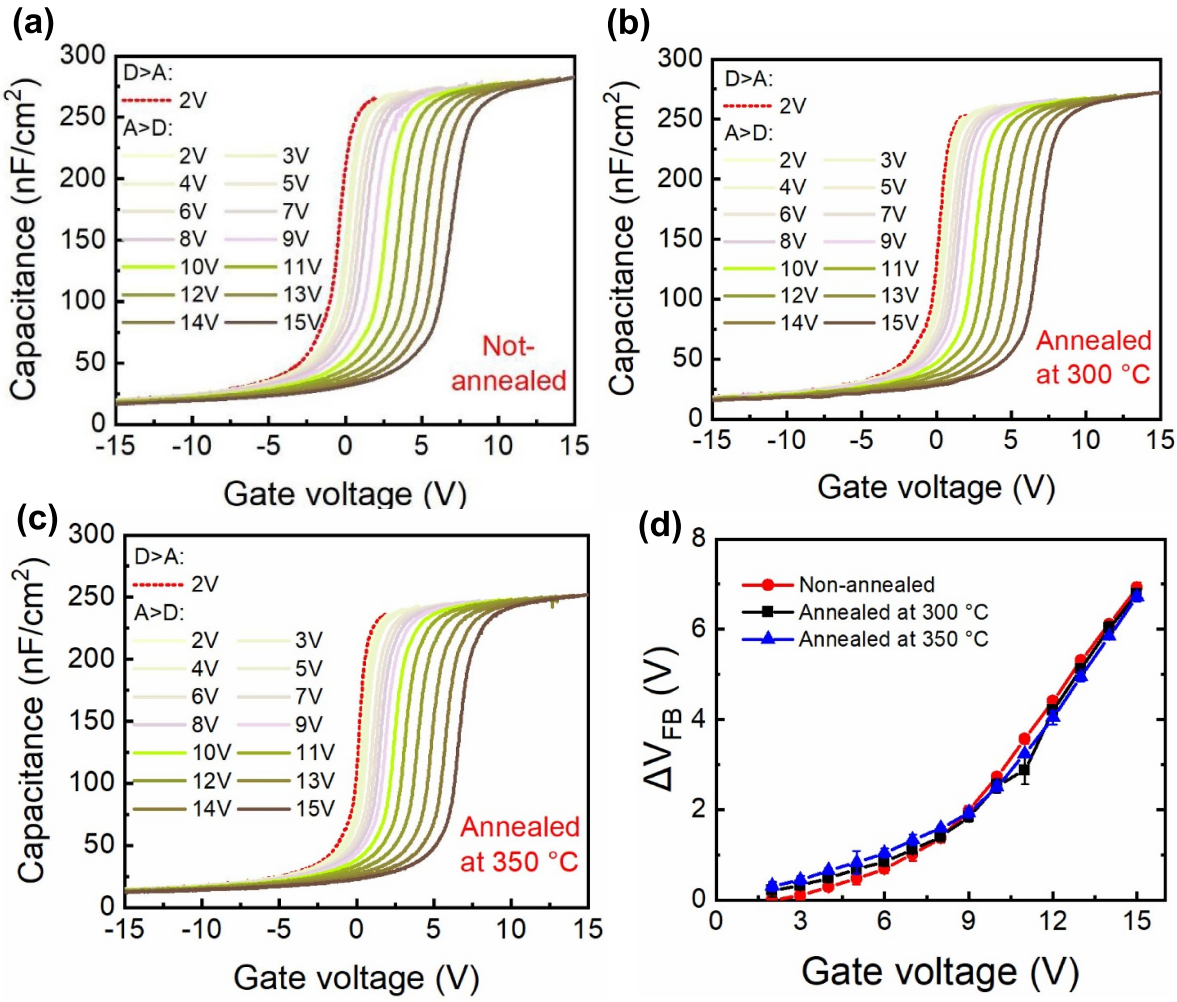

Figure 1. Forward step-stress *C*–*V* profiles of 30 nm AlSiO/Ga_2O_3 MOSCAPs: (a) not-annealed, (b) annealed at 300 °C, and (c) annealed at 350 °C. The maximum accumulation voltage was increased for each sweep from 2 V to 15 V by a step voltage of 1 V. (d) Corresponding flat-band hysteresis ΔV_{FB} versus applied forward stress for 10 s. The depletion–accumulation ($D > A$) *C*–*V* curve from 2 V to −15 V was identified as a reference for accumulation–depletion ($A > D$) *C*–*V* profiles and ΔV_{FB} calculation.

when MOSCAP was biased at the reverse region, whereas, the dielectric withheld most of the electric field when the device was biased at the forward region. Therefore, the reverse bias has less stressing impact on the dielectric and the longer stress period was needed for reverse stability test to make the *C*–*V* flat-band voltage shifts more visible. The negative depletion bias was increased for each *C*–*V* sweep from −10 V to −42 V by a step voltage of −2 V. The ΔV_{FB} is the voltage difference between measured $D > A$ curve and reference $A > D$ curve. The extracted ΔV_{FB} as a function of reverse stress voltage for five devices is illustrated in figure 2(d). The hysteresis value reduced as annealing temperature increased. For the sample not-annealed or annealed at 350 °C, the ΔV_{FB} was almost stable until the reverse voltage extended to ∼−36 V and then the ΔV_{FB} changed significantly with increasing the voltage stress. On the other hand, the *C*–*V* sweeps of sample with PMA at 300 °C were almost identical to each other and ΔV_{FB} was stable until the reverse stress reached to −38 V. Only slight increase in ΔV_{FB} was observed at reverse stress of −40 V and −42 V. This behavior is probably attributed to the reduction of defects/mobile ions at the interface and dielectric due to PMA at 300 °C. It should be mentioned that the accumulation capacitance of samples treated with PMA at 300 °C and 350 °C decreased from 265 nF cm^{-2} (not-annealed) to 261 nF cm^{-2} and 245 nF cm^{-2}, respectively. This decrease in accumulation capacitance can be explained by a dielectric degradation with lower dielectric constant probably due to the gate metal (Cr/Ti/Au) diffusion into dielectric during PMA at higher temperature [30–32].

To further explore the impact of PMA on the interface states near the conduction band edge, two *C*–*V* dual sweeps were conducted. In the first *C*–*V* sweep, the gate voltage was biased from depletion to accumulation, then held at accumulation for a 10 min stress prior to sweeping back to depletion. Since the first *C*–*V* sweep contains a stress, the measured hysteresis is associated with the behavior of both the slow and fast trap near the conduction band edge [23]. Next, another dual *C*–*V* sweep was performed without an electrical stress; the gate voltage was swept from depletion to accumulation and then immediately back to depletion, in which the slow traps were

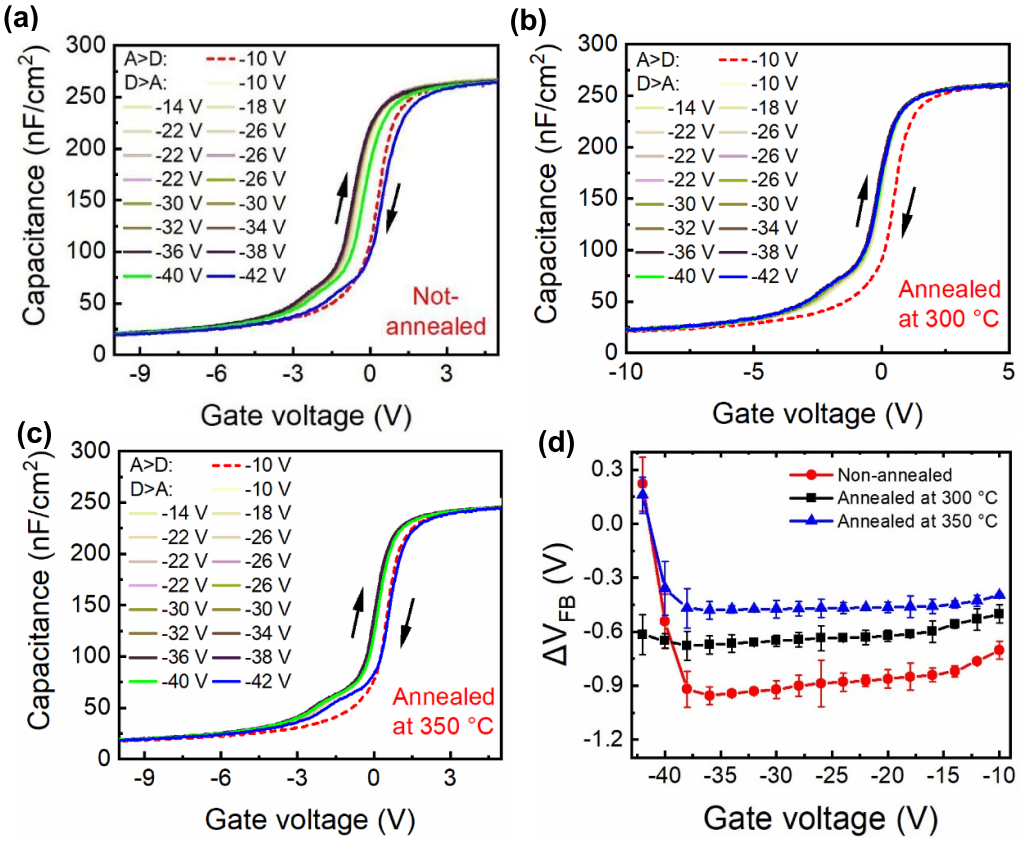

Figure 2. Reverse step-stress *C*–*V* profiles of 30 nm AlSiO/Ga_2O_3 MOSCAPs: (a) not-annealed, (b) annealed at 300 °C, and (c) annealed at 350 °C. The maximum depletion voltage was decreased for each sweep from −10 V to −42 V by a step voltage of −2 V. (d) Corresponding flat-band hysteresis ΔV_{FB} versus applied reverse stress for 3 min. The accumulation–depletion ($A > D$) *C*–*V* curve from 5 V to −10 V was identified as a reference for depletion–accumulation ($A > D$) *C*–*V* profiles and ΔV_{FB} calculation.

Table 1. Summary of hysteresis with and without stress ($\Delta V_{FB,\ w/\ stress}$ and $\Delta V_{FB,\ w/o\ stress}$), calculated near-interface fast and slow traps ($Q_{T,\ fast}$ and $Q_{T,\ slow}$) for not-annealed, annealed at 300 °C and 350 °C AlSiO/Ga_2O_3 MOSCAPs. The AlSiO thicknesses were 30 nm.

	$\Delta V_{FB,\ w/o\ stress}$ (V)	$\Delta V_{FB,\ w/\ stress}$ (V)	$Q_{T,\ fast}$ (cm^{-2})	$Q_{T,\ slow}$ (cm^{-2})
Not-annealed	0.12	0.31	1.9×10^{11}	3.0×10^{11}
Annealed at 300 °C	0.05	0.23	5.6×10^{10}	2.8×10^{11}
Annealed at 350 °C	0.06	0.26	7.5×10^{10}	3.1×10^{11}

maintained occupied and only fast traps could respond. ΔV_{FB} extracted from the *C*–*V* measurements and calculated near-interface fast and slow traps are depicted in table 1 for 30 nm AlSiO/Ga_2O_3 MOSCAPs. Annealing at 300 °C and 350 °C decreased both hysteresis values with and without electrical stress. Compared to sample without PMA treatment, the density of fast and slow traps was reduced by 68% and 6.7% for the sample with PMA at 300 °C. This decrease in the density of near-interface traps suggests that annealing reduced the interface defects or dangling bonds similar to our previously report on hysteresis reduction at the interface between Al_2O_3 and (001) β-Ga_2O_3 [33]. It is noted that PMA at higher temperature of 350 °C resulted in less reduction in the density of near-interface fast traps and slight increase in slow traps with respect to PMA at 300 °C.

Figure 3(a) depicts the D_t as a function of energy for samples with and without PMA measured via deep UV assisted *C*–*V* methodology proposed by Swenson *et al* [34] and Liu *et al* [35]. This measurement was developed to characterize the changing occupancy of interface states and bulk traps, accounting for interface traps significantly below the conduction band edge as well as hole traps in the bulk dielectric. Figure 3(b) shows the calculated average D_t statistics for samples with and without PMA. The average D_t was calculated for energy below E_C-0.15 eV, where the depletion capacitance dominates. The results show that, PMA at 300 °C reduced the density of traps occupying energy levels over the range of 0.15–1.5 eV away from the Ga_2O_3 conduction band. The average D_t for sample with PMA at 300 °C was calculated to be 3.06×10^{12} cm^{-2} eV^{-1}, which was smaller than the average D_t of 3.56×10^{12} cm^{-2} eV^{-1} calculated for not-annealed samples. PMA at 350 °C was found to increase the density of traps, which suggests a slightly degraded AlSiO/Ga_2O_3 interface and bulk dielectric.

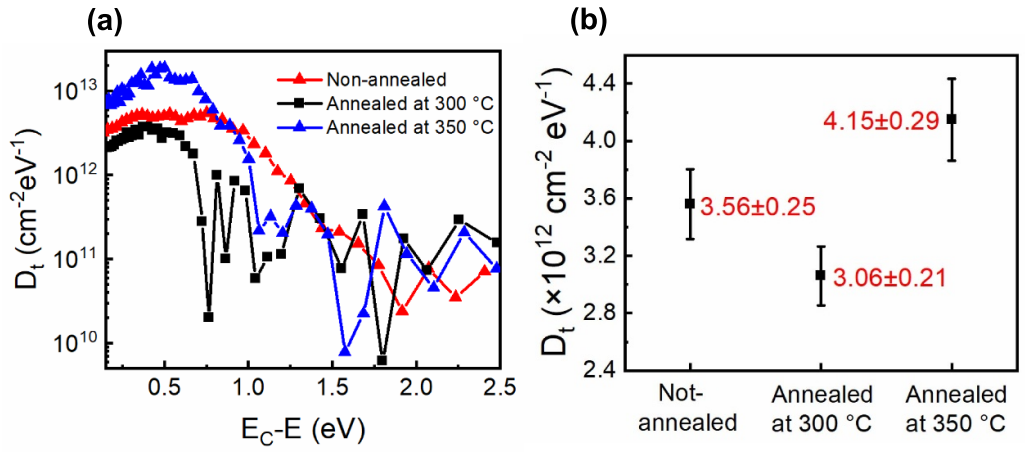

Figure 3. Total traps (D_t) as the function of energy and (b) average D_t for not-annealed, annealed at 300 °C and 350 °C AlSiO/Ga_2O_3 MOSCAPs. The AlSiO thicknesses were 30 nm for all the samples.

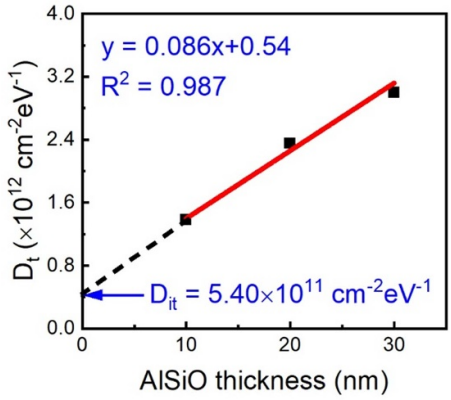

Figure 4. The linear fit of average trap density as a function of AlSiO thickness. The *y*-axis intercept and slope correspond to the interface density (D_{it}) of 5.4 × 10^{11} cm^{-2} eV^{-1} and the bulk trap density (n_{bulk}) of 4.3 × 10^{17} cm^{-3} eV^{-1}.

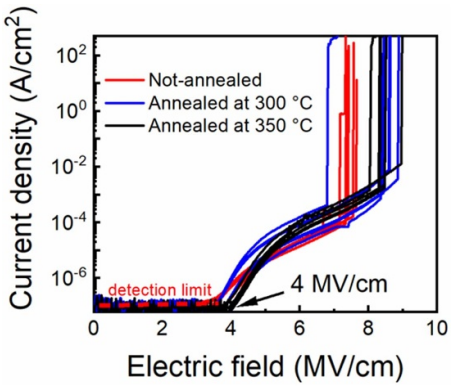

Figure 5. Forward leakage characteristics of AlSiO/Ga_2O_3 MOSCAPs with and without PMA. Annealing extended the region of low-leakage operation from 0–3.7 MV cm^{-1} to 0–4 MV cm^{-1} in the forward bias region.

Next, a series of AlSiO/Ga_2O_3 MOSCAPs with 10 nm, 20 nm and 30 nm thick AlSiO were annealed at 300 °C to characterize the interface states and bulk traps by deep UV assisted *C*–*V* method. Further details about this methodology and physical analytical model can be found in [36]. Figure 4 shows the linear fit of average D_t as a function of AlSiO thickness. The D_{it} of 5.4 × 10^{11} cm^{-2} eV^{-1} and n_{bulk} of 4.3 × 10^{17} cm^{-3} eV^{-1} were extracted from the *y*-intercept and slope of the linear fit, respectively. Both interface state density and bulk traps are smaller than that were measured on AlSiO/Ga_2O_3 MOSCAPs without annealing, with corresponding D_{it} and n_{bulk} of 6.63 × 10^{11} cm^{-2} eV^{-1} and 4.65 × 10^{17} cm^{-3} eV^{-1}, respectively [33].

Figure 5 compares the forward *I*–*V* characteristics of AlSiO/Ga_2O_3 MOSCAPs with or without PMA treatment. The *I*–*V* characteristics presents two distinguishable regions: region I of low-leakage operation identified by the leakage current below the detection limit current level (∼5 × 10^{-8} A cm^{-2}); and region II in which the gate leakage increases significantly until the gate bias approaches the avalanche breakdown. AlSiO with PMA at 300 °C extended the region of low-leakage operation from 0–3.7 MV cm^{-1} to 0–4 MV cm^{-1} compared with not-annealed samples. In addition, the average breakdown field strength was measured to be 8.2 MV cm^{-1} at average leakage current of 1 × 10^{-3} A cm^{-2} for AlSiO with PMA at 300 °C, which is higher than that of the underlying Ga_2O_3 and preferable for high power applications. No distinct improvement in low-leakage operation and breakdown strength were observed on sample with PMA at 350 °C. The results of lower-leakage operation and improved breakdown strength for AlSiO/Ga_2O_3 treated with PMA at 300 °C suggest a more reliable bulk dielectric with improved interface.

4. Conclusion

In summary, we studied the impact of PMA on the operational reliability of MOCVD-grown AlSiO/β-Ga_2O_3 (001) MOSCAPs. No significant change was observed between the sample with and without PMA treatment in forward *C*–*V* step-stress measurements. A distinct improvement in reverse operational stability (test reverse stress from −10 to −42 V) was

measured on AlSiO treated with PMA at 300 °C. In addition, the capacitance–voltage hysteresis and near-interface fast and slow traps were both suppressed by PMA at 300 °C. The low gate leakage region was extended from 3.7 MV cm^{-1} to 4 MV cm^{-1} and the breakdown strength was enhanced from 7.8 MV cm^{-1} to 8.2 MV cm^{-1} for AlSiO/β-Ga_2O_3 MOSCAPs treated with PMA at 300 °C compared with not-annealed samples. Reliable step-stress *C–V* performance, negligible hysteresis and reduced interfacial and bulk trap density achieved in this work demonstrate promising results for the improvements of MOS-based Ga_2O_3 devices.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

Acknowledgments

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ORCID iDs

Zhe Ashley Jian https://orcid.org/0000-0003-2182-4159
Subhajit Mohanty https://orcid.org/0000-0002-1469-5363
Wenjian Liu https://orcid.org/0000-0003-0483-649X
Elaheh Ahmadi https://orcid.org/0000-0002-8330-9366

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