A Low-Power Duty-Cycled Impulse-Radio Ultrawideband (IR-UWB) Transmitter with Bandwidth and Frequency Reconfigurability Scheme Designed in 180 nm CMOS Process

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***Abstract*—One of the design challenges of the implantable medical devices (IMD) is the power requirement that needs to be minimum to avoid frequent battery-replacement and surgeries. This paper presents a duty-cycled IR-UWB transmitter designed using standard 180 nm CMOS process that achieves an energy efficiency (energy-per-pulse) of 11.5 pJ/pulse at 100 Mbps data rate. Working in the frequency range of 4 - 6 GHz, the transmitter achieves a peak power spectral density (PSD) of -42.1 dBm/MHz with 950 MHz bandwidth which makes it highly suitable for high data rate biotelemetry applications. The bandwidth of the proposed transmitter system can also be varied from 500 MHz-950 MHz using control voltage of the impulse generator (IG). The wide frequency range and bandwidth range of the proposed transmitter also makes it highly suitable for distributed brain implant applications covering both lower and upper UWB frequency bands.**

***Index Terms*—IR-UWB transmitter, Voltage controlled oscillator, power amplifier, power spectral density, phase noise.**

I. Introduction

Implantable and wearable biomedical sensors have emerged as a promising research areas for advancing human healthcare technologies [1]. The wireless telemetry of biomedical sensors enables continuous health monitoring [2]. Implantable biomedical sensors and devices have a very stringent size and energy constraints. Thus, an energy-efficient transmitter module design is essential to increase the battery lifetime. Low-power communication systems like impulse radio ultrawideband (IR-UWB) transmitter is best suited for these types of sensor networks due to its low power consumption, high data-rate, low design complexity, and low-cost fabrication [3].

However, the transmitter needs to comply with the spectrum regulation imposed by the Federal Communication Commission (FCC) for UWB communication which requires the peak power spectral density to be lower than -41.3 dBm/MHz [4]. Modulation technique is one of the approaches that can be taken advantage of to meet the FCC mask regulation [5]. However, the addition of modulation circuitry increases the power consumption and complexity of the design architecture. Pulse-shaping filter [6], higher-order derivative circuit [7], and bi-phase modulation technique [8] are proposed in prior works to satisfy the FCC mask regulations. However, none of these techniques takes into account the frequency and bandwidth reconfigurability technique which gives flexibility to change the spectrum to be compliant with the FCC mask regulation. Moreover, the frequency reconfigurability technique helps transmitting data from the distributed neural implants and the bandwidth reconfigurability helps transmitting at various data rate. The higher-order derivative method in [7] is able to transmit at a high data rate of 100 Mbps while consuming 33 pJ/pulse. On the other hand, the bi-phase modulation consumes 12 pJ/pulse at 750 Mbps data rate [8]. Still, these techniques require complex circuitry. An IR-UWB transmitter architecture is proposed based on a gated oscillator with a switching pulse shaper in [9].

The proposed system consumes 13.4 pJ/pulse at 40 Mbps data rate. As the power consumption increases with the data rate, there is still some scope for achieving better performance, especially for high data rate applications, in terms of energy efficiency. To reduce the power consumption due to high data rate applications, duty-cycled radio is one of the popular choices.

For high data rate applications such as neural signal recording system for brain-computer interfacing, multiple channels ($>$100) are used to record and transmit data. A neural recording system presented in [10] shows a 128 channel system to transmit the recorded neural signal at 90 Mbps data rate which consumes 6 mW of power. If the number of channels or the sampling rate of the Analog to Digital Converter (ADC) increases, the data rate increases proportionally and as a result, the power consumption also increases. Thus, it is of utmost importance to reduce the power consumption/increase energy efficiency for such high data rate applications.

The novelty of this work is to design an energy-efficient differential cross-coupled LC Voltage Controlled Oscillator (VCO) along with a differential input class-C power amplifier

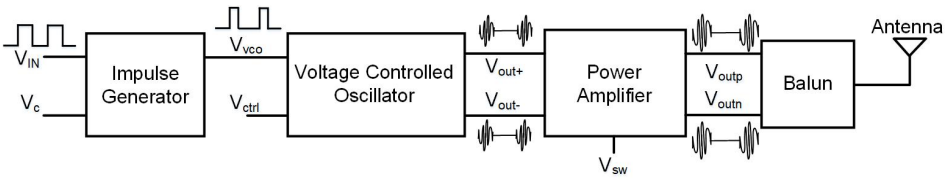

Fig. 1. Block diagram of a typical IR-UWB transmitter.

(PA) using 180 nm CMOS process for high data rate (>100 Mbps) applications. Moreover, the proposed system offers a voltage-controlled frequency and bandwidth reconfigurability feature that enables the transmitter to be used in both lower and upper UWB frequency bands and to be compliant with the FCC mask. Section II discusses the design architecture of the proposed impulse generator (IG), VCO, and PA circuitry. The simulation results are presented in section III which is then followed by a conclusion in section IV.

II. System overview

Fig. 1 shows the total system level block diagram of the proposed duty-cycled IR-UWB transmitter which includes an impulse generator, a VCO followed by a PA. The input of the impulse generator is the baseband digital data and the output is the corresponding impulse signal of a few ns of duration, which is typically used to switch on/switch off the VCO to make the transmitter duty-cycled. After the VCO, a PA or driver circuit is typically used to drive the 50 Ω antenna. The design architecture of the impulse generator, VCO and PA are described in the following sub-sections:

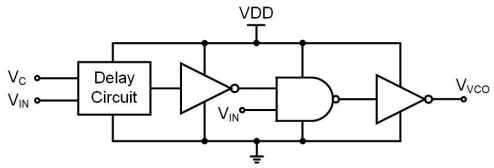

Fig. 2. Reconfigurable impulse generator.

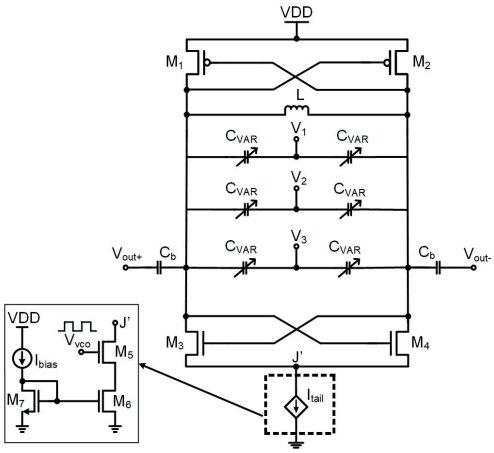

Fig. 3. Cross-coupled LC Voltage Controlled Oscillator.

A. Impulse Generator

The basic building block of the impulse generator is a tunable delay circuit, followed by an inverter, a NAND gate, and an inverter as shown in Fig. 2. The delay circuit is a current starved inverter where the delay can be controlled by changing the biasing voltage, V_c to change the pulse width of the impulse signal. The input signal, V_{in} is the digitized baseband neural signal. The frequency of the input signal depends on the sampling rate and the resolution of the analog-to-digital converters (ADC), which are typically 10 - 40 kbps and 8 - 10 bits for a single channel. The pulse width of the impulse generator can be changed to adjust the bandwidth which helps in achieving the FCC regulation compliance.

B. Voltage Controlled Oscillator

Ring oscillator is the most common and widely used VCO architecture that can be found in literature [11]. Even though the power consumption of the ring oscillator is lower compared to the LC oscillator, it shows a poor phase noise performance. On the other hand, LC oscillators are preferred due to their spectral purity [12]. The schematic of the proposed cross-coupled LC VCO is shown in Fig. 3. The oscillator is a complementary cross-coupled LC-VCO having two pMOS and two nMOS transistors. The sizing of the transistors and the LC tank is chosen in such a way that it satisfies the oscillation condition of the VCO,

$$G_m R > 1 \tag{1}$$

In equation (1), G_m is the total transconductance of the VCO and R is the loss resistance of the LC tank. The W/L ratio of the transistors M_1-M_2 and M_3-M_4 indicated in Fig. 3 are set in such a way that they operate in the strong inversion region to ensure high transconductance. To minimize the phase noise, transistor M_6 and M_7 are designed to operate in moderate inversion region, and M_5 is made to operate in the triode region to enable efficient switching and to minimize the leakage current. The detailed design parameters of the transistors of the VCO are shown in Table I.

The LC tank of the VCO includes an inductor, L of 2.26 nH, and three varactor pairs, C_{VAR} which are controlled by three voltage, V_1, V_2, and V_3. Three branches of varactor capacitors are used to cover a wide frequency range from 4 GHz to 6 GHz.

At the output of the VCO, a 250 fF DC blocking capacitor, C_b is also used to block the DC components of the generated RF signal. The tail current source of the VCO is actually a current mirror formed by transistor M_6 and M_7 (Fig. 3). To duty-cycle the VCO, the pulse signal generated by the impulse

TABLE I
TRANSISTOR PARAMETERS FOR THE VCO.

Transistor	W/L (μm)	g_m/I_d
M_5, M_6 (pMOS)	96/0.18	10
M_7, M_8 (nMOS)	36/0.18	12
M_9	96/0.18	1.03
M_{10}	96/0.18	16
M_{11}	6/0.18	16

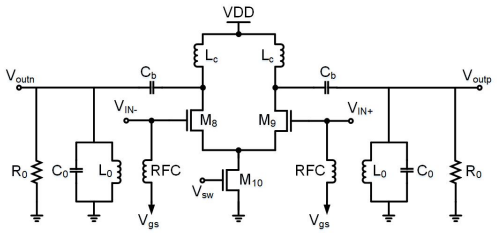

Fig. 4. Differential class C power amplifier.

generator is provided at the gate of the transistor M_5 that turns on and off the tail current source of the VCO. This enables the transmitter to turn on during the data transmission only, thus reducing the overall power consumption.

C. Power Amplifier

A class C PA is proposed for the IR-UWB transmitter. The reason for choosing the class C PA is to achieve a high efficiency with moderately low power. Fig. 4 shows the differential architecture of the class C PA which is able to achieve double the output compared to the single-ended PA. Here, two-transistor M_8 and M_9 are used to provide the differential input signals which are biased through RFC inductor using voltage, V_{gs}. A switching transistor, M_{10} is used to duty cycle the PA using an impulse signal, V_{sw} generated by the impulse generator. The output of the PA is connected to a 50 Ω load which is modeled as an RLC tank indicated by R_0, L_0, and C_0 in Fig. 4. In practical use, the output should be connected to a 50 Ω antenna.

III. SIMULATION RESULTS

The IR-UWB transmitter is simulated using the Cadence Virtuoso custom IC design tool and standard 180 nm CMOS process. The designed impulse generator is able to generate pulses with a wide range of pulse widths ranging from 1.5 ns to 20 ns by varying the control voltage of the delay circuit from 100 mV to 1.8 V. The supply voltage is set to be 1.8 V for all the circuit designed in this work. With the bias current of the VCO set to 35 μA, the tail current (Itail) is ∼560 μA which results in ∼1 mW of power consumption with 1.8 V supply voltage. The energy efficiency of the VCO is calculated to be ∼5 pJ/pulse for 100 Mbps data rate considering a 50% duty cycling.

The main purpose of the proposed LC VCO is to cover both the lower and upper UWB frequency bands. The combination of three control voltage (V_1, V_2, and V_3) is used to achieve one lower frequency and two upper frequencies in the UWB band. Fig. 5 shows the achieved frequency range of the VCO. The X-axis indicates the control voltage where V_1, V_2, and V_3

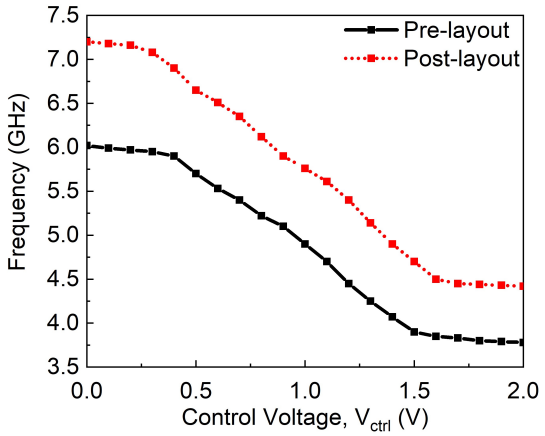

Fig. 5. Frequency range of the proposed transmitter over various control voltage where the value of V_{ctrl} is equal to V_1, V_2, and V_3. The solid line represents the pre-layout simulation results and the dotted line represents the post-layout simulation results.

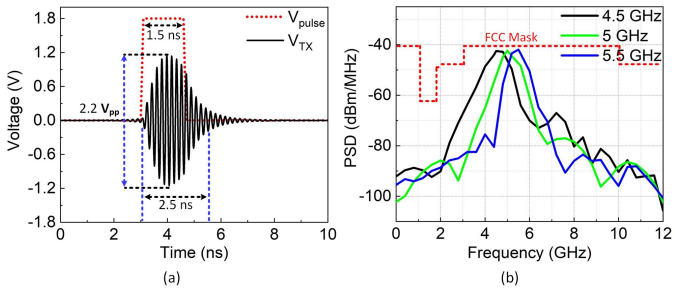

Fig. 6. (a) Generated pulse signal of the impulse generator (Red dotted line), and Output signal of the UWB transmitter (Black solid line), (b) Power spectral density of the UWB transmitter

use the same voltage level and represented as V_{ctrl}. Different combinations of three voltages can be used to fine-tune the frequency. According to the pre-layout simulation results, a linear range of frequency can be seen from 4 GHz to 5.8 GHz for the control voltage range of 0.5-1.5 V which can achieve 36.7% frequency range for the center frequency of 4.9 GHz. With a supply voltage of 1.8 V, the PA draws 2.3 mA current which results in power consumption of 4.14 mW. Fig. 5 also represents the post-layout simulation results for the frequency reconfigurability. The post-layout simulation shows frequency of the LC VCO varies from 4.5 GHz to 7 GHz for varying control voltage. The post-layout simulation shows a frequency range of ∼60% when the center frequency is 5.75 GHz. For the simulation of the IR-UWB transmitter, a voltage pulse train of 1.8 V with a frequency of 100 MHz and a pulse width of 1.5 ns, which is generated by the impulse generator, is used as input pulse signal of the PA. Fig 6(a) shows the generated pulse by the impulse generator (Red dotted line) and corresponding transmitter output signal (Black solid line), respectively. The energy efficiency of the PA is calculated to be 6.22 pJ/pulse for 1.5 ns pulse signal. As the power consumption of the impulse generator is negligible, the total energy efficiency of the transmitter is ∼11.5 pJ/pulse for 100 Mbps data rate. The corresponding power spectral density

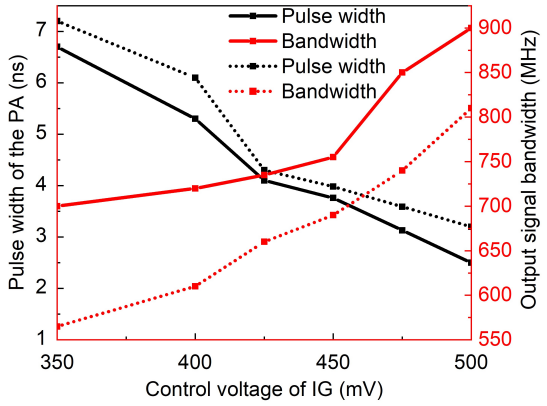

Fig. 7. Pulse width variation and output signal bandwidth variation for different control voltages of the IG. The solid line represents the pre-layout simulation results and the dotted line represents the post-layout simulation results.

(PSD) of the transmitter is simulated for the 2.5 ns window and shown in Fig. 6(b).

The figure shows PSD for three frequencies 4.5 GHz, 5 GHz, and 5.5 GHz where 4.5 GHz represents the lower UWB band and 5 GHz, and 5.5 GHz represent the upper UWB bands. For the differential output, a 3 dB higher PSD will be achieved, which would still be lower than the FCC mask regulation of -41.3 dBm/MHz. The PSD plot shows the peak amplitude value of -42.5 dBm/MHz, -42.3 dBm/Hz, and -41.9 dBm/MHz for 4.5 GHz, 5 GHz, and 5.5 GHz, respectively. The bandwidth of the 4.5 GHz, 5 GHz, and 5.5 GHz is simulated to be 1 GHz, 900 MHz, and 850 MHz, respectively. Fig. 7 shows bandwidth reconfigurability and pulse width of the PA for the pre-layout (solid line) and post-layout (dotted line) results of the 5 GHz transmitted signal. The output signal bandwidth changes with the change in pulse width of the PA which changes with the control voltage of the IG. The pulse width of the PA ranges from 2.65 ns to 6.7 ns and 3.2 ns to 7.2 ns, for pre-layout and post-layout simulation, respectively. According to the post-layout simulation results, the bandwidth varies from 560 MHz to 810 MHz for the control voltage range of 350 mV to 500 mV. A bandwidth variation from 710 MHz to 900 MHz is observed in pre-layout simulation for varying control voltage of IG. A comparison with the prior published works is shown in Table II with the expected results for the proposed work. The proposed system works in both UWB bands (3.1 - 6 GHz) with frequency and bandwidth reconfigurability feature whereas the prior works only operate in higher UWB band. The frequency and bandwidth reconfigurability of the proposed transmitter makes it a better candidate compared to the other state-of-the-arts to transmit data from the distributed neural implants.

IV. Conclusion

For high data rate applications like a neural signal recording system where multiple channels (>100) are used for data acquisition and transmission, reducing the overall power consumption for such an application is of utmost importance. This paper presents a duty-cycled IR-UWB transmitter that has a very low energy efficiency for high data rate (e.g. 100 Mbps or higher) compared to the other state-of-the-art works making it highly suitable for energy-constrained biomedical sensor applications. Moreover, the use of both lower and upper UWB frequency bands enable the system to transmit data recorded from different areas of the brain. The future work includes the measurement of the fabricated transmitter chip.

TABLE II
Comparison with Other Works

Reference	[5]	[8]	[9]	This work
Technology (nm)	90	130	110	180
Frequency band (GHz)	6-10	6-10	6-10	3.1-10
Maximum output voltage (mV_{pp})	324	120	300	780
Pulse repetition frequency (MHz)	25	750	40	100
Energy efficiency (pJ/pulse)	268 at 25 Mbps	12 at 750 Mbps	13.4 at 40 Mbps	11.5 at 100 Mbps
Maximum PSD (dBm/Hz)	-53 at 8 GHz	-45 at 8 GHz	-41.5 at 8 GHz	-42.1 at 5.5 GHz

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