A Low-Power Front-End with Compressive sensing Circuit for Neural Signal Acquisition Designed in 180 nm CMOS Process

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***Abstract*—Multi-channel data acquisition of bio-signals is a promising technology that is being used in many fields these days. Compressed sensing (CS) is an innovative approach of signal processing that facilitates sub-Nyquist processing of bio-signals such as an electrocardiogram (ECG) and electroencephalogram (EEG). This strategy can be used to lower the data rate to realize ultra low power performance, As the count of recording channels increase, data volume is increased resulting in impermissible transmitting power. In this paper, the implementation of a CMOS based front-end design for CS using standard 180 nm technology is presented. A novel pseudo-random sequence generator is proposed, which consists of two different types of D flip-flops that are used for obtaining a completely random sequence. The power consumed by the bio-signal amplifier block is 277 μW. The SAR-ADC block that is designed to digitize the amplified signal consumes 2.35 μW of power and the power consumption value of pseudo-random bit sequence generator (PRBS) is 546 μW. The low power consumption per channel confirms the importance of the proposed approach for multiple channel high-density neural interfaces.**

***Index Terms*—Compressive sensing, Pseudo random sequence generator, LFSR, Pseudo Random sampling, Sub-Nyquist Sampling.**

I. Introduction

Compressive sensing (CS) as the name suggests, is an approach of the acquisition of the data itself that is implemented in an efficient and compressive way. The signals can be interpreted sparsely or in a compressible way, Based on signals that are sparsed, The compressed sensing method lets us sample the Signals at a much lower rate than that of the conventional sampling rate that is suggested by the Nyquist sampling theory [1].

CS lets the original signal to be faithfully reconstructed back from the pseudo-randomly sampled signal which needs far fewer data bits when compared to the signal sampled using the conventional Nyquist sampling approach.In the applications specifically in domains where there are high data rates and low-power constraints CS can play important role in performing the tasks efficiently. For example, in the medical imaging domain, the speed or the data rate is the highest priority. In the circuit implementation of the data compression of the physiological signals such as EEG, ECG [2], low power consumption is considered as the highest priority. While other strong survey articles are available in CS literature [3], [4]. CS strategy is used in many biomedical applications such as signal processing of bio-signals, efficient neural signal acquisition, genomic sensing, and bacterial composition reconstruction. Here, in this paper, the application of neural signal acquisition based on CS is emphasized.

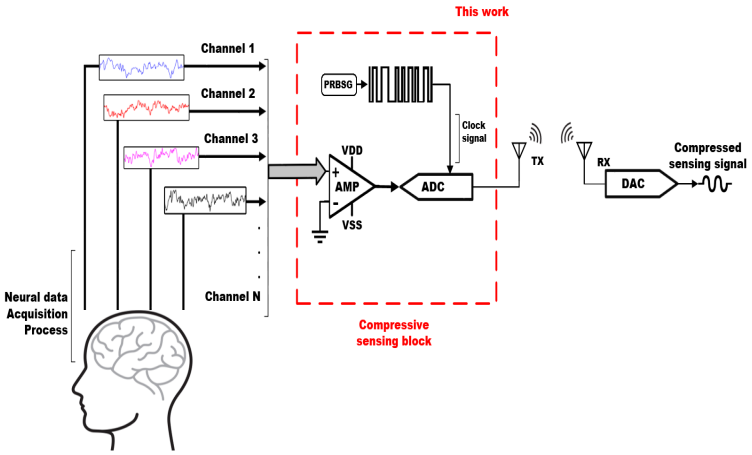


Figure 1: Proposed CS-based neural signal acquisition system.

II. Compressed sensing methodology

A. Primary objective

The chief objective of our work is to implement a CMOS based circuit which can compressively acquire the EEG/ ECG data without actually losing the essence of the original data. This CS strategy results in the reduced amount of data needed for transmission and thus results in reduction in the power required for data transmission.

B. Conventional CS Methodologies

The method of detection of spikes based on the threshold values [5] is commonly used for compression of data of bio-signals based on activity parameters. It transmits the spike-activity signal segments while omitting the segments of signal

that wont involve any essential spike activity. The threshold crossing detection method is the most common spike detection method. However, this approach retains the spike's shape While discarding the inter-spike signal, which involves undetected spikes and other significant neural voltage variations. As the research scholars are interested in the analysis of the entire neural signal, this compression approach can not be used.
The nearly lossless alternative of the wavelet transform based compression approach which involves the off-chip transmission of only the important coefficients values of wavelet after the signals are converted into their wavelet representations using an on-chip circuit. Wavelet transform systems allow for impressive compression rates, thus ensuring excellent efficiency for the signal reconstruction [6]. However, in terms of the power and area consumption, wavelet transformation based on the ASIC implementation is insignificant as it involves the digital filter implementation and memories that are on-chip running at faster rate than the Nyquist sampling rate.

The conventional multi-channel compressive sensing (MCS) architecture has many problems, For Instance, the need for analog to digital converter (ADC) with high resolution. [7] Improving the conventional MCS architecture, there is another architecture consisting of a block of multiple inputs with single output compressive sensing (MISOCS) which utilises the methodology to embed data present in all channels into each sample of the compressed signal. [8].

Proceeding further in improving this CS system architecture, there is another methodology that involves implementing an optimized neural signal recording system for wireless compressed sensing [9], [10]. The system benefits from both integrated circuits which are custom and compatible wireless solutions. An wireless system-on-chip (SoC) which is implantable and an external relay which is wireless based are involved in their proposed system. Another approach in implementing the CS is involved in the design of a system-on-chip (SoC) CS current sensor using bipolar 0.16 μm CMOS-DMOS technology. For the data rate reduction, two current sensing cores which are broadband, each constitutes of a 9-bit ADC and Hall-effect probe are integrated together monolithically with a multiple mode digital compressive sensing encoder (DCSE) [8], [11].

III. Design Architecture

Even though all the previously proposed methodologies are achieving the improvement in the compressed sensing performance [12], however low power consumption criteria have been compromised to significant level. Thus, we have proposed a simple and novel CS system design block giving the highest priority to the low power consumption criteria. To address the problem of high power consumption in a multi-channel neural data acquisition system, a new CS system is proposed. In this proposed design, unlike the conventional CS strategy [13] where the input analog signal is multiplied with a random sequence using a Gilbert multiplier which alone consumes 10 mW power with a supply of 1.8 V, we have proposed a new strategy, that is to use this random sequence as a clock to the ADC block and feed the analog neural data signal as input directly to the ADC. The proposed approach is also presented in Fig.1, the entire proposed CS system consumes the total power of 825.35 μm which is significantly less amount when compared to the power consumed by Gilbert multiplier [14] alone in the conventional methodology. The individual sub-blocks that are involved in the proposed CS system are discussed in the upcoming sub-sections III-A, III-B, III-C respectively.

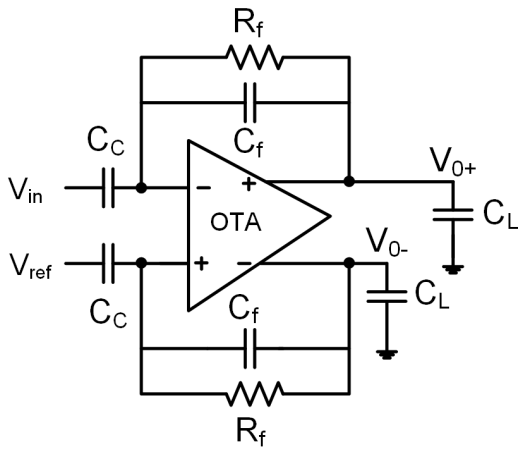


Figure 2: Schematic of the closed-loop amplifier.

A. Neural amplifier

This paper presents a fully-differential neural amplifier with a capacitive-resistive feedback network [15]. A folded-cascode (FC) architecture is used as the operational transconductance amplifier (OTA) [16]. The FC-OTA which achieves wider swing in the signal along with high gain is presented in this paper. The complete amplifier schematic with the closed-loop is presented in Fig.2. The reference input of the amplifier uses the reference neural electrode data. Two DC-blocking

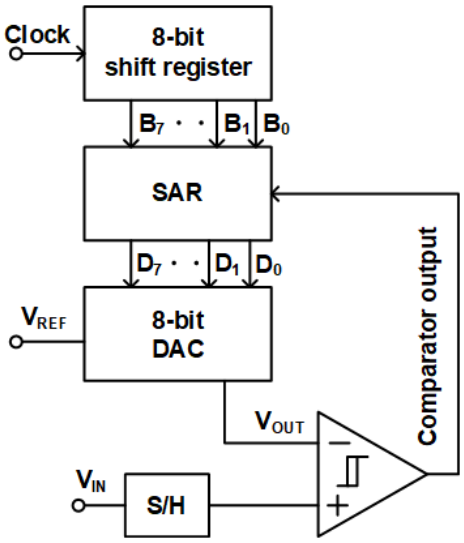


Figure 3: SAR-ADC block diagram.

capacitors are connected to each of the inputs to block the DC component from the inputs. This amplifier design gives enhanced performance in terms of gain-bandwidth (GBW). The neural amplifier achieves a gain of 50.3 dB within the neural signal bandwidth of 0.1 Hz - 5 kHz.

B. ADC

To digitize the amplified version of input neural data from the designed amplifier, a successive approximation register analog-to-digital converter (SAR-ADC) is designed in the 180 nm CMOS process [16]. The block diagram of the SAR-ADC is shown in Fig.3. It consists of the 8-bit shift register, SAR logic block, DAC (digital-to-analog converter), and a dynamic comparator. This SAR-ADC has a sampling rate ranging from 10 to 40 kHz and consumes a 277 μW of power.

C. Pseudo random bit sequence (PRBS) generator block

Even before designing the PRBS block, we ask ourselves the following questions: Can we generate a long random bit sequence without compromising the low power criteria? Can this random bit sequence be generated using fewer components when compared to conventional methods that involve complex design blocks? [17] The conventional way to implement the pseudo-random bit sequence (PRBS) generator is to use 14 D-flip flops, 2 xors, and one Mux [18]. As this method involves more number of register blocks (D-flip flops) resulting in a significant increase in power consumption, we have proposed a simple PRBS block through efficient usage of components. The Proposed pseudo-random bit sequence topology consists of two different types of D-flip flops which are responsible to attain a high data rate simultaneously satisfying the low-power and low area constraints. Two extended genuinely single-phase clock (E-GSPC) logic dependent D-flip flops are used to shorten the critical path delay and thus boost the data rate. The power consumption value of pseudo-random bit sequence generator (PRBS) is 546 μW at 1.8-V VDD including the clock buffer. The E-GSPC, GSPC D-flip flops along with an XOR and buffer constitutes to form the proposed PRBS generator block. An XOR gate is used to maintain the randomness of the generated bit sequence and a feedback loop is used for the repetition of the random signal sequence. Unlike the conventional methods where 14 D-flip flops, 2 XOR's, and one Mux are used to generate random bit sequence [18], this proposed PRBS block is simply built with just 7 D-flip flops, XOR, and a buffer. There is a possibility of dynamic flip flops losing their states when the PRBS block is made to run with a slow sequence rate. So, while designing the PRBS block we made sure that there is no loss of the state in D-flip flops.

IV. Simulation Results

A previously recorded neural signal as shown in Fig.10a, whose maximum amplitude is 4 mV is imported in the Cadence Virtuoso Custom IC design tool to be used as an input to the amplifier. The resultant amplified version of the neural signal has its peak amplitude as 0.96 V. The mid-band gain of the designed amplifier is 50.3 dB.

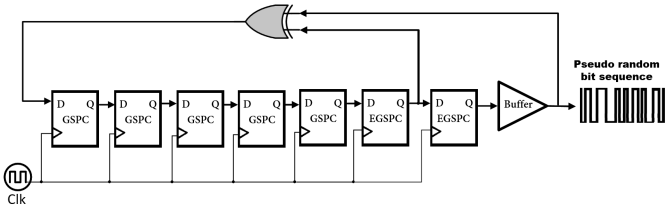


Figure 4: Pseudo random bit sequence block.

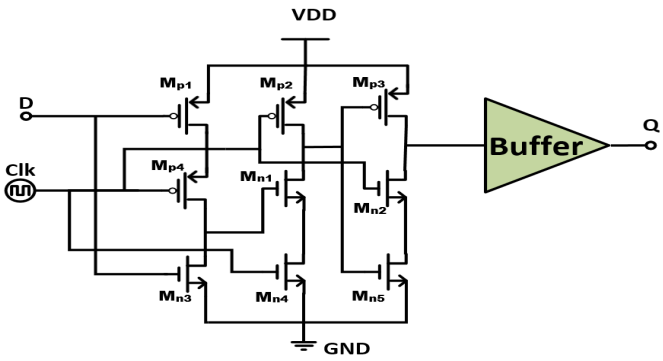


Figure 5: Schematic of Genuinely Single-phased clock dependent D-flip flop.

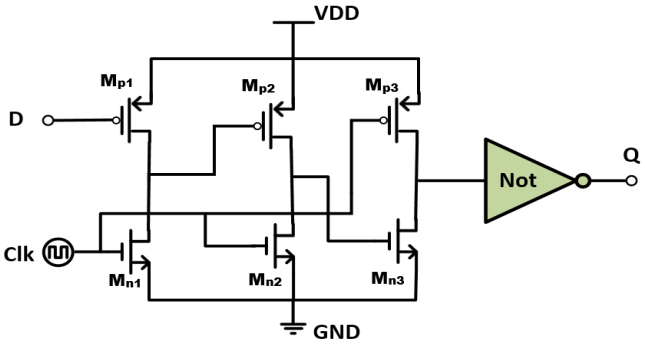
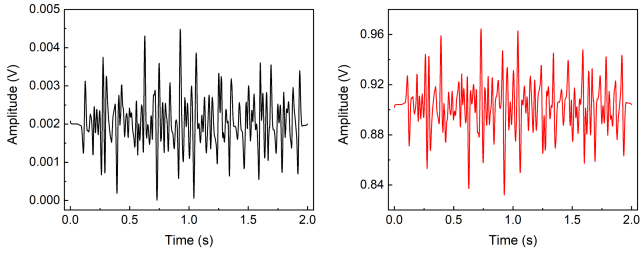


Figure 6: Schematic of Extended Genuinely Single-phased clock dependent D-flip flop.



(a) Input neural signal (b) Amplified neural signal

Figure 7: Simulation results of the proposed neural amplifier

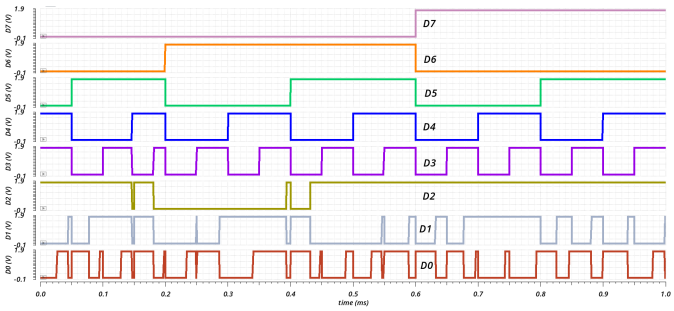


Figure 8: Simulation results of the ADC.

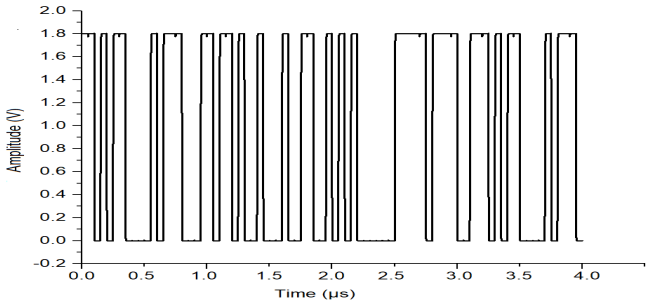


Figure 9: Output of the PRBS block.

In this paper, we have considered collecting neural data from the 32 channels, each sampled at 20 KS/s with an 8-bit SAR-ADC, making the total data rate of 32×20 K×8. The analog neural data from one channel among the 32 channels is considered and its equivalent digitized version with the 8-bit resolution is presented in Fig.8.

The amplitude of this PRBS is 1.8 V. A transient run for 4 μ-sec time-frame is done and the output of the proposed pseudo-random bit sequence generator is shown in Fig.9. To verify the quality of reconstruction of the original signal from the compressively sensed signal, the digitized output data is given as an input to Ideal ADC and the corresponding reconstructed signal is presented in Fig. 10b.

The output of SAR-ADC is reconstructed using an Ideal DAC (digital to analog converter) in LabVIEW (Laboratory Virtual Instrument Engineering Workbench) software and the resultant output is presented in Fig. 10b.

V. Conclusion

This paper proposes the design of a novel compressed sensing system which is implemented using 180 nm CMOS technology. The highest priority is given to the low power consumption of the proposed novel CS system design. The proposed CS-based neural acquisition system needs 825.35 μW of power, the performance and power consumption results show the significance of the proposed approach.

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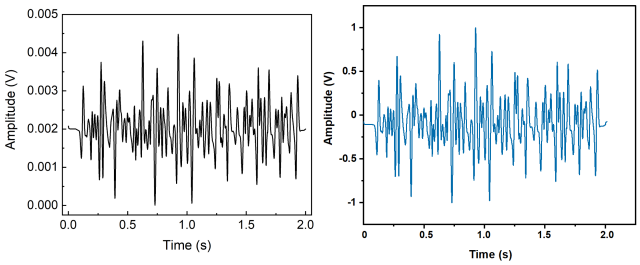

(a) Original neural signal (b) Reconstructed signal.

Figure 10: Comparision between original and reconstructed signal.

Table I: Comparision among previous works

Parameters	Comparision of works		
	Tsung [19]	***O.U Khan [20]***	***This Work***
CMOS Technology	180nm	180nm	180nm
Signal type	ECG	Sinusoidal signal	Neural
Compression methodology	Algorithm based	CS	CS
No. of channels	2	NA	32
Sampling rate	90 MHz	1.2 GHz	10 to 40 kHz
Power consumption	6.7 mW	11.2 mW	825.35 μW

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