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Voltage-dependency Effect of Through-silicon Vias on the Power Distribution Network

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Abstract

This paper analyzes the effect of voltage-dependent (power/ground) P/G through-silicon vias (TSVs) on the power distribution network (PDN) impedance of high bandwidth memory (HBM) systems. First, the voltage-dependent behavior of TSV structures is discussed and the equivalent capacitance range of power/ground (P/G) TSV arrays with different patterns and quantities are compared. A hierarchical PDN model for HBM systems including printed circuit board (PCB) PDN, package, and on-chip PDN with different P/G TSV arrays, is proposed to model the PDN impedance affected by the voltage dependence of the P/G TSV arrays.

Author(s) Biography

Wei Zhang received the B.S. degree in electronic information engineering, Central South University in 2014, and received the M.S. degree in electronic science and technology, Beihang University in 2017. Currently, she is a PhD student in EMC laboratory, Missouri university of Science and Technology. Her research interests are measurement and analysis in system EMI, RFI and 3D IC TSV technology.

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Bo Pu is a visiting assistant research professor of Electromagnetic Compatibility (EMC) Lab and National Science Foundation (NSF) Industry/University Cooperative Research Center for EMC at Missouri University of Science and Technology, Rolla, MO, USA. His research interests include the design methodology for chip-package-PCB systems in areas of signal/power integrity and EMC. He recently focuses on the research of high-speed integrated circuits system up to 224 Gbps, 2.5D Si-interposer for high bandwidth memory (HBM), and 3D IC integration. He holds 10 patents about high-speed links and 2.5D/3D ICs. From 2015 to 2020, he was a Staff Engineer with Foundry Business, Semiconductor R&D Division of Samsung Electronics, Hwaseong, Korea. Dr. Pu received the B.S. degree in electrical engineering from Harbin Institute of Technology, China, in 2009, and the Ph.D. degree in electronic and electrical engineering from Sungkyunkwan University, South Korea, in 2015. He was the recipient of Best Student Paper Award as first author at the IEEE APEMC 2011, a Young Scientists Award from the International Union of Radio Science (URSI) in 2014, and the 2019 Distinguish reviewer for IEEE Transactions on EMC. He also obtained Ph.D. Fellowship Award in 2013, Best Innovation Award,

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Excellent Performance Award, and Excellent Project Award as the first awardee in 2015-2019 from Samsung Electronics for his outstanding contributions. He was as a Session Chair in IEEE APEMC 2017, IEEE EMC+SIPI 2020, and a TPC Member of the Joint IEEE EMCS & APEMC 2018. He is currently an Associate Editor for IEEE Access as well as the IEEE senior member.

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Introduction

The JEDEC standards [1] [2] have specified the details of high bandwidth memory (HBM) systems. In HBM systems, through-silicon vias (TSVs) provide short vertical interconnections between stacks of dynamic random-access memory (DRAM) chips. Under DC bias conditions, the metal-oxide-semiconductor (MOS) structure of the TSV can form a depletion region between silicon oxide (SiO2) and silicon (Si), resulting in a bias-dependent capacitance of the depletion layer [3] – [8]. In power distribution networks (PDNs), this bias-dependent capacitance will significantly affect the low-frequency behavior (below 1 GHz) of the PDN impedance when the number of power/ground (P/G) TSVs is sufficiently large. This situation may become worse when the power supply voltage decreases and the power consumption of the chip increases. Therefore, voltage dependent PDN modeling and evaluation of various P/G TSV patterns or quantities are necessary in the design stage of the PDN in HBM systems to predict the accurate PDN impedance and reduce the PDN impedance below the target impedance.

The modeling of the system PDN has been extensively investigated. In [9], a physics-based approach to extract the equivalent circuit of the system PDN from PCB to the chip was discussed. For 3D ICs and packaging, Green's function-based method in [10] can be used to extract the PDN impedance with multi-dielectric layers. For the P/G grids of the interposer and on-chip PDN of 3D ICs with TSVs, the calculation of the capacitance, inductance, and resistance on the unit cell of the P/G grid and TSVs has been discussed and equivalent circuit models have been proposed for fast prediction of PDN impedance [11] – [15].

In this work, the bias-dependent effect on the low-frequency capacitive behavior of a single TSV is investigated. Furthermore, the total bias-dependent capacitance of P/G TSV arrays with different patterns and quantities is investigated. Then, to investigate the effect of the voltage-dependent capacitance of P/G TSVs on PDN impedance of HBM systems, a hierarchical PDN model is developed including PCB and package, Si interposer, and on-chip PDN with voltage-dependent P/G TSV array. Based on the system PDN model, the influence of bias voltage on the system PDN is analyzed in both frequency and time domains.

The following content of this paper is divided into three parts. First, an extraction method for the bias-dependent equivalent capacitance of P/G TSVs is presented, including the influence of patterns and the number of P/G TSVs in an array. Then, a circuit model for hierarchical PDN from PCB to on-die PDN with P/G TSVs is developed. Finally, the influence of the voltage-dependency effect of TSVs on the PDN impedance and voltage ripple in the power rail is studied. The potential problems of the system PDN caused by the voltage-dependency effect of TSVs are discussed and mitigation methods are proposed.

Equivalent capacitance extraction of P/G TSVs

P/G TSVs in HBM systems provide short vertical interconnections between the multi-layer PDNs in the stacked dies. The MOS structure of a TSV will provide a voltage-dependent capacitive effect due to the depletion region that forms between the oxide layer and silicon layer when a bias voltage is applied to the TSV structure. This capacitance significantly affects the low frequency (below 1 GHz) behavior of the PDN impedance, especially when the number of P/G TSVs is sufficiently large. In this section, the hysteresis

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of the equivalent capacitance with the bias voltage for a TSV structure is discussed first. Then, the total bias-dependent equivalent capacitance for P/G TSV arrays is investigated under different patterns and numbers of the P/G TSV array according to the P/G pin maps recommended in the JEDEC standard for the HBM system.

TSV equivalent capacitance vs. bias voltage

Fig.1 shows a TSV structure with silicon (Si) substrate and its equivalent circuit [4]. Since the TSV is a MOS structure, it should be noted that when a bias voltage is applied to the power (PWR) TSV, a depletion region could be formed between the SiO2 layer and Si layer. The width of the depletion region depends on the bias voltage and thus the capacitance formed in the depletion region depends on the bias voltage. The total capacitance caused by the SiO2 layer and depletion layer dominates the low-frequency behavior of the coupling between TSV and other structures.

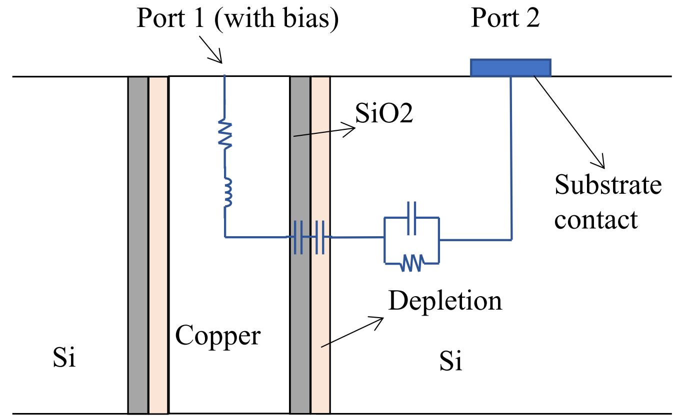

Fig.1 TSV structure and depletion region.

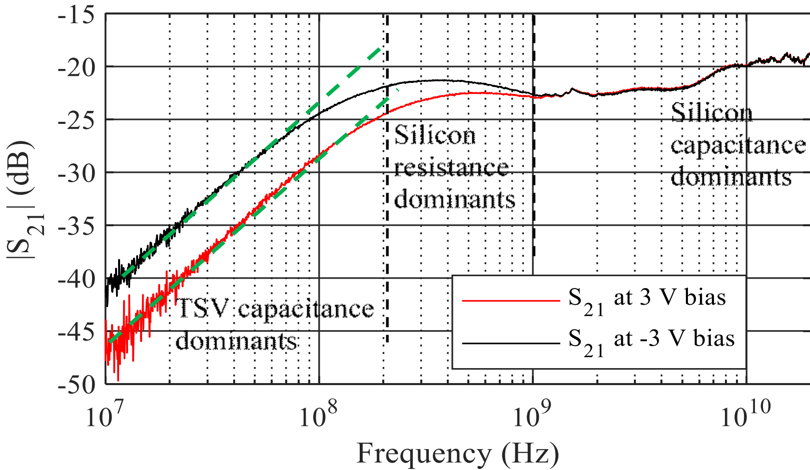

Fig.2 Measured coupling ($|S_{21}|$) between a single TSV and Si substrate contact under +3 V and –3 V bias voltages.

For the coupling between a TSV structure and the Si substrate contact, Fig. 2 shows the measured S_{21} under the bias voltage of +3 V and -3 V applied to the TSV. The dimensions

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of the TSV structure are shown in TABLE I. Due to the short length of TSV (80 um), the equivalent resistance and inductance show a negligible effect on S_{21} in the frequency below 200 MHz. According to the equivalent circuit model of the TSV-substrate structure in Fig. 1, the TSV equivalent capacitance caused by the series connection of the capacitance between the SiO2 layer and depletion layer dominates the total coupling below 200 MHz. The resistance caused by the Si substrate dominates the total coupling in 200 MHz – 1 GHz. And the capacitance of the Si substrate dominates the total coupling above 1 GHz.

TABLE I Dimensions of the TSV structure

Parameters	Description	Value
H_{TSV}	Height of TSV	80 μm
tox	Thickness of the SiO2 layer	0.23 μm
R_{TSV}	Radius of the TSV copper	14.65 μm
ε_{SiO2}	Relative permittivity of SiO2	4.1
ε_{Si}	Relative permittivity of Si	11.9
σ_{Si}	Conductivity of Si	10 S/m

The hysteresis curve of the low-frequency equivalent TSV capacitance vs. bias voltage is shown in Fig. 3 [4]. For the TSV structure studied in this paper, the equivalent TSV capacitance varies between 1280 fF and 677 fF with the bias voltage changes between + 3 V and -3 V. The low-frequency equivalent TSV capacitance is also affected by the thickness of the SiO2 layer since it is a series connection of the SiO2 layer and the depletion layer capacitance. The bias-dependency effect is only caused by different widths of the depletion layer corresponding to the varying bias voltages.

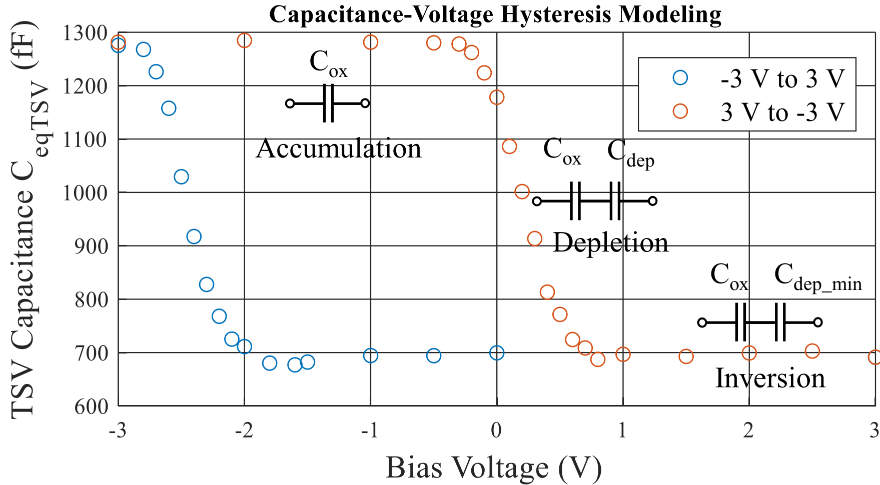

Fig. 3 Hysteresis of low-frequency equivalent TSV capacitance vs. bias voltage.

Since the voltage-dependent effect of equivalent TSV capacitance affects the low-frequency electrical characteristics, it needs to be considered during the pre-design of an HBM system in terms of power integrity (PI) analysis when a large number of power TSVs are present.

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Estimation of low-frequency equivalent capacitance of TSV array in HBM systems

HBM system

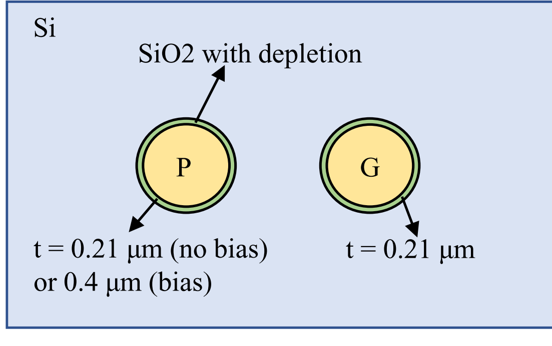
In JEDEC standards such as JESD235B, the core supply voltage (VDDC) of a HBM IC is recommended in the range of 1.14 V – 1.26 V with a typical value of 1.2 V. The maximum rated DC voltage of VDDC is -0.3 V – 1.5 V. Therefore, when the HBM system is powered up or down, the TSV capacitance will change accordingly. According to the specification in the JESD235B, 2 – 12 layers of DRAM dies/chips can be stacked in the 3D IC. From the recommended micro-bump array and the ballout footprint of the VDDC net, it is roughly estimated that the number of P/G TSV pairs in one DRAM die can be greater than 880.

To estimate the total capacitance induced by the TSV array in an HBM system in the low-frequency range, the patterns and number of TSVs were investigated in estimating the total capacitance of the TSV array.

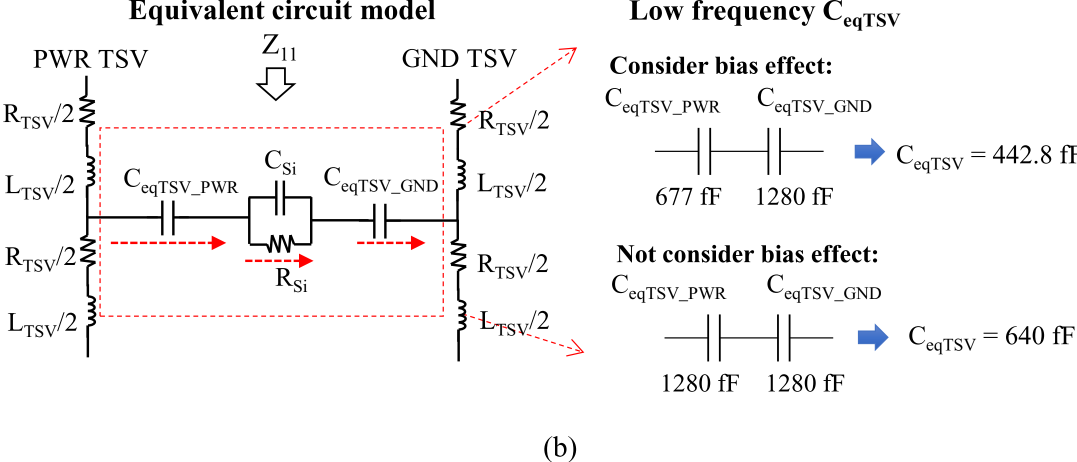
Low-frequency equivalent capacitance of different TSV patterns and number of TSVs

In practical applications, different P/G TSV patterns may exist for vertical connections between different layers of P/G grids. The equivalent capacitance of different TSV patterns is investigated, such as the P/G TSV pair, GPG TSV pair, GGPGG TSV pair, and so on. As an example, the equivalent capacitance of the P/G TSV pattern is extracted for cross-validation using various methods including, Q2D, circuit model from the analytical calculation, and HFSS.

To simplify the modeling, the capacitance in the depletion region is converted to an extra thickness of the SiO2 layer. Therefore, for the total TSV capacitance with a variation of 1280 fF – 677 fF caused by the bias voltage between -0.3 V and 1.2 V, the corresponding equivalent thickness of SiO2 layer (t_{oxe}) is 0.21 μm – 0.4 μm, where the TSV height, TSV radius, SiO2 property, and Si property are shown in TABLE I. Since a voltage of 0 V is applied to the ground TSVs, the effective thickness of the SiO2 layer in the simulation model is set as 0.21 μm, which provides an equivalent TSV capacitance of 1280 fF contributed from SiO2 layer without any depletion effect.



(a)



(b)

Fig. 4 P/G TSV pair and the corresponding equivalent circuit model. (a) PG TSV pair; (b) Equivalent circuit model.

Fig. 4 shows an example of the equivalent capacitance extracted from a single PG TSV pair. Since in the low-frequency range (< 200 MHz), the Si substrate exhibits only the resistive effect (R_{Si}), the low-frequency equivalent capacitance of the P/G TSV pair is formed by the series connection of the equivalent capacitance (C_{TSV_PWR}) of the power (PWR) TSV and the equivalent capacitance (C_{TSV_GND}) of the ground (GND) TSV. As the bias voltage changes from -0.3 V to 1.2 V (corresponding t_{oxe} in the simulation model from 0.21 μm to 0.4 μm), the C_{TSV_PWR} changes from 1280 fF to 677 fF, while the C_{TSV_GND} remains constant as 1280 fF (the corresponding t_{oxe} in the simulation model remains the same as 0.21 μm). A comparison of the low-frequency equivalent capacitance of this structure extracted from different methods is shown in TABLE II.

TABLE II Extracted TSV capaciatnce for different single PG TSV pair

C_{eq} (fF)	Q2D	Circuit model	HFSS
Not consider depletion effect/1.2 V bias	641.1	640.0	642.6
Consider depletion effect/1.2 V bias	443.3	442.8	443.8

To further understand the effect of bias-dependent TSV capacitance on the low-frequency behavior of the coupling from TSV to the other structures, the E-field distribution at 1 MHz of the TSV region is analyzed in Fig. 5. A constant E field exists between the PWR TSV and the Si substrate, and between the GND TSV and Si substrate in the low-frequency range. Therefore, the Si substrate shows a conductive behavior (with very small R_{Si}) at low frequencies, which is consistent with the behavior of the equivalent circuit model in Fig. 5 (b).

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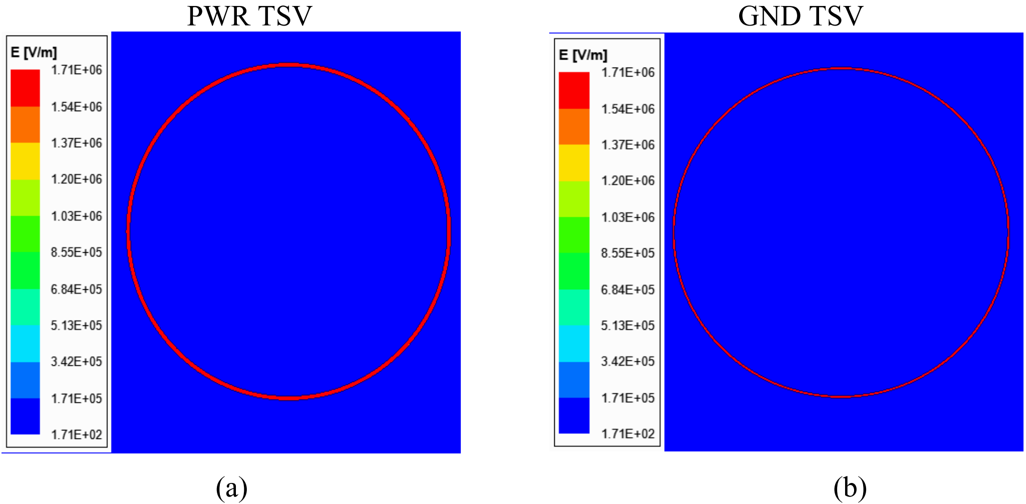

Fig. 5 E field in the SiO2 layer and Si substrate at 1 MHz. (a) E field distribution in PWR TSV region; (b) E field distribution in GND TSV region

The models of the PWR and GND TSV arrays for other patterns are shown in Fig. 6. Based on the E-field distribution between the PWR TSVs, the Si substrate, and GND TSVs, the low-frequency equivalent capacitance of the TSV array in the MHz range can be calculated from the series capacitance between the PWR TSVs and the Si substrate, and between the GND TSVs and the Si substrate. Therefore, the locations or patterns of the PWR and GND TSVs do not affect the total capacitance of the TSV array in low frequency, but the number of PWR and GND TSVs will determine the total capacitance. A simple equation to estimate the low-frequency equivalent capacitance of the P/G TSV array is shown in (1):

$$C_{eqTSV} = \frac{1}{\dfrac{1}{N_{GNDTSV} \cdot C_{GNDTSV}} + \dfrac{1}{N_{PWRTSV} \cdot C_{PWRTSV}}} \tag{1}$$

Where the parameters in (1) are described in TABLE III.

TABLE III Description of parameters in (1)

Parameters	Description
C_{eqTSV}	Low-frequency equivalent capacitance of P/G TSV array
N_{GNDTSV}	Number of GND TSVs
C_{GNDTSV}	Equivalent capacitance of each GND TSV
N_{PWRTSV}	Number of PWR TSVs
C_{PWRTSV}	Equivalent capacitance of each PWR TSV

To validate the proposed equation (1), the extracted capacitance from Q2D and (1) for the patterns in Fig. 6 are compared in TABLE IV.

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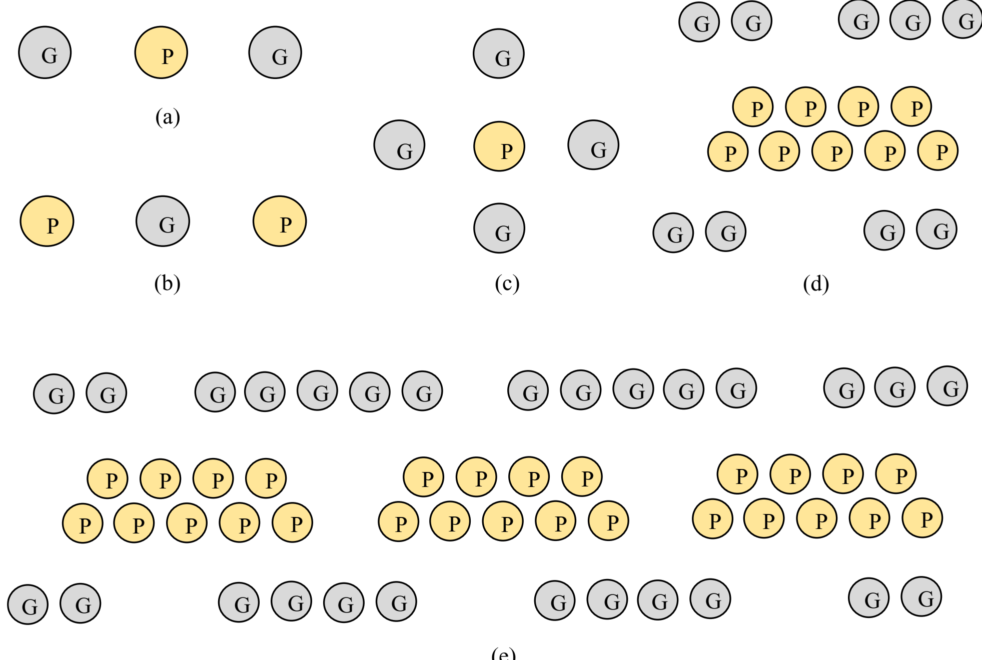

Fig. 6 Patterns (simplified illustration) of P/G TSV array studied. (a) GPG TSVs; (b) PGP TSVs; (c) P/G TSV array 1; (d) P/G TSV array 2; (e) P/G TSV array 3.

TABLE IV Extracted TSV capacitance for different TSV patterns

Patterns in Fig. 6	C_{eqTSV}	**Q2D**	**Equation (1)**
(a)	Not consider depletion/1.2 V bias	854.82 fF	853.33 fF
	Consider depletion/1.2 V bias	535.89 fF	535.41 fF
(b)	Not consider depletion/1.2 V bias	854.83 fF	853.33 fF
	Consider depletion/1.2 V bias	658.78 fF	657.98 fF
(c)	Not consider depletion/1.2 V bias	1025.80 fF	1024.00 fF
	Consider depletion/1.2 V bias	598.41 fF	597.90 fF
(d)	Not consider depletion/1.2 V bias	5.77 pF	5.76 pF
	Consider depletion/1.2 V bias	3.99 pF	3.99 pF
(e)	Not consider depletion/1.2 V bias	17.31 pF	17.28 pF
	Consider depletion/1.2 V bias	11.97 pF	11.96 pF

TABLE V Extracted TSV capaciatnce for TSV arrays in 3 D IC

Bias of PWR TSV \ $C_{totalTSV}$ **(nF)**		**2 layer**	**4 layer**	**8 layer**	**12 layer**
Not consider depletion effect/1.2 V bias	C_{PWRTSV} = 1280 fF C_{GNDTSV} = 1280 fF	1.54	3.07	6.14	9.22
Consider 1.2 V bias	C_{PWRTSV} = 677 fF C_{GNDTSV} = 1280 fF	1.06	2.13	4.25	6.38

Therefore, for HBM 3D ICs with 2 – 12 DRAM die layers, if there are 1200 TSV pairs per DRAM die, the total equivalent capacitance caused by the SiO2 layer of the PWR and GND TSVs, and the depletion layer of the PWR TSVs can be estimated in TABLE V when a bias voltage is applied. It is noted that the total low-frequency capacitance

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generated by the on-die P/G TSV array is in the nF range, which can play an important role in on-die decoupling techniques. However, the bias voltage may shift the total capacitance of the TSV array to a smaller value, which is unavoidable. Therefore, in the following sections, the influence of TSV bias-dependency on the system PDN impedance is investigated, which needs to be considered in the power integrity (PI) analysis of such systems with 3D IC TSV technology.

PDN extraction for HBM systems with 3D IC

In this section, a hierarchical PDN model is built, including PCB and package, Si interposer PDN, and on-die PDN with TSVs. The PCB and package PDN are extracted from measurement on an actual graphic card with HBM2 GPU memory. The Si interposer PDN and on-die PDN are extracted by simulation. This hierarchical PDN model is used to evaluate the impact of bias dependence of on-die P/G TSVs on the system PDN impedance.

PCB and package PDN of a graphic card

Fig. 7 shows a commercial graphic card including AMD Radeon RX Vega 56 GPU with HBM 2 memory. This graphic card is used for PDN impedance measurement. As the impedance of the PDN is very low for a commercial product, the two-port measurement method is used [16].

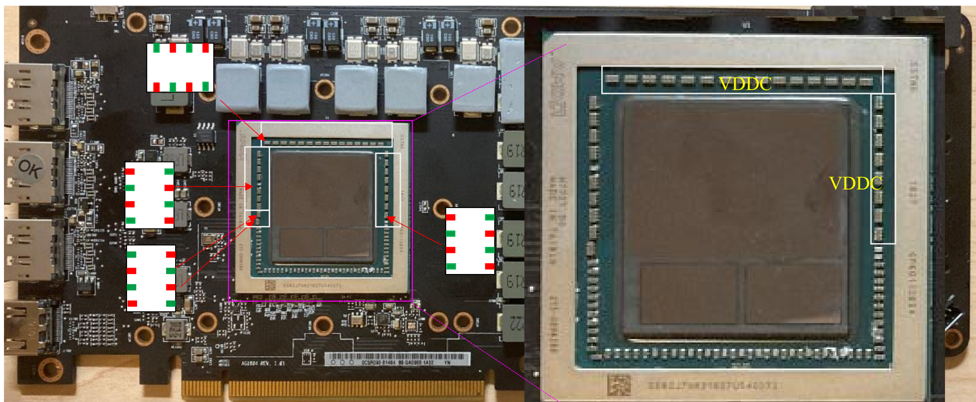

Fig. 7 Photo of a graphic card.

The PDN impedance of the power supply for the core (VDDC) net can be extracted from the measured S_{21} using (2):

$$Z_{DUT} = 25\frac{S_{21}}{1-S_{21}} \tag{2}$$

Two on-package decoupling capacitors were removed for probe landing. Since the IC is not removed, the measured impedance up to the 200 MHz range is used as the impedance caused by the PCB and package. The setup is shown in Fig. 8 (a), and the equivalent circuit model extracted from the PDN impedance is shown in Fig. 8 (b). The comparison between the measured and simulated impedance curves is shown in Fig. 8 (c). The measured PDN curve shows a very low value of PDN impedance which is due to a large number of decoupling capacitors mounted on the PCB.

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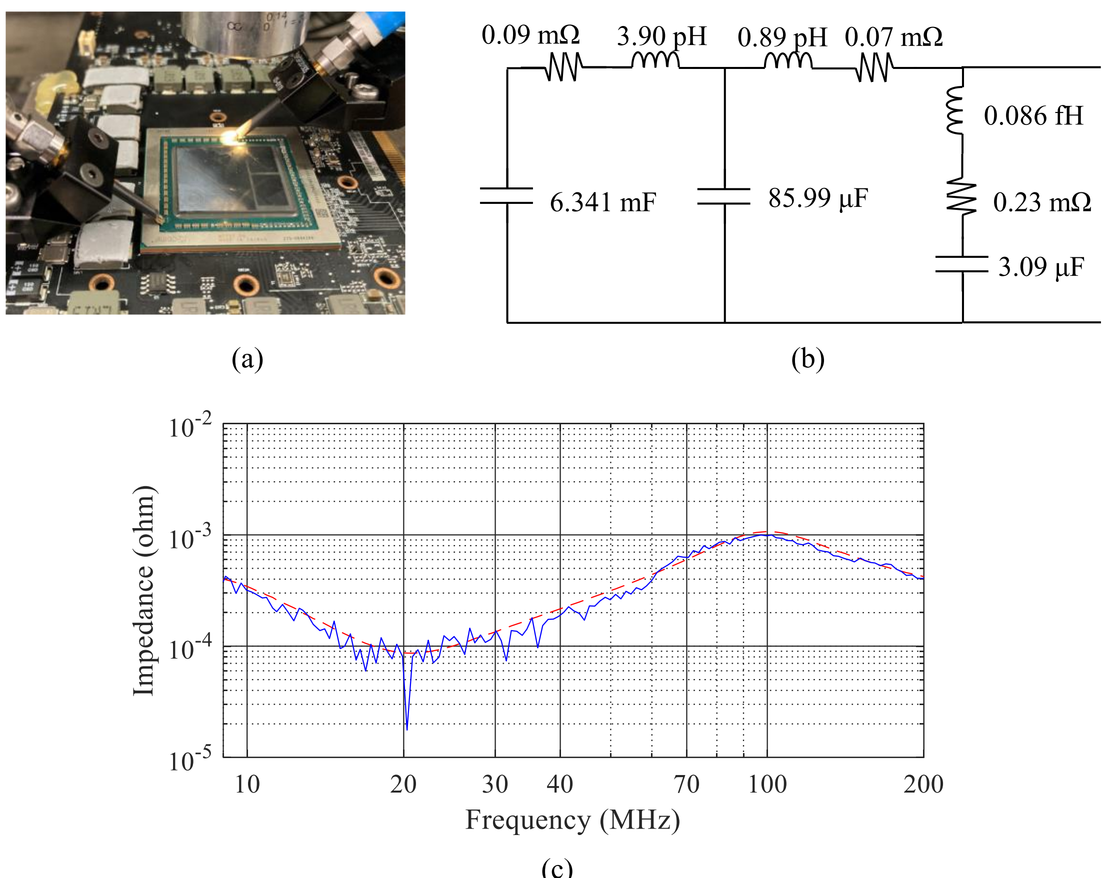

Fig. 8 PDN measurement setup and results. (a) Measurement setup; (b) Equivalent circuit model; (c) PDN impedance (Z_{11}) from measurement and equivalent circuit simulation model.

On-die and silicon interposer PDN modeling

Power and ground (P/G) grids are typically used for on-die and silicon interposer PDN. As the integration size of the 3D IC increases, the width of the single P/G bar will keep reducing and the metal density for the P/G grid will keep increasing, which results in much more time and complexity when using the 3D full-wave model for PDN impedance simulation. Therefore, the equivalent circuit model is widely applied for the simulation of on-die and silicon interposer PDN with high density and large area.

The P/G grid is divided into repeated unit cells. The method of extracting the unit cell parameters from the analytical equation is introduced in [14] and [17].

Fig. 9 shows the structure of a P/G grid. It contains two layers of traces with vertical interconnections of the same net between each layer. In the top layer, the P/G traces are in the Y direction. In the bottom layer, the P/G traces are in the X direction. The dimensions of the P/G grid traces are shown in TABLE VI. The metal density for the PDN used is 30%.

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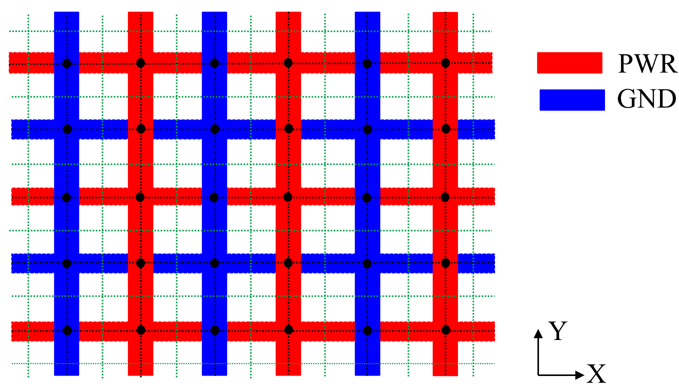

Fig. 9 P/G grid and unit cells

TABLE VI Dimensions of the P/G grid

Parameter	Description	Value
W	Width of the P/G trace	10 μm
L	Length of the P/G trace between the near 2 nodes	60 μm
T1	Thickness of the P/G trace in the top layer	0.76 μm
T2	Thickness of the P/G trace in the bottom layer	0.76 μm
td	Gap between the P/G trace between the top and bottom layer	0.8 μm

The distributed circuit model based on the distributed equivalent circuit method is used for the P/G grid. The segmentation for the P/G grid is shown in Fig. 9. The nodes (black dots in Fig. 9) are defined at the crossing region between each two orthogonal P/G traces in one layer, where equivalent capacitances are defined. A capacitance (C_{PWR_GND}) is defined between the upper and lower nodes with the same position in the XY plane if they are of different nets. Besides, a capacitance (C_{self}) is defined at each node, which is the intrinsic capacitance (self-capacitance) between the trace and the ground at an infinite distance. A branch segment is formed between the two adjacent nodes on the same plane, where the self-inductance (L_{self}) and resistance (Rs) are defined. The black dot lines in Fig. 9 describe the trace branches for segments of inductance and resistance. Moreover, capacitance and mutual inductance are defined between two parallel traces in the same layer. The extracted lumped terms are shown in TABLE VII for each node, trace segment, and between the adjacent trace segments.

Modified nodal analysis (MNA) is used with MATLAB to solve the voltage at each interconnect node and the current through each branch in the distributed equivalent circuit model. Therefore, the impedance of the P/G grid can be solved quickly when there is a large number of segments, which is much faster than the commercial 3D solvers.

Fig. 10 shows the PDN impedance of 20 × 20 segments (1.2 mm × 1.2 mm) extracted from the equivalent distributed circuit model and HFSS. Good agreement with the 3D commercial solver validates the accuracy of the distributed equivalent circuit model.

In this paper, the length of the P/G trace between the near 2 nodes (L) is set as 30 um and other parameters are the same as TABLE V, which has the metal density as 55.6%; the size of the on-die PDN is 3 mm × 3 mm and the size of the silicon interposer is 36 mm × 28 mm. The extracted impedance curves for a 1-layer on-die PDN with 6 mm × 6mm and the interposer PDN with 36 mm × 28 mm are shown in Fig. 11.

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TABLE VII Comparison of parameters extracted from analytical equation and Q3D

Parameters	C_{self}	C_{PWR_GND}	L_{self}	R_s	$C_{Parallel}$	L_{mutual}
Equation calculation	———	9.4771 fF	34.92 pH	0.169+ 0.033i Ω	1.525 fF	-5.606 pH
Q3D simulation	1.6 fF	9.58 fF	33.76 pH	0.136+ 0.048 Ω	1.36 fF	-5.64 pH

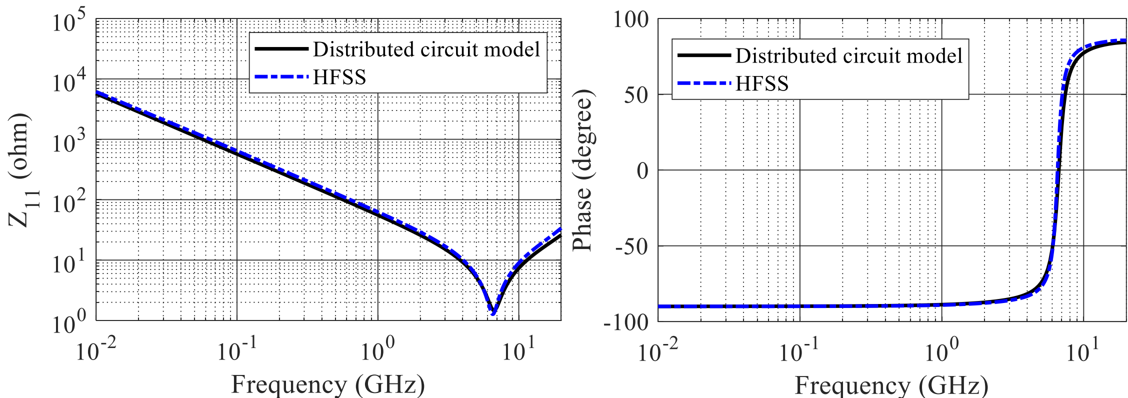

Fig. 10 Comparison of P/G grid impedance between the distributed circuit model and HFSS.

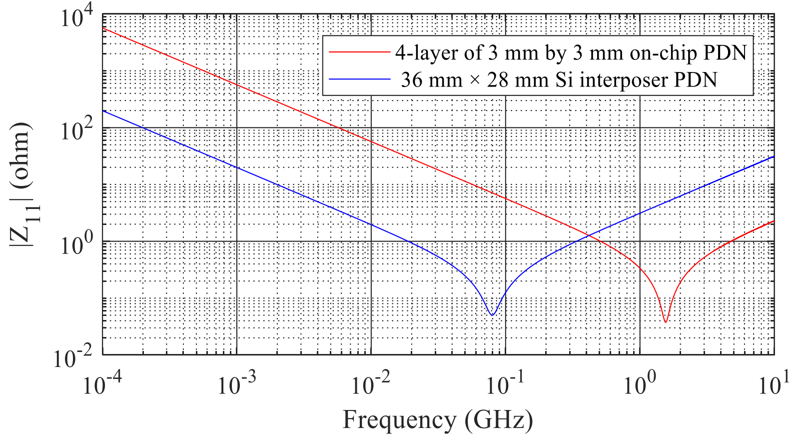

Fig. 11 Impedance of a 1-layer 6 mm × 6 mm on-die PDN and 36 mm × 28 mm Si interposer.

Effect of bias-dependent P/G TSV on the system PDN and mitigation methods

Based on the extracted PDN model from PCB to the on-die P/G TSV array, the hierarchical equivalent circuit model of system PDN is built, as shown in Fig. 10. It is under the assumption that there are 4 layers of DRAM dies with 1200 pairs of P/G TSVs in each layer, the on-die P/G grid size is 6 mm × 6 mm for each layer, and the P/G grid in

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the Si interposer is 36 mm × 28 mm. The hierarchical PDN circuit model built in this paper and the system PDN impedance extracted is assumed to be extracted by looking at the PDN from the top layer of the DRAM die into the system. It is noted that the circuit model could be different if extracted from other DRAM layers such as the bottom DRAM layer.

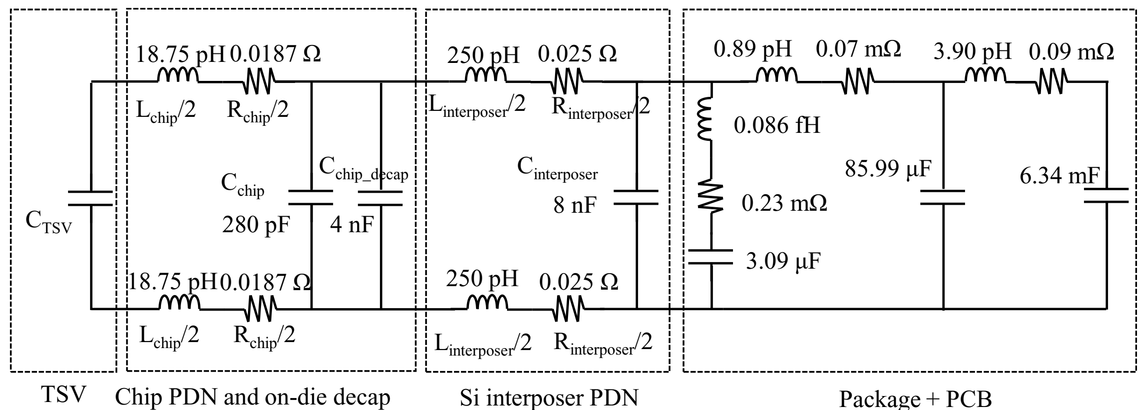


Fig. 10 Hierarchical PDN model from PCB to on-die PDN with TSV.

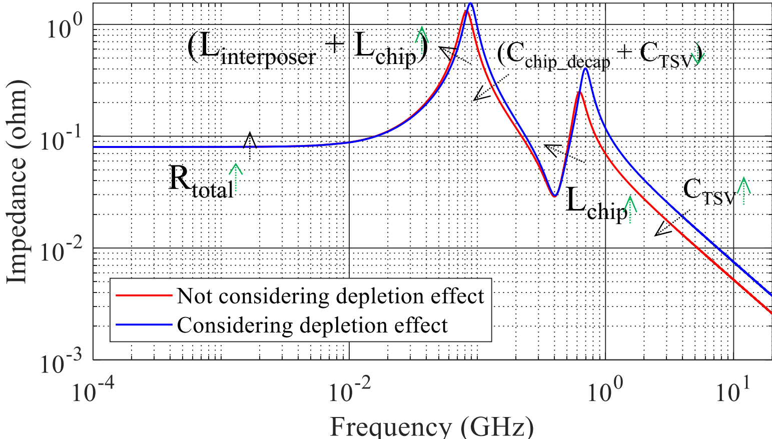


Fig. 11 Effect of the bias-voltage-dependent TSV capacitance on the system PDN.

The model is used to investigate the influence of bias voltage on the system PDN impedance. As shown in Fig. 11, when no depletion effect is considered, two resonances at 82.1 MHz and 629.1 MHz are generated by the capacitance of the TSV P/G array and the inductance of the P/G grid of the multilayer die and the Si interposer. The first resonance at 82.1 MHz is caused by the total inductance of the Si interposer and on-die PDN, and the total capacitance of the TSV array and the on-chip decoupling capacitor. The second resonance at 629.1 MHz is caused by the inductance of the on-chip PDN and the capacitance of the TSV array.

When a bias voltage of 1.2 V is applied, the total capacitance of the P/G TSV array changes from 3.07 nF to 2.13 nF, causing the resonance from 82.1 MHz and 629.1 MHz to shift to 89.1 MHz and 705.1 MHz, respectively.

Information Classification: General

These resonances caused by the capacitance of the P/G TSV array, the on-chip decoupling capacitors, the inductance of the interposer, and the on-chip PDN can cause severe problems to the supply voltage of the system when a signal is operating near the resonance frequencies in the 3D IC.

Time-domain simulation

The voltage of the power supply rail in the PDN network will generate ripples due to the transient switching current of the IC and the impedance of the PDN. In the time-domain simulation of the PDN model as shown in Fig. 12, we investigated the voltage ripple under a certain switching current profile. The noise in the power supply is set to 100 MHz with the rising and falling edges are set as 200 ps and 400 ps, respectively. The maximum current consumption is assumed as 1 A [18] [19]. The voltage ripple is simulated for the system PDN model with 4 layers of DRAM dies (shown in Fig. 10).

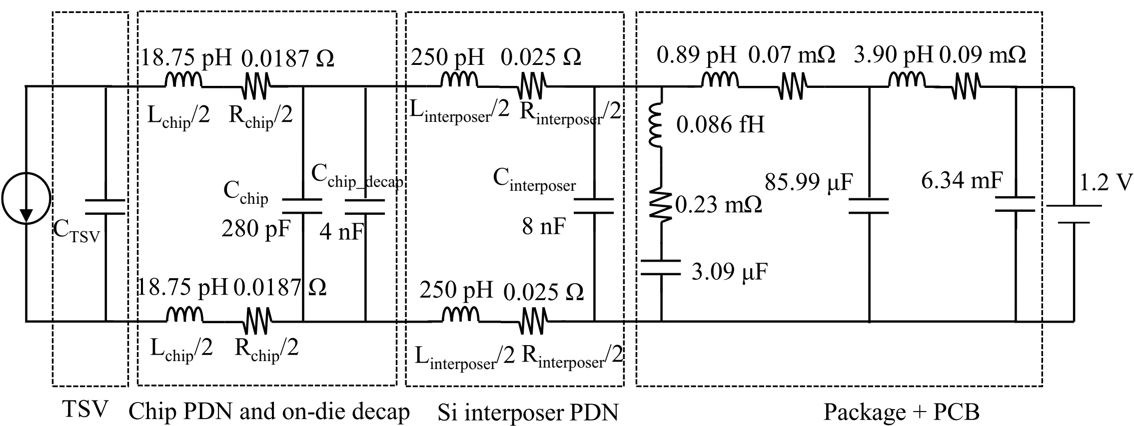


Fig. 12 Circuit model for simulating the power switching noise in time domain.

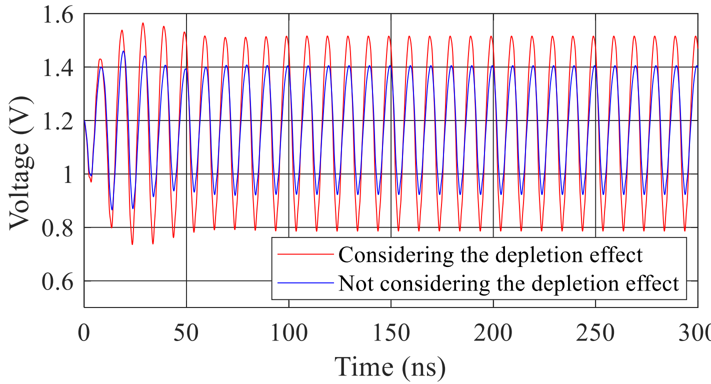


Fig. 13 Time domain waveform of the supply voltage (Vdd - Vss) in power rail considering and not considering the 1.2 V bias effect on the total capacitance of P/G TSVs.

As shown in Fig. 13, two cases are compared: (1) without considering the bias-dependent effect of the TSV arrays; (2) with considering the depletion/bias-dependent effect of the TSV arrays. For the system PDN model with 4-layer DRAM and specific I/O

current characteristics, a maximum voltage difference of 177mV can be observed between considering and not considering the depletion/bias-dependency effect of TSV arrays. Therefore, taking into account the bias-dependent effect of the TSV array is critical for the PDN design of the HBM system with 3D ICs and TSVs.

Due to the noise in the power supply network, power supply induced jitter (PSIJ) can be a potential issue. As shown in Fig. 14, an inverter model is created to investigate the induced jitter by the power supply noise. The data rate for the input of the inverter is set as 1.60001 Gbps with 50 ps rising and falling time. The load of the output of the inverter is set as 10 pF. Three cases were compared: 1) no power supply noise applied; 2) power supply noise without considering the P/G TSV bias effect; 3) power supply noise considering the P/G TSV bias effect. Fig. 15 shows the simulated eye diagrams and the calculated parameters from the eye diagram are compared in TABLE VIII.

Therefore, when adding power supply noise, the deterministic jitter increases in the output signal. Besides, when considering the bias effect of the P/G TSV in the PDN, the power supply induced jitter also increases, which is non-negligible during the SI and PI design of the HBM system.

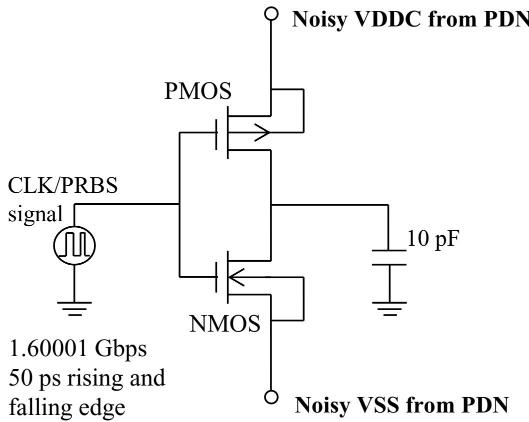
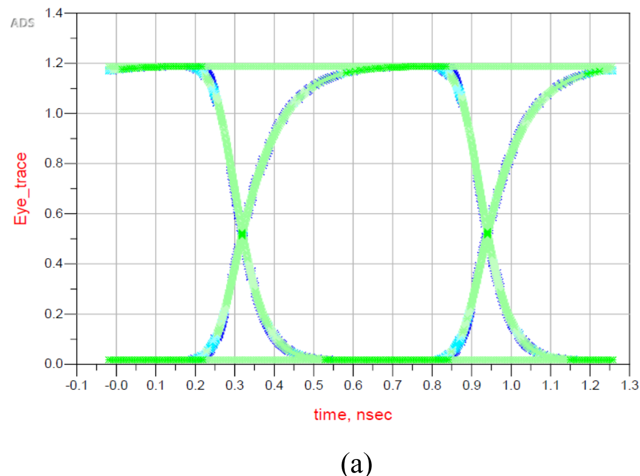


Fig. 14 Inverter model for PSIJ simulation.



(a)

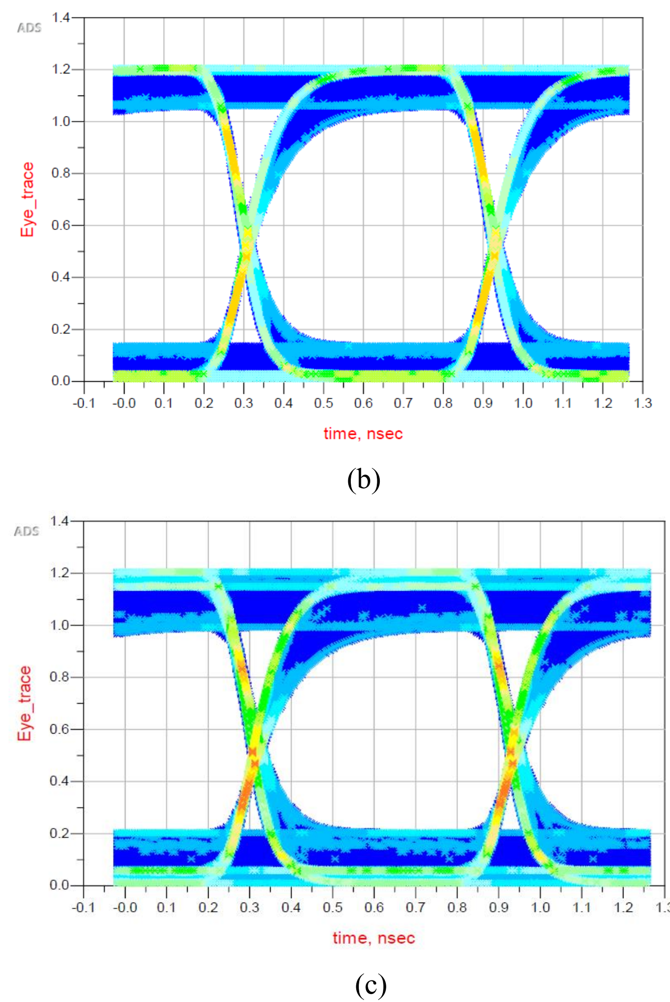


Fig. 15 Eye diagram of different cases of output signal. (a) Case 1: without the power supply noise; (b) Case 2: with power supply noise, not considering the bias effect; (c) Case 3: with power supply noise, considering the bias effect.

TABLE VIII Parameters extracted from eye diagram

	Eye height	Eye width	Peak-peak jitter
Case1	1.136 V	0.603 ns	5.677 ps
Case2	0.878 V	0.599 ns	22.708 ps
Case3	0.744 V	0.588ns	31.223 ps

Mitigation method

Besides, the resonances of the PDN impedance caused by the capacitance of the TSV array and the inductance of the on-die and Si interposer PDN is playing an important role in creating the large voltage ripples in the power rail. Mitigation methods should be considered to reduce such ripples.

To reduce the resonance on the system PDN impedance, the possible methods are:

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- Reducing the inductance of Si interposer PDN ($L_{interposer}$), which can be achieved by reducing the size of Si interposer PDN.
- Reducing the inductance of on-chip PDN (L_{chip}), which can be achieved by reducing the size of on-chip PDN or increasing the layers of on-chip PDN.
- Increasing the number or value of the on-chip decoupling capacitor. However, this method is not efficient due to the limitation of areas in the 3D IC for on-chip decoupling capacitors. Besides, the capacitance of on-chip capacitors only affects the first resonance.
- Increasing the number of TSVs in the 3D IC, which is effective to reduce both resonances in the PDN impedance.

Fig. 16 shows a comparison of the impedance of the system PDN with 4-layers dies and 8-layer dies under 1.2 V bias voltage. It can be seen when adding multiple layers of on-die PDN, the system impedance could be reduced at the resonances due to the inductances of Si interposer and on-die PDN, and the capacitances from the TSV array and on-die decoupling capacitors. Correspondingly, Fig. 17 shows the voltage ripple in the power rail from the system PDN model of 4-layer and 8-layer DRAM die. The voltage ripple in the power rail is significantly reduced when more DRAM dies are used while keeping the metal density the same. Similar to Fig. 15, the eye diagram of the output signal of the inverter with the P/G noise is shown in Fig. 18, which is interfered by the P/G noise from

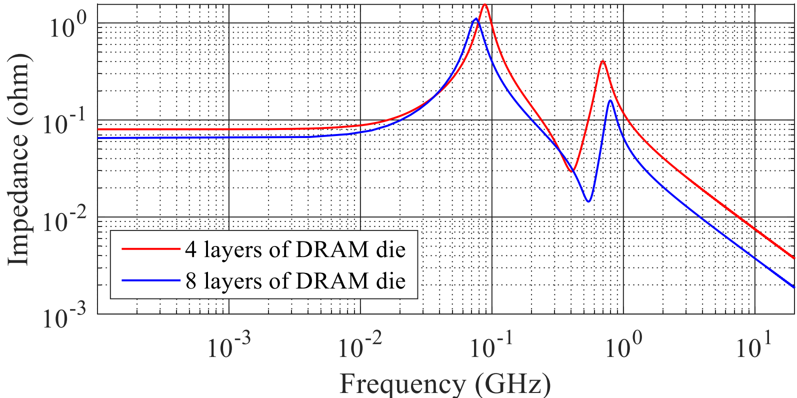

Fig. 16 Effect of the number of DRAM die layers on the system PDN.

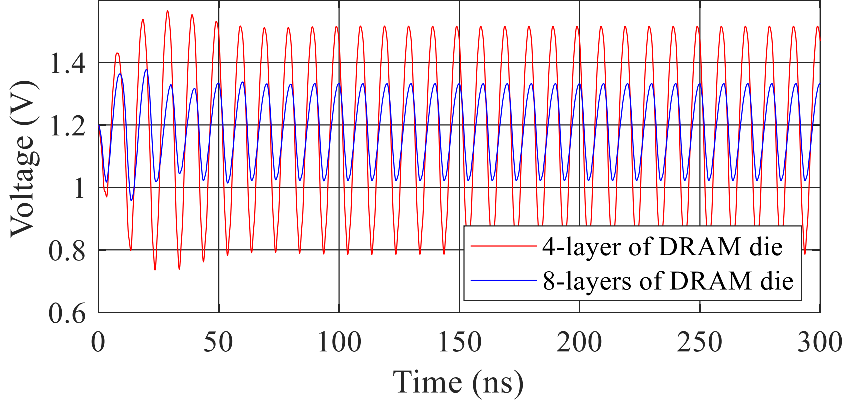

Fig. 17 Time domain: Effect of the number of DRAM die layers on the power rail of PDN.

Information Classification: General

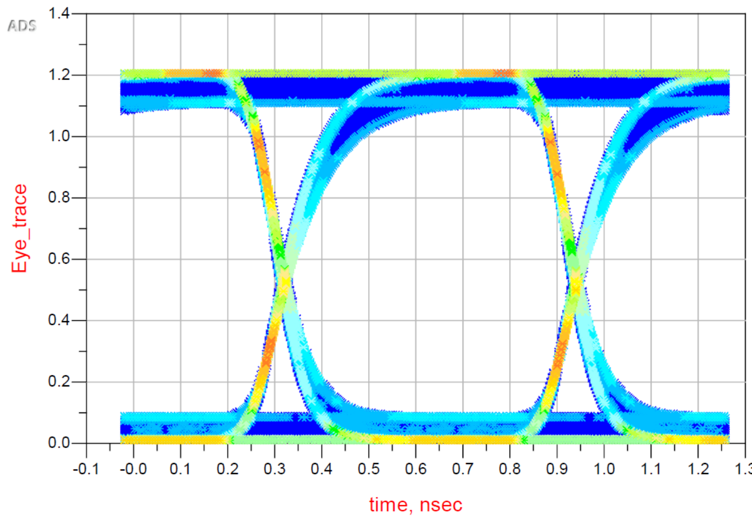

Fig. 18 Eye diagram of output signal from an inverter considering the power supply noise from 8-layer DRAM dies in an HBM system.

the HBM system with 8-layer DRAM in the 3D IC. The calculated eye height and width are 0.983 V, 0.600 ns, respectively. The peak-peak jitter is calculated as 17.31 ps.

Discussions - How industry can benefit?

Since the equivalent capacitances of the P/G TSV array are in the nF range, they can be considered as additional decoupling capacitors in the pre-design stage of the 3D IC or HBM system. Assuming that the Z_{11} of the PDN is extracted from the top layer of the DRAM die into the system PDN, two main effects should be considered when more layers of DRAM die are designed in an 3D IC: 1) the number of P/G TSVs will increase, causing a larger equivalent total capacitance of the P/G TSV array; 2) the total equivalent inductance and resistance of the DRAM layers will decrease. Therefore, the number/value of on-chip decoupling capacitors can be further reduced if more DRAM layers are to be stacked in the 3D IC in the future.

TABLE IX shows 3 scenarios to study the system PDN impedance curve with different DRAM layers and values of on-chip decoupling capacitors. The corresponding PDN impedance curve is shown in Fig. 19. When the on-chip decoupling capacitor is 4 nF and the 4 layers of DRAM die are changed to 8 layers, the maximal PDN impedance decreases from 1.54 Ω to 1.13 Ω. Moreover, the maximum PDN impedance for 8 layers of DRAM die with the total on-chip decoupling capacitor of 1 nF reaches the same value as that for 4 layers of DRAM die with the total on-chip decoupling capacitor of 4 nF.

By taking advantage of the decoupling effect offered by the P/G TSV arrays, the industry can significantly reduce the cost of incorporating a large number of on-chip decoupling capacitors in a compact 3D IC. However, this method is only beneficial in PDN design including 3D IC with power/ground TSVs and is not preferred for signal/ground TSVs because the additional TSV capacitance causes larger RC delays for the high-speed signal transmitted through the signal/ground TSVs, which can lead to potential signal integrity issues.

Information Classification: General

TABLE IX Cases of 3 D IC with different DRAM dies and on-chip decoupling capacitors

Cases	Description
Case3	4 layers of DRAM die, 4 nF on-chip decap
Case3	8 layers of DRAM die, 4 nF on-chip decap
Case3	8 layers of DRAM die, 1 nF on-chip decap

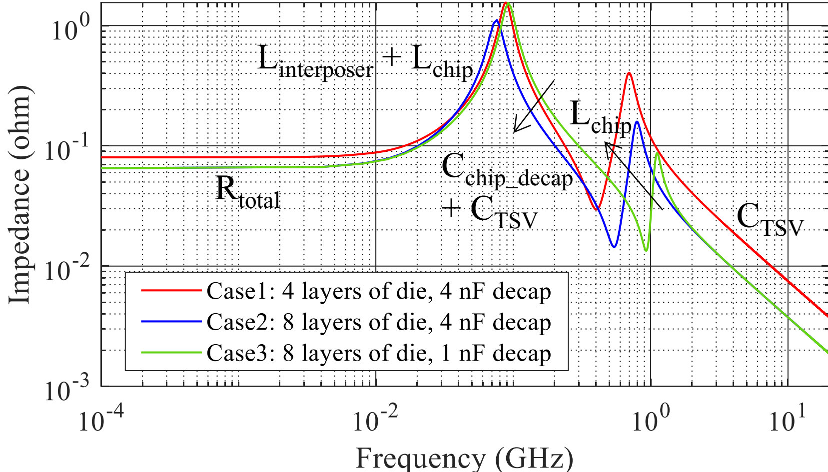

Fig. 19 Comparison of system PDN impedance curves with different number of DRAM layers and decoupling capacitors.

Summary and conclusions

This paper presents the bias-dependent effect of power TSVs in HBM 3D ICs and highlights the importance of considering the low-frequency bias-dependent TSV capacitance on the system PDN during the preliminary design phase of the HBM system. The depletion/bias effect of the TSV structure at different bias voltages is discussed. In addition, it is found that the number of P/G TSVs instead of the pattern of the P/G TSV array mainly affects the overall capacity of the TSV array in low frequency regions (< 200 MHz). To investigate the depletion/bias effect of the P/G TSV array on the system PDN, a hierarchical equivalent circuit model is built for the system PDN, including the PCB, package, Si interposer, and the on-die PDN, which are extracted from measurements and simulations. Frequency domain and time domain simulates are performed to analyze the PDN impedance, power supply noise and power supply induced jitter with/without considering the depletion effect of the power TSVs. Methods to reduce the system PDN impedance by reducing the resonances generated by the bias-dependent TSV capacitance are discussed.

By considering the depletion effect of the P/G TSV pair in the pre-design stage, the potential power and signal integrity risks in the system PDN can be more accurately assessed. By considering the TSV capacitances as on-chip decoupling capacitors in the pre-design phase, the cost of placing a large number/value of on-chip decoupling capacitors can be significantly reduced.

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The limitations of the proposed PDN model are: 1) the impedance is extracted extracted by looking from the top layer of the DRAM die into the system PDN; 2) the structure and size of the on-chip PDN and Si interposer are under assumption of ideal dimensions; 3) no actual PDN measurement validation on the 3D IC system with TSVs.

In the future, the current work can be improved in the following aspects: 1) PDN modeling by looking from the different layers of the DRAM die into the system PDN; 2) system PDN modeling from PCB to on-die PDNs with more realistic structures and sizes of on-chip PDN and Si interposer and measurement validation; 3) modeling of hysteresis behavior and analysis of TSV structures as a function of temperature, bias voltage, and changing speed of bias voltage and temperature.

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