Multilevel Switched-Capacitor AC-DC Step-Down Rectifier for Wireless Charging with Reduced Conduction Loss and Harmonic Content

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***Abstract*—In this paper, a wireless charging architecture employing a multilevel switched-capacitor (MSC) AC-DC rectifier is investigated. The proposed MSC rectifier features a multilevel design which is scalable to accommodate different power ratings and load ranges. The topology showcases advantages for wireless power transfer (WPT) systems in terms of compactness, efficiency, impedance tunability, and harmonic attenuation. The single-stage active topology is capable of varying its low-distortion staircase input voltage to tune the wireless power transfer system for high system-wide efficiency. A 7-level, 20 W prototype is used to verify the WPT loading and loss analysis. The prototype operates at 150 kHz with up to 3:1 step-down conversion ratio to an output voltage of 5.0 V. The experimental peak DC-to-DC efficiency is 93.8% and the rectifier peak efficiency is 98.3%. The rectifier demonstrates low waveform distortion and high efficiency across many WPT loading conditions, solidifying its place as a strong candidate for wireless power applications.**

Index Terms - wireless power transfer, switched-capacitor converter, multilevel converter, rectifier, inverter, SHE, WPT tuning.

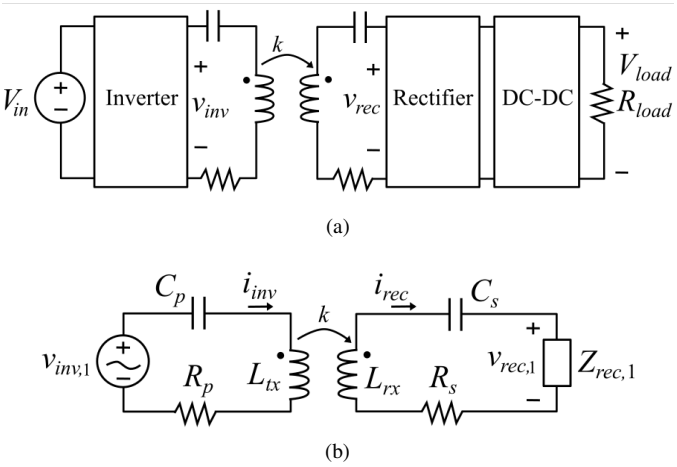

Fig. 1. The (a) block diagram and (b) fundamental model of a typical WPT system.

I. Introduction

Consumer mobile electronics have become prolific in daily lives. Computation capabilities, communication speeds, and display resolutions have gradually increased, resulting in power demand that approaches the daily energy limit of modern mobile battery technologies. To decrease the impact of periodic recharging, fast charging technology has been proposed and adopted by many manufacturers [1–3], with commercial devices supporting wired charging in excess of 20 W. Wireless power transfer has been developed in recent years, with commercial wireless chargers integrated into many products [3].

A typical wireless power transfer (WPT) system architecture is shown in Fig. 1a. The tuned primary and secondary coils are referred to as the WPT tank. The inverter presents an AC voltage to the WPT tank, inducing a voltage on the receiver side. The secondary-side waveform is then rectified back to DC, and the DC-DC converter steps the voltage up or down to regulate the output, V_{load}. Motivated by the bandpass nature of the WPT coil tuning, the first harmonic approximation (FHA) is used to model the system as in Fig. 1b. In this work v_{inv} and v_{rec} refer to the AC (plus harmonics) inverter and rectifier voltages, respectively. Variables $v_{inv,1}$ and $v_{rec,1}$ are the fundamental components of these voltages.

Fig. 1 illustrates two important system characteristics: distortion and loading. The FHA model assumes negligible power transmission and loss occur at any harmonic other than the fundamental. Further, even with broadband modeling, the presence of additional harmonic components increases the risk of interference with other electronics and may necessitate additional filtering components [4, 5] and increases loss due to reduced efficiency of power transfer at harmonic frequencies. Thus, solutions whose real waveforms are well-approximated by the FHA are advantageous. Second, the complex rectifier impedance, Z_{rec}, loads the system. Therefore, the fundamental impedance component, $Z_{rec,1}$, is directly responsible for system-wide efficiency [1]. An optimal value of $Z_{rec,1}$ ensures the highest system-wide efficiency [6]. These metrics of total harmonic distortion (THD) and real-time impedance tuning (ability to vary $Z_{rec,1}$) are used to evaluate WPT rectifiers.

Two other metrics are especially important for small consumer devices: efficiency and size. A high efficiency circuit is always desired, but it is especially important for thin handheld

electronics that must remain cool to the touch. Also, size is a premium in tightly-packed consumer device circuit boards, so low-footprint-area topologies using low-profile components are desired. Avoiding bulky and lossy DC filter inductors [7, 8] and topologically combining stages (integrating the rectifier and DC-DC converter) are attractive attributes for WPT rectifiers.

The diode full bridge (DFB) of half bridge (DHB) rectifier (without a DC-DC conversion stage) is attractive for its simplicity and compactness. However, the rectifier input impedance is fixed as a function of R_{load} under the FHA approximation [1]. Furthermore, the square wave voltage produced by the DFB is known to contain high harmonic content. These shortcomings result in high-distortion waveforms and non-optimal values of $Z_{rec,1}$ that can cause large tank currents [9]. Because of the static value of $Z_{rec,1}$, the work in [9] requires V_{in} be tuned in order to keep V_{load} constant across different values of R_{load}.

Another popular approach is including a DC-DC converter between the DFB and V_{load}. This may be implemented with a buck [10], boost [11], cascade buck and boost [12], or buck-boost [6, 13, 14]. For any of these approaches, impedance $Z_{rec,1}$ is now a function of both R_{load} and DC-DC converter duty cycle, D. Depending on the DC-DC converter, impedance magnitude $|Z_{rec,1}|$ can now be increased, decreased, or both relative to the case without a DC-DC converter [6]. The drawback is that these implementations not only add a second stage to the rectification scheme, but the second stage requires a large filter inductor. The bulky DC filter inductor can be avoided by using a DC-DC switched capacitor converter (SCC) [15, 16] in lieu of buck/boost implementations. However, discrete steps in regulation (and consequently $|Z_{rec,1}|$) make this implementation challenging [17].

Replacing the DFB devices with transistors, a synchronous full bridge (Sync FB) can reduce conduction losses due to diode forward voltage without significantly altering in-circuit behavior [18–21]. If the transistor full bridge is additionally controlled through phase or duty-cycle modulation, it is considered an active full bridge (AFB). An AFB can control $\angle Z_{rec,1}$ by varying the switching times within the period [22]. The ability to vary $\angle Z_{rec,1}$ equips the rectifier to inject reactance into the circuit to retune the system in the event L_{rx} and C_s do not resonate at the fundamental frequency [23]. With the combination of an AFB and an up/down regulator (such as a Sync FB + LDO [24]), the rectifier could theoretically reach any value of $Z_{rec,1}$, enabling WPT tank retuning for optimal system-wide efficiency over a wide range of coil mismatch, coupling change, output power, and interference situations.

However, each of the reviewed approaches has some set of drawbacks. The DFB is compact and single-stage, but it cannot retune its impedance or address waveform distortion. Multi-stage approaches enable control of $|Z_{rec,1}|$, but those with buck/boost style DC-DC converters require a large filter inductance [12–14]. SCC converters avoid the filter inductor, but they produce discrete steps in $|Z_{rec,1}|$, making precise impedance tuning more difficult. AFB rectification enables reactance injection, but even in the case of 3-level modulation, their waveforms produce significant harmonic content, and they require an additional dc-dc for bidirection impedance magnitude conversion. More-complex resonant resonant class-E rectifiers [5] can exhibit very low distortion, but are difficult to design over a wide range of operating conditions.

Switched-capacitor step-down rectifiers have previously been studied for AC-DC rectification [25] in wired applications where THD, impedance control, and compactness were of lesser concern. In this work, the multi-level switched capacitor (MSC) rectifier is proposed as a holistic solution for WPT applications that simultaneously addresses each evaluation metric by achieving low-THD, regulated impedance, small-size and high-efficiency. In order to achieve these metrics, the topology, design, and modulation are tailored to the intended application. The single-stage topology requires no DC filter inductor, can inject reactance ($\angle Z_{rec,1}$), possesses both up and down regulation of $|Z_{rec,1}|$, is highly efficient, and significantly reduces WPT tank distortion (relative to the nominal square wave case) via its staircase waveforms.

The remainder of the paper is organized as follows. Section II further motivates the impedance tuning characteristics of the MSC topology. Section III establishes the main operating principle of the MSC WPT system, and Section IV investigates how the MSC modulation scheme interacts with the FHA model. Section V derives loss mechanisms, and Section VI supports the analysis with experimental testing. Finally, Section VII concludes the work.

II. Topology Comparison

To emphasize the impedance and tunability differences among the reviewed topologies, an example application is examined uder the FHA. An example tank is employed for comparing different rectification approaches in Fig. 2. These example tank parameters are set such that $L_{tx} = L_{rx} = 10$ μH, the $L_{rx}|C_s$ pair resonates at 150 kHz, and $R_p = R_s = 100$ mΩ. These coil inductances and quality factors are within a realistic range: a market-available 10 μH WPT coil has equivalent series resistance (ESR) values between 43 and 554 mΩ through the first 5 harmonics [26]. In this example, the consumer device is paired with a transmitter system that is tuned to 100 kHz, that is $|Z_{Ltx}| = |Z_{Cp}|$ at 100 kHz.

Each of the cases in Fig. 2 shows the tank efficiency (color), power contours (black lines), peak efficiency point (black X), and peak 20 W efficiency point (black O). Furthermore, the DFB, DFB and buck converter (DFB + buck), and AFB topologies are included. These are denoted by the black dot, dashed line, and translucent white area, respectively. Each topology is overlaid onto the plots such that the output voltage remains constant at $V_{load} = 5$ V. The active full bridge and buck converter (AFB + buck) topology is not pictured as it can reach any point on Fig. 2 via full control of $Z_{rec,1}$.

The first case in Fig. 2a shows the system with a nominal coupling value of $k = 0.55$. Here, inverter voltage V_{in} is set to 26.2 V so that the diode full bride rectifier experiences $P_{out} = 20$ W, the desired system power. Because the DFB

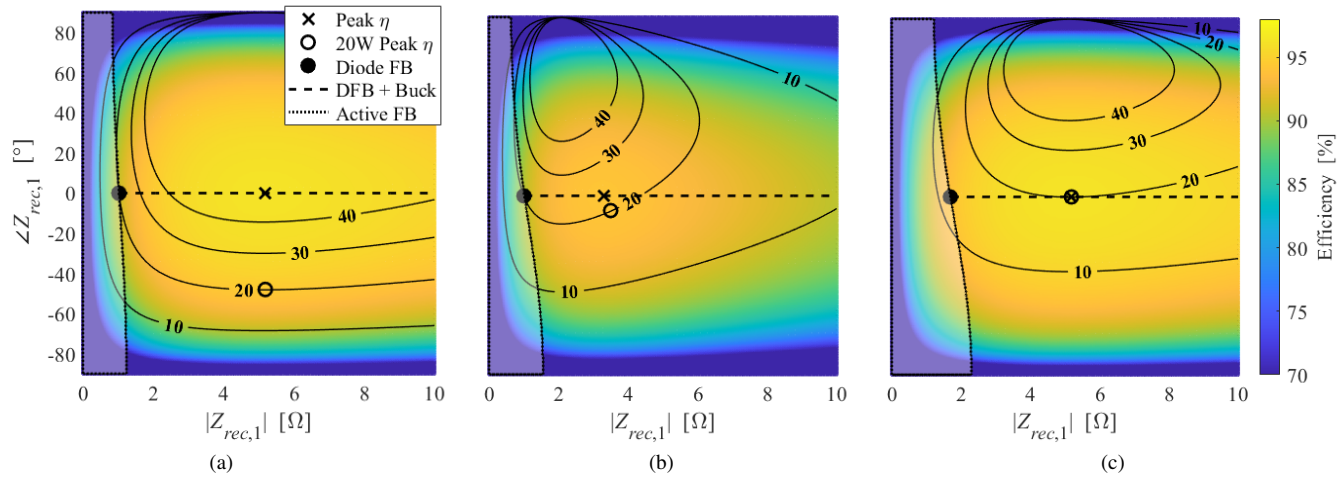

Fig. 2. Efficiency (color) and power (contours) plots with rectification strategies and optimal points overlaid. $V_{load} = 5$ V for all cases. The cases have (a) $k = 0.55$ and $V_{in} = 26.2$ V, (b) $k = 0.35$ and $V_{in} = 18.7$ V, and (c) $k = 0.55$ and $V_{in} = 16.4$ V.

cannot vary its input impedance, maintaining $P_{out} = 20$ W means that a coupling change to $k = 0.35$ forces an input voltage change to $V_{in} = 18.7$ V in Fig. 2b.

Taken in isolation, Figs. 2a and 2b illustrate some important points. First, the AFB topology does no better in either scenario: the duty cycle impedance step-down mechanic is not helpful for these cases. Second, the DFB + buck topology is beneficial to improve the efficiency of 20 W power transfer in Fig. 2b. Here, the step-up impedance transformation is useful because $Z_{rec,1} = 1.0\ \Omega$ and $Z_{rec,1} = 4.3\ \Omega$ both yield 20 W, but the latter does so at a higher efficiency by reducing WPT tank current. Finally, full impedance control (as with the AFB + buck) is beneficial in both cases. Reaching the 20 W peak efficiency point requires full control of $Z_{rec,1}$, and it showcases $\approx 4\%$ higher efficiency than the DFB in both cases. For Figs. 2a and 2b, the DFB efficiencies are 90.7% and 90%, compared to the optimal 20 W load efficiencies of 94.5% and 94.1%, respectively.

Fig. 2c extends the concept of leveraging V_{in} to the case with full impedance control. This optimal case revisits $k = 0.55$ but sets $V_{in} = 16.4$ V so that the overall most efficient operating point occurs at 20 W. Because the $L_{rx}|C_s$ pair is tuned to the operating frequency (150 kHz), this point occurs at $\angle Z_{rec,1} = 0$. Here, the DFB + buck and AFB + buck can both reach the optimal point: 20 W output at 96.2%.

Therefore, cases with non-optimal transmitter characteristics (like Figs 2a and 2b) benefit from both magnitude and reactance tuning. Cases where communication enables primary-side optimization (like Fig. 2c) benefit from magnitude tuning. The MSC topology is able to fully control $Z_{rec,1}$, hitting each of the optimal 20 W operating points in Fig. 2. Additionally, the topology has reduced THD, avoids bulky filter inductors, and combines the rectification and DC-DC conversion stages, making it a promising candidate for miniaturization in mobile electronics applications.

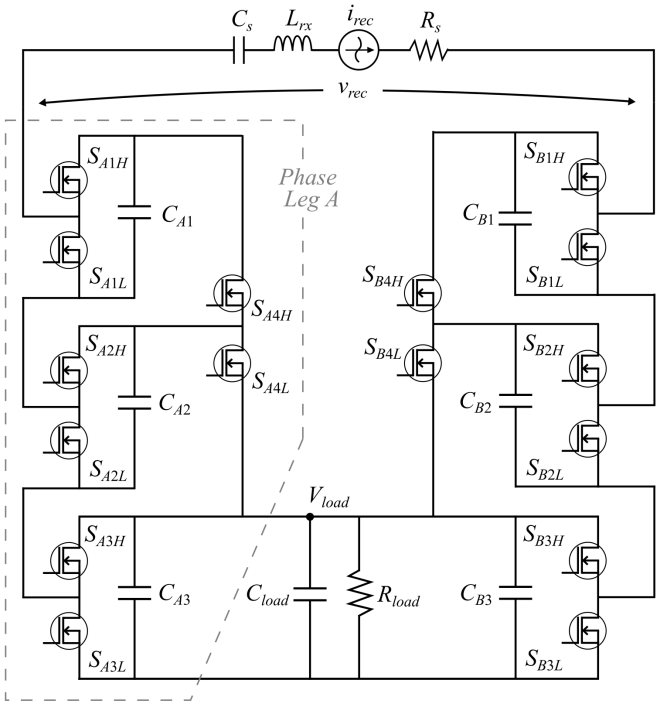

Fig. 3. Schematic circuit of the proposed 7-level switched-capacitor ac-dc rectifier with 3:1 voltage step-down.

III. Multilevel Switched Capacitor

The schematic circuit of the multilevel switched-capacitor rectifier is shown in Fig. 3, using a 7-level implementation as an example. The topology comprises a bipolar series-parallel switched capacitor converter. Because the topology is modular, it can be expanded to more levels. The 7-level implementation is selected in this study to achieve conversion ratios of above 3:1, which mimics the buck converter's impedance transformation capability as highlighted in the previous section. In accordance with the fundamental model, elements L_{rx}, C_s,

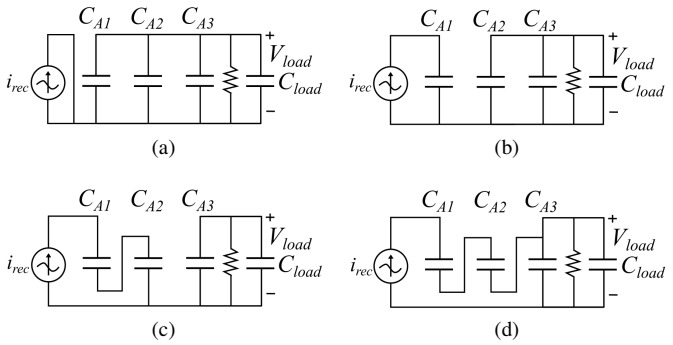

Fig. 4. Operation principle of step-down MSC rectifier in one half-cycle. Operation sequence: 1-2-3-4-3-2-1. (a) Subinterval 1; (b) Subinterval 2; (c) Subinterval 3; (d) Subinterval 4.

and R_s are included, while sinusoidal current i_{rec} is used as the source for the rectifier model.

The topology of Fig. 3 forms a single-phase rectifier with two identical legs, *Phase Leg A* and *Phase Leg B* (not labeled in Fig. 3), operated symmetrically with 180° phase shift synchronized to the zero-crossings of v_{rec}. The circuit composition and control signal sequence of the two legs are the same, so only the positive half-cycle of v_{rec} is discussed in detail. All devices in the rectifier switch on and off once per period, and switching devices in a half bridge configuration, such as S_{A1H} and S_{A1L}, have complementary schemes.

This topology is previously studied as a wired AC-DC rectifier in [27]; however, switching actions of all devices in one phase leg were synchronized such that the differential voltage v_{rec} was a two-level square wave with a fixed conversion ratio. In this work, individual switch pairs in a phase leg are independently controlled to generate a multilevel staircase waveform, instead of a two-level square wave. Therefore, the low-order harmonic magnitudes are smaller than those in a square wave of the same fundamental amplitude. Additionally, the modulation pattern is varied to allow variable conversion ratio and variable phase alignment. Together, these two modulation freedoms allow the MSC to vary both the magnitude ($|Z_{rec}|$) and angle ($\angle Z_{rec}$) of the impedance presented to the WPT system, which can be used to optimize system efficiency as discussed in Section I.

Equivalent circuits of the proposed 7-level SC rectifier during switching subintervals in one half-cycle are shown in Fig. 4. The MSC switching pattern is quarter-wave symmetric with 7 subintervals per input half-cycle. The operation sequence in one half-cycle is subintervals:

$$1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 3 \rightarrow 2 \rightarrow 1,$$

and the control signals for switching devices in *Phase Leg A* are given in Fig. 5.

In order to simplify analysis, two assumptions are made about the converter design: 1) All flying capacitors are large enough to ensure small voltage ripple, and the output capacitance C_{load} is sufficient to ensure a constant V_{load}; 2) All subinterval durations are much longer than the switched capacitor circuit internal RC dynamics, so that the slow

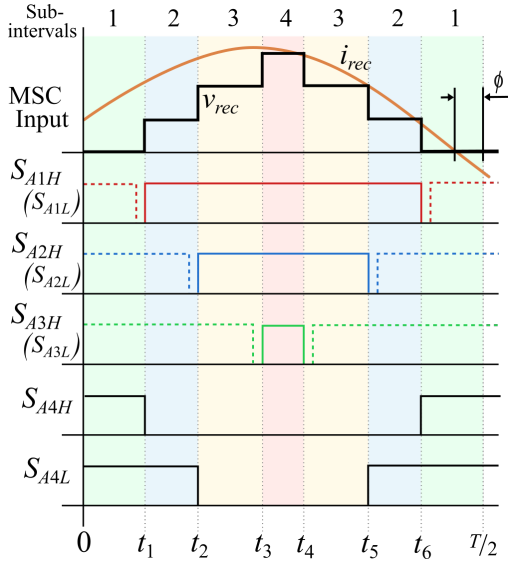

Fig. 5. Control signal sequence for 7-level SC rectifier in one input half-period. For each gate signal, Solid line: high side switches and charge sharing switches (S_{A1H}, S_{A2H}, S_{A3H}, S_{A4H}, S_{A4L}); dashed line: low side switches (S_{A1L}, S_{A2L}, S_{A3L}).

switching limit (SSL) applies at given switching frequency (150 kHz) [28]. Under these assumptions, the flying capacitor voltages are approximately DC, with magnitude equal to the load voltage V_{load}.

In subinterval 1, the input voltage of the rectifier is 0 V, and all low-side switches (S_{xxL}) conduct to provide a return path for the input current. All flying capacitors, $C_{A1} - C_{A3}$, are connected in parallel with the output, discharging to the load, as shown in Fig. 4a. In subinterval 2, C_{A1} is charged by the input current, and the input voltage is equal to the load voltage V_{load}. By switching additional flying capacitors in series with the input, the rectifier can generate an input of $2V_{load}$ in Fig. 4c, or $3V_{load}$ in Fig. 4d.

Because the bottom module is directly shorted to the output capacitor, the voltage of C_{A3} is always the output voltage, V_{load}. As such, C_{A3} (and C_{B3}) can be combined with C_{load} and implemented as a single component. Flying capacitors C_{A1} and C_{A2} are periodically shorted to the output by S_{A4H} and S_{A4L}, respectively, at the instances t_5 and t_6, as shown in Fig. 5. For the opposite half-cycle, *Phase Leg A* stays in subinterval 1 where all flying capacitors are clamped to the output DC bus, while the *Phase Leg B* operates in the same manner with 180° phase shift to provide the negative half-cycle of v_{rec}. In a full period, this MSC rectifier generates a 7-level staircase voltage v_{rec} at the input terminal, with the peak value $|v_{rec}(t)| = 3V_{load}$.

For the 7-level SC topology, the number of capacitors in one phase leg is $n_m = 3$. By stacking more modules ($n_m > 3$), the MSC can achieve a higher voltage step-down ratio, directly affecting the converter's input impedance. However, more switching devices and flying capacitors are required, which may contribute to higher conduction and switching loss, as well as increased size. Therefore, it is

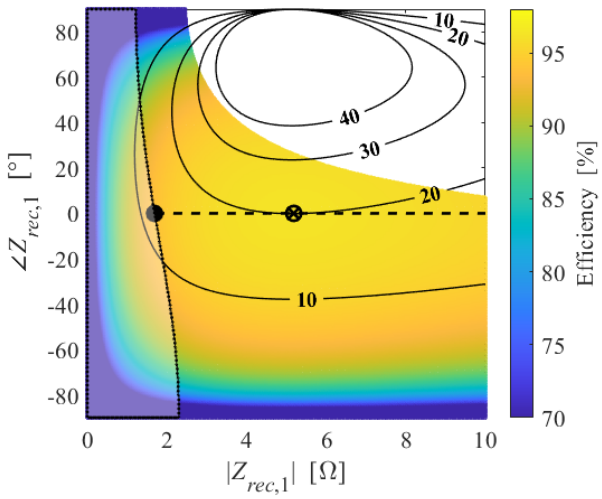

Fig. 6. Operation region of the MSC under the $k = 0.55$ and $V_{in} = 16.4$ V example of Section I. The MSC cannot reach the white region because $M > 3.81$. The most efficient 20 W operating point for this example tank is $\eta = 96.2\%$.

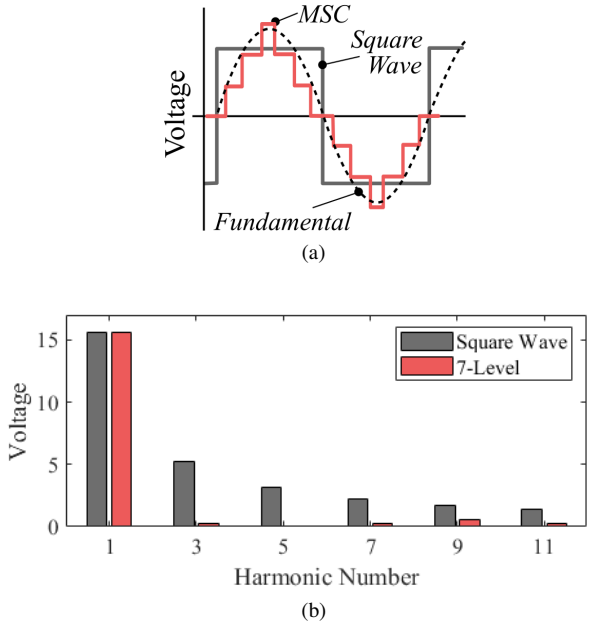

Fig. 7. A comparison of the 7-Level SC rectifier input voltage and a square wave voltage with the same fundamental component. (a) Time domain waveforms and (b) spectrum comparison.

necessary to understand how the number of modulation levels affects both the rectifier's impedance characteristics and the rectifier's conversion efficiency.

IV. MSC Fundamental Representation

The fundamental model of Fig. 1b is again referenced. The rectifier fundamental voltage and the DC load voltage are divided to define modulation index,

$$M = \frac{|v_{rec,1}|}{V_{load}}, \quad [1], \tag{1}$$

a metric used to describe the total step-down effect of the rectification stage. In general, the output voltage (V_{load}) is determined by the combination of modulation index M, rectifier switching times (i.e. $\angle Z_{rec,1}$), and R_{load}. By design, this steady state modeling work sets $V_{load} = 5$ V, but a final design would utilize closed-loop control for regulation. The proposed MSC rectifier relies on modulation index to achieve rectifier impedance magnitude transformation. The modulation of multilevel converters has been studied extensively, where either carrier-based modulation [29, 30] or selective harmonic elimination (SHE) [31] are employed.

The equivalent impedance of the MSC rectifier when the rectifier voltage and current are in phase is

$$Z_{rec,1} = |Z_{rec,1}| = \frac{M^2}{2} R_{load}. \quad [1] \tag{2}$$

Here, $Z_{rec,1}$ is a simple function of the modulation index and the load. However, because the circuit is actively switched, the rectifier input voltage and input current can be set out of phase by changing the device switching times. In the case of a non-zero phase shift ($\angle Z_{rec,1} = \phi \neq 0$), the total fundamental impedance of the MSC rectifier is given by

$$Z_{rec,1} = \frac{M^2}{2} R_{load} \cdot \cos(\phi) e^{j\phi}. \tag{3}$$

For a 7-level SC rectifier, both the modulation index and switching time determine the total input impedance at a given load. The upper and lower bounds of M depend on the number of levels in the converter and the specific modulation scheme selected. With $n_m = 3$, M can range from 0 to $n_m \cdot 4/\pi = 3.81$ using carrier-based modulation. In the extreme, when $M = 3.81$, the 7-level staircase waveforms resembles a two-level square wave which provides a maximum rectifier impedance. Though the fundamental amplitude changes with modulation index, the instantaneous peak voltage remains $|v_{rec}(t)| = 3V_{load}$ as long as each modulation level is employed.

Motivated in Section II, Fig. 6 compares the functional operating area using the example in Fig. 2c. The operating range of the 7-level circuit is shown by the colored portion of Fig. 6 and covers most of the graph area. Again, the levels of the contour plot in Fig. 6 show output power. The empty white section near the top right of Fig. 6 represents the area where the modulation index must exceed $M = 3.81$ for a given output voltage of $V_{load} = 5$ V, and the MSC cannot, therefore, operate in this region as designed with $n_m = 3$.

To extend impedance transformation ability, more modules can be stacked to allow a larger number of voltage levels, which essentially increase the range of M from modulation perspective. In general, the achievable modulation range is $0 < M < n_m \cdot 4/\pi$. This scalability helps to accommodate different applications by adding/subtracting modules.

The 7-level SC rectifier modulation reduces the harmonic content in the WPT circuit. Compared with a full bridge rectifier, the multilevel converter generates low THD, near-sinusoidal voltages with a switching frequency equal to the fundamental frequency [30]. In Fig. 7b, the harmonics of an

TABLE I
HIGH AND LOW SIDE SWITCH LOSS CONTRIBUTIONS FROM FIG. 8

Case	Loss Mechanism			
	ON	OFF	Diode	C_{oss}
1: $I_{lc} < 0$	HS	LS	LS	HS
2: $I_{lc} < I_{th}$	HS	LS	—	HS
3: $I_{lc} = I_{th}$	—	LS	—	—
4: $I_{lc} > I_{th}$	—	LS	HS	—

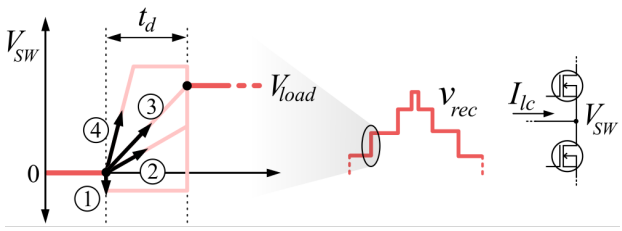

Fig. 8. Linearized dead time for a rising edge showing the potential V_{sw} translation cases dependent on I_{lc}.

example, sinusoidally-modulated 7-level staircase waveform are compared with a two-level square waveform with the same fundamental magnitude. The MSC waveform shows significantly lower 3rd, 5th, and 7th harmonics. This reduces the necessary size (and loss) of filtering, and it facilitates compliance with bandwidth requirements and EMI standards. If necessary, the harmonics of the MSC can be further reduced by employing selective harmonic elimination (SHE) to nullify a range of low-order harmonics such as the 3rd and 5th with a programmed switching pattern [31].

Overall, the MSC topology enables lower waveform distortion, provides complete impedance tunability, and avoids bulky filter inductors, resulting in a higher system-wide efficiency and increased secondary-side compactness. Next the loss mechanisms of the converter are analyzed to develop a design that enables these benefits.

V. LOSS ANALYSIS

This section analyzes several major losses of the proposed MSC rectifier. The following loss analysis is based on the control sequence shown in Fig. 5 and assumes all switching devices are identical.

1) Conduction Loss: The conduction loss consists of two parts: the conduction loss due to the R_{dson} of the switching devices in a current path; and the conduction loss induced by the flying capacitor ESRs. The total conduction loss is

$$P_{cond} = 2 \cdot n_m \cdot I_{rms}^2 \cdot R_{ds(on)} + P_{ESR,C} \tag{4}$$

where I_{rms} is the RMS value of the input current i_{rec}, and $P_{ESR,C}$ is the conduction loss of the flying capacitors. The function for calculating $P_{ESR,C}$ is

$$P_{ESR,C} = \sum_{x=1}^{n_m} I_{recRMS}(x)^2 \cdot R_{ESR,C} \tag{5}$$

where the function I_{recRMS} describes the RMS equivalent on current seen by the capacitor (not including charge redistribution current) in modulation level $x = \{1, 2, 3\}$. Equation (6) defines I_{recRMS} with $(t_{7-x} - t_x)$ as the on time of level x ($x = 1$ denotes $v_{rec} = 1 \cdot V_{load}$, $x = 2$ denotes $v_{rec} = 2 \cdot V_{load}$, etc.) and $R_{ESR,C}$ as the series resistance of each flying capacitor. Under the FHA, (6) assumes i_{rec} is a single-frequency sinusoid.

$$I_{recRMS}(x) = \frac{1}{2} |i_{rec}|^2 f_s \, (t_{7-x} - t_x) \cdot \left(2 + \frac{\sin(2(\omega t_x - \phi)) - \sin(2(\omega t_{7-x} - \phi))}{\omega(t_{x-7} - t_x)}\right) \tag{6}$$

A. Switching Loss

Each level change in v_{rec} is consequent of one pair of half-bridge switching actions. Generalizing this action with Fig. 8, the dead time waveforms are approximated as linear, under the assumption that the dead time is very short relative to circuit dynamics and the fundamental operating period. One of four scenarios occurs. A threshold current is defined as

$$I_{th} = 2C_{oss} \frac{V_{load}}{t_d}, \tag{7}$$

where t_d is the dead time. Current I_{lc} is the approximated-constant current during the dead time, defined by the value of i_{rec} at the switching instant. The relationship between I_{lc} and I_{th} determines the case as shown in Table I. A negative current (case 1) forces diode conduction, a small current (case 2) reduces hard switching loss, exact ZVS current (case 3) only results in T_{off} loss, and a large dead time current (case 4) causes over charging of the switch node.

The switching loss mechanisms are summarized by

$$P_{on} = 1/2 \, |I_{lc}| \, V_{on} \, t_{on} \, f_s \tag{8}$$

$$P_{off} = 1/2 \, |I_{lc}| \, V_{load} \, t_{off} \, f_s \tag{9}$$

$$P_{diode} = V_d \, |I_{lc}| \, t_{dc} \, f_s \tag{10}$$

$$P_{coss} = 1/2 \, C_{oss} \, V_{on}^2 \tag{11}$$

where parameters V_{on} and t_{dc} are defined as

$$V_{on} = V_{load} \, (I_{th} - I_{lc})/I_{lc} \tag{12}$$

$$t_{dc} = t_d \, (I_{lc} - I_{th})/I_{th} \tag{13}$$

for cases 2 and 4, assuming linearized dead time waveforms during the short dead time, as shown in Fig. 8. These parameters are $t_{dc} = t_d$ and $V_{on} = V_{load} + V_d$ for case 1. Parameters V_d, t_{on}, and t_{off} are the body diode voltage, turn-on time, and turn-off time, respectively. Since all devices switch on and off only once in a full period, the switching frequency f_s is the WPT carrier frequency. Gate loss is not considered in the power stage model. Fig. 8 and Table I show the loss breakdown for rising edges, but the same approach is applied to falling edges and inverter switching actions (with appropriately modified equations and thresholds).

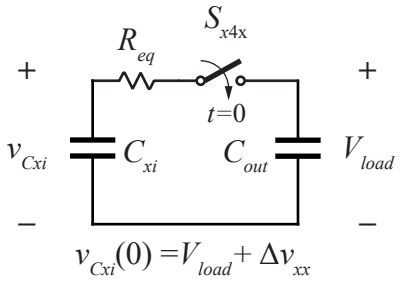

Fig. 9. Charge sharing loss equivalent circuits in MSC rectifier: capacitor to capacitor.

B. Charge Sharing Loss

In the MSC converter, each flying capacitor C_{xi} is charged by i_{rec} during the portion of the period where that capacitor contributes to v_{rec}, resulting in a small increase in capacitor voltage Δv_{xx}. During the non-active half period, charge sharing switches S_{x4x} turn on for $T_s/2$ and the respective flying capacitors are connected in parallel with the output capacitance C_{out}. This causes a pulsed current which equalizes the capacitor voltages through a resistive path, resulting in charging sharing loss [28]. It is assumed that $C_{out} \gg C_{xi}$, either by design or, due to the connection of multiple flying capacitors in parallel with the output at any moment, and therefore V_{load} remains nearly constant during the process. Charge sharing loss is modeled using the generalized equivalent charge sharing circuit of Fig. 9.

Resistance R_{eq} consists of the capacitor ESR, transistors' $R_{ds,on}$ and any other parasitic resistance in the charging path. In the following analysis, the charge sharing dynamics are assumed to be consistent with the slow switching limit (SSL) approximation, conssitent with the prototype of Section VI. In the SSL, the impacts of R_{eq} are negligible [28, 32]. This approximation holds for the worst-case charging loop, when C_{x1} is connected to V_{load}, if

$$\max(\tau) = C_{xi}\ \left(2R_{ESR,C} + 4R_{ds,on}\right) \ll \frac{T_s}{2}, \qquad (14)$$

Because the switching frequency is a fixed $f_s = 150$ kHz, this inequality holds when the MSC is designed such that resistances are minimal and the capacitance C_{xi} is less than some maximum value. Increasing C_{xi} will reduce charge sharing losses until this inequality is violated, after which efficiency gains will be negligible due to the charge sharing dynamics approaching the fast switching limit (FSL) [28, 32].

In Fig. 7, if $\Delta v_{xx} = 0$, no loss occurs when the switch closes. However, with a voltage difference ($\Delta v_{xx} \neq 0$) the charge redistributes as the two capacitors are shorted. For capacitor C_{xx}, the voltage ripple is dictated by the portion of the power current i_{rec} going through the device.

$$v_{xx} = \frac{1}{C_{xx}} \int_{t_x}^{t_{7-x}} |i_{rec}| \sin(\omega t + \phi) dt + V_0, \qquad (15)$$

where the initial voltage is equal to the output voltage, $V_0 = V_{load}$, due to SSL operation. Solving the integral and ignoring the DC component gives the voltage ripple on capacitor C_{xx},

$$\Delta v_{xx} = \frac{|i_{rec}|}{\omega C_{xx}} \Big(\cos(t_x\omega + \phi) - \cos(t_{7-x}\omega + \phi) \Big). \qquad (16)$$

Assuming a small incremental voltage Δv_{xx}, a constant V_{load}, and $C_{load} \gg C_{xx}$, then the charge sharing loss is

$$P_{cs} = {}^1\!/_2\, C_{xx}\, \Delta v_{xx}^2\, f_s. \qquad (17)$$

From (17), the charge sharing loss, which can be significant in hard-charging SC converters, is proportional to the switching frequency, capacitance and voltage ripple on flying capacitors. Each of the flying capacitors, C_{x1} and C_{x2}, is subject to voltage ripple and consequent charge sharing loss defined in (17).

The conduction, charge sharing, and switching loss calculations each rely on approximations within the model. To test the accuracy of these approximations, the circuit model is compared with a prototype WPT system. Accurate prediction of the system-wide efficiency reinforces the validity of the modeling approach.

VI. Experimental Results

The experimental setup is shown in Fig. 10. A single FPGA controls both a full bridge inverter and the 7-level MSC rectifier, and both use the 30 V, 25 A half-bridge silicon module and gate driver listed in Table II. Floating voltages are required to drive each switch that is not grounded at its source. Many of these floating DC voltages are required for the 7-level switched capacitor converter. Each floating voltage is generated via bootstrap circuitry, requiring no additional switching actions. Finally, the isolators seen in Fig. 10 are used to level-shift the FPGA PWM signals to the floating voltages.

The circuit used to provide floating supplies to each gate driver is shown in the partial schematic of Fig. 11. In the gray dashed boxes, commercial half-bridge drivers are used with bootstrap diode and decoupling capacitors for each gate driver. During the half-period where this phase leg is non-active, all low side switches S_{xiL} and charge sharing switches S_{x4H} remain on for duration $T_s/2$. During this time D_{B2} will recharge the low-side supply of S_{x2L} from the gate drive supply voltage V_{dr}; the same will happen in the top module S_{x1L} and D_{B1} (not shown). For the charge sharing switches, D_{B4} recharges the supply of S_{x4L} whenever S_{x3H} is on, which can be guaranteed by modulation pattern. Due to the use of silicon FETs with wide V_{gs} range, even with multiple diodes in the bootstrapping path, the reduced driving voltage does not significantly increase R_{dson}.

The wireless power tank is designed to reduce loss and compliment the study of the MSC rectifier. Two 9 A high-Q WPT coils are physically separated by thin paper dividers, fastened in place, and tuned. Either side of the tank is measured with the opposite side open, and a final measurement of the primary is taken with the secondary shorted. Values L_{tx}, L_{rx}, C_p, and C_s are reported by a Keysight E4990A impedance analyzer. Capacitances C_p and C_s are comprised

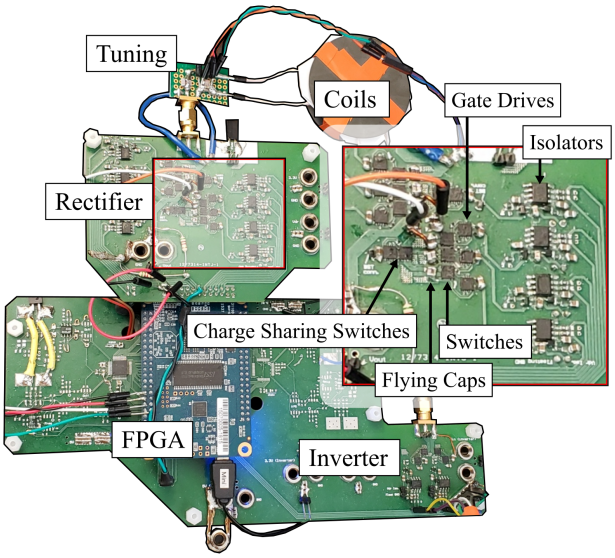

Fig. 10. Experimental setup showing the FPGA controller, inverter, tuned WPT tank, and rectifier.

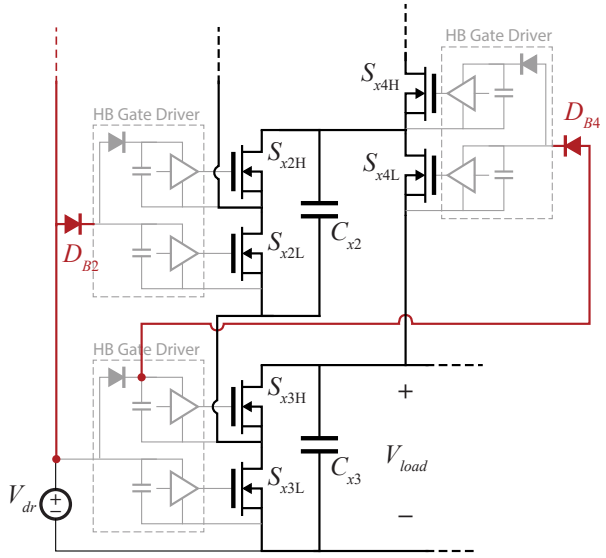

Fig. 11. Bootstrapping scheme for gate drive power supplies.

of multiple discrete components in parallel, each of which is rated for 100 V. The coupling value of $k = 0.773$ is calculated by matching the theoretical circuit to the impedance analyzer measurements.

The impedance analyzer returns ESR values of 78.55 mΩ and 73.08 mΩ for the primary and secondary sides of the WPT tank, setting the 150 kHz quality factors at 158.6 and 171.0, respectively. Next, blank rectifier and inverter PCB's are semi-populated: the inverter has the input capacitance populated and one complimentary switching pair shorted, and the rectifier sees the switches in the ground path shorted ($v_{rec} = 0$). The ESR values of each PCB are measured at 150 kHz, and the final values of $R_p = (78.55 + 8.20)$ mΩ and $R_s = (73.08 + 45.40)$ mΩ are reported in Table III.

TABLE II
PROTOTYPE CHARACTERISTICS

Part / Characteristic	Part Number	Value
Silicon Module (HB)	BSZ0910NDXTMA1	—
Gate Driver (HB)	MP1907AGQ-P	—
Isolator	SI8423BB-D-IS	—
Controller	Altera Cyclone IV	—
Tx & Rx Coils	760308101141	10 μH
Switching Frequency	—	150 kHz
Input Voltage	—	7-20 V
Output Voltage	—	5.0 V
Rated Power	—	20 W

TABLE III
CIRCUIT VALUES OF EXPERIMENTAL PLATFORM

L_{tx}	C_p	R_p	C_{xx}
13.22 μH	757.56 nF	86.75 mΩ	15.66 μF
L_{rx}	C_s	R_s	C_{load}
13.26 μH	111.76 nF	118.48 $m\Omega$	27.41 μF
V_d	t_{on}	t_{off}	C_{oss}
0.78 V	1.4 ns	1.4 ns	525 pF
t_d	R_{dson}	$R_{ESR,C}$	k
13.33 ns	7.7 mΩ	1.39 $m\Omega$	0.773

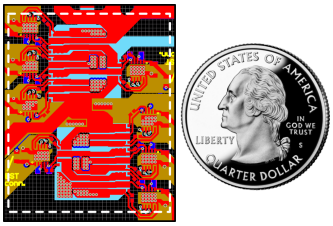

Fig. 12. The PCB layout of the rectifier power stage (switches, power capacitors, gate drivers, and bootstrap circuitry) with a US quarter for size reference. The white dotted line measures 31.4 mm x 27.5 mm.

A 5 V DC bias derating is considered for the flying capacitance (C_{xx}). Four parallel 10 V, 0603 capacitors (C1608JB1A226M080AC) have measured total capacitance of 15.66 µF and 1.39 mΩ at 5 V bias, as shown in Table III. Because the flying capacitors are much larger than C_s and are only periodically inserted into the power path, the value of C_{xx} does not affect the WPT tank resonance.

Values V_d, C_{oss}, and R_{dson} are derived from the datasheet. $R_{ESR,C}$ is found by measuring a flying capacitor at 150 kHz. Times t_{on} and t_{off} are calculated using a gate drive current of 1 A and the Q_{gs} value from the device datasheet, and t_d is set as two clocks from the 150 MHz FPGA digital modulator.

With the component values defined in Table III, the worst case charge redistribution is calculated to ensure that the

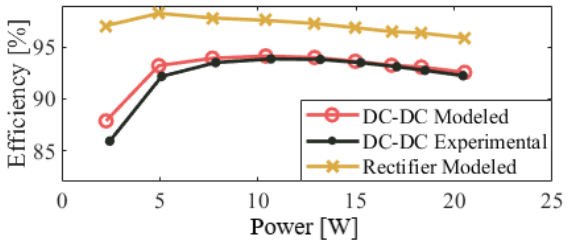

Fig. 13. DC-DC experimental data compared to the model for 2.45 W to 20.45 W, including the modeled rectifier efficiency for reference.

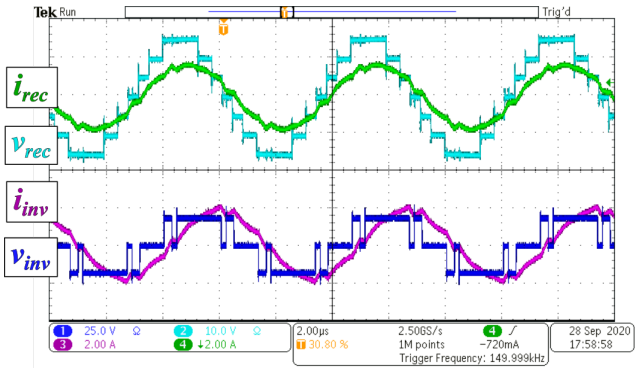

Fig. 14. Experimental waveforms of the circuit at $P_{out} = 13.18$ W.

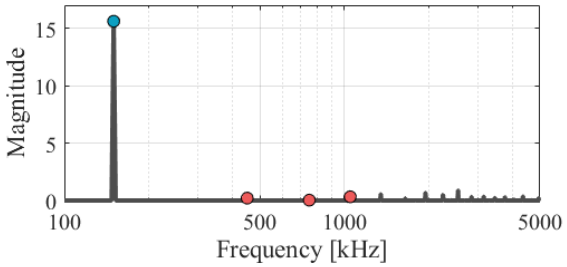

Fig. 15. Spectrum of the v_{rec} waveform in Fig. 14.

system operates according to the slow switching limit, i.e. the flying capacitors completely balance with V_{load} each cycle. The minimal allotted time for charge redistribution is one half period, $T_s/2 = 1/(150\text{ kHz}) \cdot 1/2 = 3.33$ µs. The worst cast charge redistribution time constant is calculated by $\max(\tau) = (4R_{dson} + 2R_{ESR,C})C_{xx} = 0.53$ µs. Therefore, in the worst case, $3\tau_{wc}$ uses only 47% of the allotted time to achieve greater than 95% charge redistribution. Losses could be further reduced by increasing each flying capacitance C_{xx} until the FSL is reached, at the expense of greater board area.

The power stage shown in Fig. 12 is responsible for carrying the full power currents of the rectifier. The other circuitry that can be seen on the rectifier circuit board (upper PCB) in Fig. 10 is comprised of DC voltage connectors, isolators, and digital control circuitry. Fig. 12 compares the rectifier power stage and a US quarter to convey the density of the layout. Without the need for bulky DC inductance, the rectifier is laid out to be a very small footprint. This compactness serves to reduce trace inductance and resistance, and it therefore also reduces consequent high frequency ringing and conduction loss. At $P_{out} = 20$ W, the power density of the MSC is 74.42 W/in^3. Notably, the only components on the bottom side of the board are bootstrap capacitors, so maneuvering only a few elements increases the power density to $\approx 103\text{ W/in}^3$.

The 7-level SC rectifier enables output regulation without the need for a bulky filter inductance or discrete steps in voltage conversion. However, the layout in Fig. 12 only begins addressing the MSC's full potential to be a power dense topology. The experimental power density is limited by the use of discrete components; in the future, power stage integration onto a single IC, with only external capacitors, can substantially increase power density.

A. Experimental Data and Waveforms

Fig. 13 shows a comparison of the DC-DC experimental efficiency to the modeled DC-DC efficiency. Good agreement validates the modeling approach put forth in this paper. The modeled rectifier efficiency is included and remains bounded between 95.9% and 98.3% for all surveyed points. One example test point is isolated from the 9 experimental points in Fig. 13, and its waveforms are shown in Fig. 14. This point occurs at $P_{out} = 13.18$ W, demonstrates excellent efficiency, and maintains exceptionally low distortion. The two waveforms near the top of Fig. 14 are the rectifier input: v_{rec} and i_{rec}. The two bottom waveforms are the tank input (or inverter output): v_{inv} and i_{inv}.

TABLE IV
WAVEFORM DISTORTION IN FIG. 14

	1^{st}	3^{rd}	5^{th}	7^{th}	THD_7	THD_∞
v_{rec} [V]	15.60	0.20	0.03	0.32	2.44	12.51
i_{rec} [A]	1.70	0.02	0.00	0.01	1.17	7.27
v_{inv} [V]	18.80	0.36	0.06	0.12	2.03	45.19
i_{inv} [A]	1.79	0.03	0.00	0.01	1.99	7.48

The THD_7 and THD_∞ of a square wave are 41.1% and 48.3%, respectively.

The operating point is taken with a DC input voltage of 18.46 V and a DC output voltage of 5 V. The DC currents at the input of the inverter and the output of the rectifier are recorded. The oscilloscope waveform data shown in Fig. 14 is exported and processed in MATLAB. The fundamental voltage, current, and impedance of the rectifier are calculated for comparison with the model. This operating point occurs at $|Z_{rec,1}| = 9.2\ \Omega$ and $\angle Z_{rec,1} = 14.6°$. Matching this impedance to the model, the predicted output power and efficiency of 12.8 W and 93.5% are shown to be in good agreement with the experimental results of 13.2 W and 93.8%.

The waveform data is also evaluated for harmonic content. Fig. 15 shows the spectrum of waveform v_{rec} from Fig. 14.

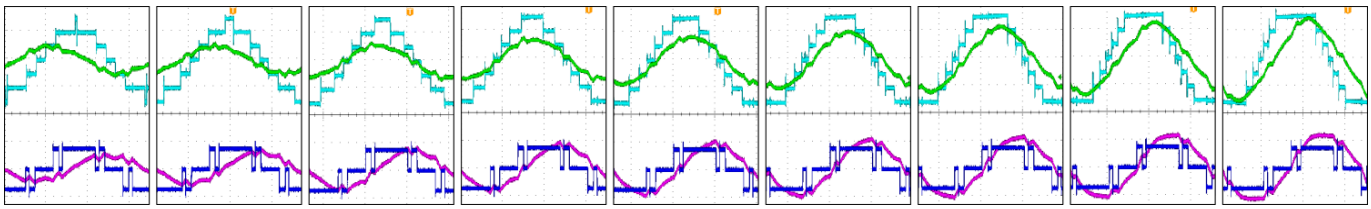

Fig. 16. Waveforms of experimental test points. Each image is a different experimental operating point with consistent oscilloscope scaling, laid out such that output power increases from left to right. The central image is repeated from Fig. 14

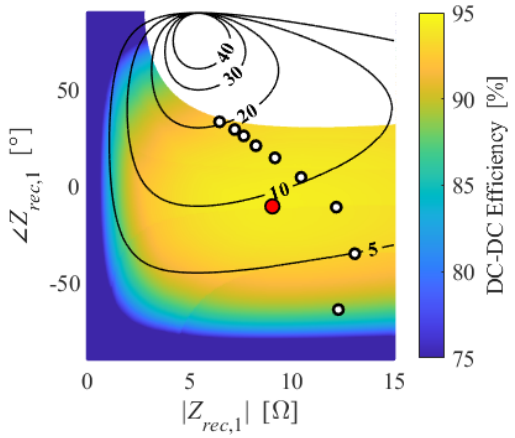

Fig. 17. Experimental data points overlaid on the complete loss model showing the efficiency (color gradient), power contours (black lines), and unreachable area (white) for $V_{load} = 5$ V.

As predicted, the 3rd, 5th, and 7th harmonics are significantly smaller than the fundamental component. Total waveform THD is calculated using

$$\text{THD}_i(x) = 100 \cdot \frac{\sqrt{\sum_{n=2}^{i} x_n^2}}{x_1}, \tag{18}$$

where x_n is the RMS value of the n^{th} harmonic and x_1 is the RMS value of the fundamental component. The THD_7 of v_{rec} in Fig. 14 is 2.44%.

In the experimental waveforms, the full-bridge inverter employs additional switching actions for further harmonic elimination. When harmonic content is reduced at both WPT voltages (v_{inv} and v_{rec}), the currents in the WPT tank are subject to significantly less distortion [31, 33]. The distortion considering only the 1^{st}-7^{th} harmonics, THD_7, and the THD + noise, THD_∞, values for each waveform in Fig. 14 are reported in Table IV. The distortion is quite low through the 7^{th} harmonic, but higher frequency noise (including switching) contributes to a larger degree of distortion when including all harmonics, especially in the case of v_{inv}.

B. Complete Experimental Power Sweep

Every experimental point is conducted without deviation from the parameters in Table III. Fig. 17 shows the total modeled system efficiency, output power, and reachable operating area. Output voltage $V_{load} = 5$ V remains constant, the modulation necessary to reach the white region ($M > 3.81$) is unattainable with the 7-level design, and the contour lines identify powers of up to 40 W. The experimental data points are overlaid on the modeled data for visualization of how the rectifier impedance is used to traverse the operating region. Each experimental point is comprised of a different modulation index, control phase, and DC load, resulting in a range of output powers from 2.45 W to 20.45 W. This experimental trajectory through the operating space is near-optimal. The red dot indicates the peak system-wide efficiency, which is less than 0.5% higher than the nearest modeled test point.

The waveforms of each of these test points are summarized in order of ascending output power in Fig. 16. The modulation index increases with power, as does the phase at the input of the rectifier. To control the experimental test, the phase between v_{rec} and v_{inv} is varied, which can be seen clearly in Fig. 16. Note that Figs. 13, 16, 17, and 18 all refer to the same set of data points.

Fig. 18 gives detail about the loss distributions, THD_7, and impedance of the experimental results. The modeled loss distribution in Fig. 18a shows that the tank and rectifier losses scale with power while the inverter losses remain nearly constant. The black line (and corresponding set of dots) is obtained by locating the point of minimal tank conduction loss for each power contour on Fig. 17, which results in the optimal loading trajectory per fundamental conduction losses. By comparing this line to the blue "Tank" bars, Fig. 18a illustrates how closely the experimental data set matches the optimal trajectory for tank efficiency. Because V_{in} is constant for the entire experimental data set, the high-efficiency traversal from 2 to 20 W via controlling Z_{rec} does not require coordinated control with the inverter for power regulation.

The rectifier loss distribution in Fig. 18b is also model-based. The switching loss is a very small portion of the loss profile, and both the charge sharing and conduction losses are heavily influenced by increasing power.

Furthermore, a straightforward manipulation of (16) and (17) provides insight into how Fig. 18b changes with C_{xx} size. For a constant steady state operating point, if $\sigma = |i_{rec}|/\omega \cdot \big(\cos(t_x\omega + \phi) - \cos(t_{7-x}\omega + \phi)\big)$, then (17) is written as

$$P_{cs} = \sigma^2/2C_{xx}\ , \tag{19}$$

showing that charge sharing loss is inversely proportional to

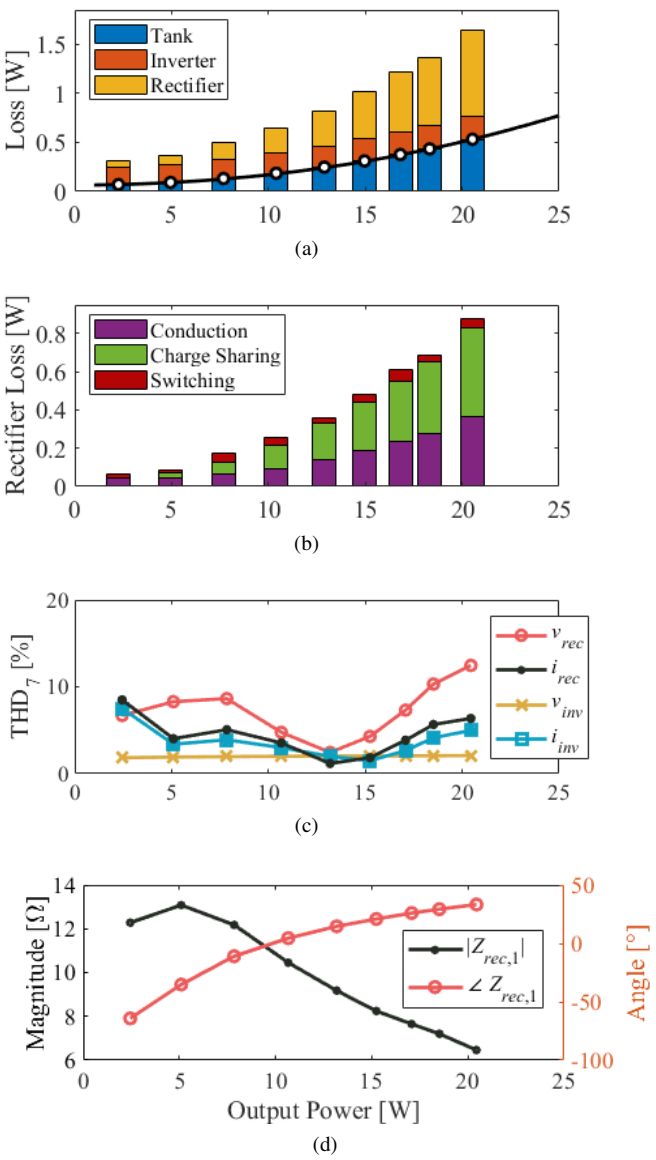

Fig. 18. Experimental results of (a) the loss profile of the system, (b) the loss profile of the rectifier, (c) the harmonic distortion of all tank waveforms, and (d) the fundamental impedance of the rectifier.

the amount of flying capacitance. Take the highest power operating point in Fig. 18b as an example. The charge sharing loss is $\approx$ 400 mW for $C_{xx} = 15.66$ µF. If three of the four parallel capacitors used to implement C_{xx} were removed, the volume of each capacitor would reduce by 75%, but the charge sharing loss would increase to ≈ 1.6 W at $C_{xx} = 4$ µF.

Fig. 18c shows the experimental total harmonic distortion through the 7^{th} harmonic for each waveform in the WPT tank. The waveforms remain at relatively low levels of distortion throughout the power sweep; the highest recorded THD remains below 13%. This result is a significant improvement relative to the square waveforms in a traditional WPT system. The THD_7 of a square wave is 41.41%, but the THD_7 of v_{rec} is experimentally demonstrated to be much lower, bounded from 2.44% to 12.46%.

Fig. 18d shows the fundamental impedance (magnitude and phase) of the rectifier over the testing range. This plot characterizes the two axes of Fig. 17 and shows more clearly how the impedance of the rectifier can directly influence the power throughput of the system without significantly degrading system efficiency. In this set of test points alone, the MSC showcases low power operation and high power operation, consistently high efficiencies, resistive loading capability ($\angle Z_{rec,1} \approx 0$), and dramatically reduced harmonic content. Each of these is achieved without externally adjusting the WPT coupling factor, tank tuning, inverter voltage, or fundamental operating frequency.

To demonstrate the MSC topology under different WPT tuning conditions, the primary and secondary side coils (originally tuned at 50 kHz and 131 kHz) are retuned to 131 kHz and 150 kHz, respectively. Other than the new values of C_p and C_s, the same hardware is used, and the system is tested up to 19.86 W. Here, V_{in} is varied to compliment the desired output power. The MSC once again performs at a consistently high efficiency, with system-wide DC-DC measurements of 95.12% at 8.5 W and 92.95% at 19.85 W. Fig. 19 shows the waveforms of the 8.5 W operating point. The MSC topology is able to maintain a high efficiency under a wide range of WPT tank tuning and alignment scenarios.

Finally, Table V is included for comparison to other work with similar operating frequencies and output power levels. Table V includes THD values for holistic comparison. Measured values from prior literature are included whenever available and theoretical values are used otherwise; harmonic orders are reported in parentheses for measured results. Nevertheless, Table V shows the MSC in this work to be the only solution to simultaneously exhibit full step-up, step-down, and phase control while also demonstrating low THD without the need for bulky power inductors.

Two noteworthy challenges of MSC design are the number of switches and the amount of capacitance. Under the 5 V DC bias, the six flying capacitors have total capacitance nearly 94 µF, and the number of switches is significantly higher than other approaches.

As with other multilevel converters, the total semiconductor area required is comparable to that of two-level implementations for the same power and input voltage v_{rec} due to the low voltage stresses on each individual device balancing the higher device count [8, 34]. SMD capacitors maintain a low profile, very low ESR, and high power density relative to filter inductors [7, 8].

In Table V, the MSC topology exhibits superior performance in many metrics due to the ability to use the staircase waveform to simultaneously achieve multiple objectives, providing near-optimal system loading and high efficiency loading while simultaneously providing control and low harmonic content in a small footprint without bulky inductors. In alternative implementations, one-or-more aspect must be sacrificed. With full impedance control, the highest efficiency, and the lowest distortion, the topology showcases some significant advantage over each of the other approaches listed in Table V. Overall,

TABLE V
COMPARISON TO OTHER PUBLISHED WPT RECTIFIERS

Reference	f_s	Rectifier	Control		k	P_{out}	V_{out}	η_{dc-dc}	THD$_i$ v_{rec} (i)	Rectifier Component Count		
			$\lvert Z_{rec}\rvert$	$\angle Z_{rec}$						Inductors	Switches	Capacitors
[11]	515 kHz	DHB + Boost dc-dc	↑	no	≈ 0.2	17.7 W	100 V	85%	$\approx 48\%$[2]	1 (dc-dc)	1+3D	2
[5]	200 kHz	Active Diff. Class E	↑	yes	0.71	24 W	12 V	90%	7.16% (10$^{\text{th}}$)	2 (coupled)	2	1
[35]	200 kHz	Semi-active HB	↑	yes	–	16 W	24 V	–[1]	46.3% (10$^{\text{th}}$)	0	1+1D	1
[22]	205 kHz	AFB + Buck dc-dc	↑ / ↓	yes	0.6	11.2 W	4 V	77.3%	$\approx 48\%$[2]	1 (dc-dc)	6	2
[24]	100 kHz	Sync FB + LDO	↓	no	–	5.3 W	5.3 V	76%	$\approx 48\%$[2]	0	4	2
This Work	150 kHz	MSC	↑ / ↓	yes	0.77	20 W	5 V	93.8%[3]	2.44%[3] (7$^{\text{th}}$)	0	16	7

[1] No dc-dc efficiency given; rectifier ac-dc efficiency is $\approx 98\%$
[2] Theoretical value for squarewave, consistent with reporting in [5]
[3] Values at $P_{out} = 13.8$ W.

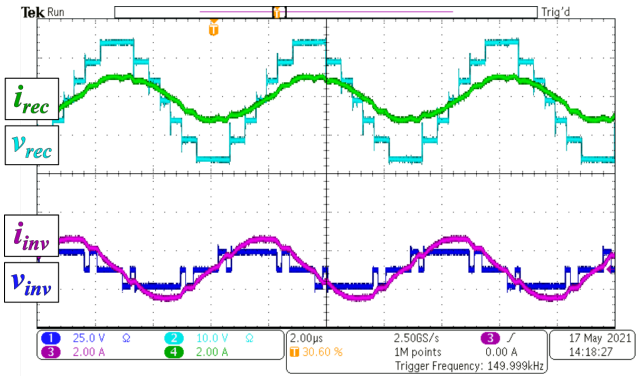

Fig. 19. Experimental waveforms of the retuned circuit at $P_{out} = 8.5$ W.

the MSC approach manages highly efficient direct charging of a 5 V output without the need for an additional dc-dc converter.

VII. CONCLUSIONS

A 7-level switched capacitor rectifier is constructed in a 150 kHz wireless power transfer system. The rectifier is compact, efficient, real-time tunable, and capable of reducing waveform distortion. An FHA circuit model is constructed to include conduction, switching, and charge sharing losses. The inverter and rectifier are both experimentally switched to reduce waveform harmonic content.

The experimental data points are laid over the model in terms of Z_{rec} to convey how the rectifier's tuning capabilities enable traversal of the WPT operating region. The modeled DC-DC efficiency is shown to be in good agreement with the experimental data, and the modeled rectifier efficiency is between 95.9% and 98.3% for all tested power levels. THD is also low across the full power sweep, validating the MSC as a strong candidate for highly efficient, compact rectification in consumer device wireless power transfer applications.

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