A 4-way Nested Digital Doherty Power Amplifier for Low-Power Applications

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***Abstract*—This paper demonstrates the advantages of a nested digital Doherty power amplifier (PA) to achieve high efficiency in deep power back-off (PBO) for low-power applications. A differential 4-way digital Doherty PA is implemented in a general purpose 65 nm CMOS process as a proof-of-concept that ideally achieves efficiency enhancement through 9 dB PBO. The PA uses a compact input and output matching network through consolidation of components, and it achieves a peak drain efficiency (DE) of 48% and system efficiency (SE) of 31% with 7.3 dBm of output power (P_{out}) and 14 dB of gain at 4.75 GHz. It also obtains a DE of 42% and 20% at 0 dB and 12.8 dB PBO, respectively, at 5.25 GHz, which corresponds to a 2.2× improvement over normalized class B PA. Finally, RF modulation measurements performed on the PA show that it achieves a DE of 34% and an r.m.s error vector magnitude (EVM_{rms}) of -20.5 dB for a 1 MSym/s 16 QAM RF waveform at 5.25 GHz.**

***Index Terms*—Compact matching network, complementary metal-oxide-semiconductor (CMOS), differential power amplifier, digital Doherty, Internet of Things (IoT), low-power.**

I. Introduction

EMERGING applications, such as agriculture monitoring, inventory tracking, and smart home connectivity require ultra low-power ad-hoc sensor networks [1]. These networks are composed of transceiver nodes that can benefit from a compact form-factor. Since antennas dominate the overall volume of such nodes, increasing the frequency of operation is desirable to reduce the antenna size. However, reducing the volume of these nodes limits the battery capacity, which in turn affects their lifetime. Since the power amplifier (PA) is the most power-hungry component of this system, there is a need for high-efficiency PAs for low-power applications ($<$ 10 dBm). Also, the nodes in these ad-hoc networks can form asymmetric links with the base-station, where the use of higher-order modulation schemes can reduce the energy consumption per bit by keeping the PA turned on for a shorter period of time [2]. Such nodes can benefit from PAs with high efficiency in deep power back-off (PBO) to further extend their lifetime. Therefore, a 4-way nested Doherty PA operating around 5 GHz is proposed for such applications.

Current state-of-the-art low power PAs are implemented digitally [2], [3], as this facilitates the integration of the PA into the transmitter. Typically, they use advanced topologies such as class D [4]–[6] and class E/F_2 [7], [8] to improve the efficiency at maximum output power, but the efficiency deteriorates in PBO. To improve the performance of a digital PA [9]–[13] in back-off, it can be used in conjunction with the popular Doherty architecture [14], [15]. However, it offers improvement to only about 6 dB PBO [16]–[18]. A class G technique [19], applied to the Doherty architecture, has been shown in the literature to boost the performance of PAs in deep PBO [20]–[22] for high-power applications ($>$ 25 dBm). However, it relies on switching the V_{DD} of the PA to a lower value to achieve efficiency enhancement. This technique is challenging to scale down to PAs with low output power ($<$ 10 dBm) operating at higher frequency ($\sim$ 5 GHz), as described in Section II.

In the past, the use of multi-way analog Doherty architectures [23], [24] has been limited due to linearity concerns of the over-driven main amplifier. The main amplifier saturates in deep back-off when the input swing is relatively small, and when the input swing is increased to saturate the auxiliary amplifiers, the main amplifier is driven in deep saturation, causing non-linearities [25]. Recent digital implementations of multi-way combiner based Doherty architectures, such as the Nested Doherty PA illustrated in Fig. 1, have overcome the linearity concern related to the over-driven main amplifier since they require the input swing to remain constant, and they have been shown in the literature to offer improved efficiency in deep PBO [26], [27]. In this work, a differential 4-way

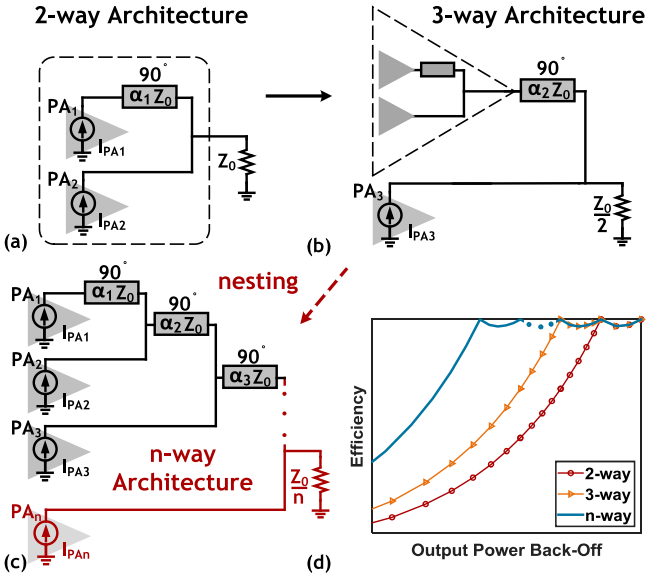

Fig. 1. Extension of a generic (a) 2-way Doherty architecture to (b) 3-way, and to (c) n-way through nesting, which results in (d) 2, 3, and n efficiency enhancement peaks, respectively, in power back-off (PBO).

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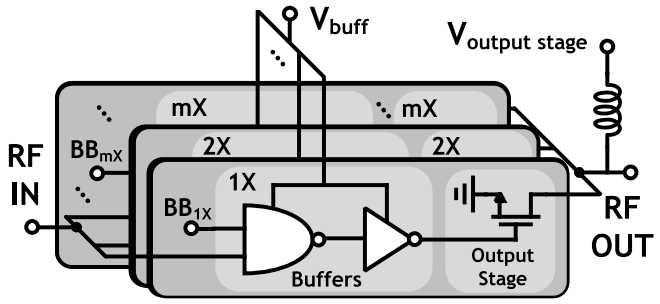

Fig. 2. Digital implementation of a power amplifier (PA) block consists of multiple unit cells, where each unit cell is composed of a set of digital buffers and a common source output stage.

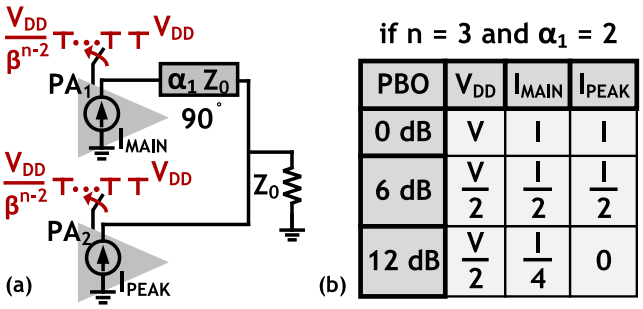

Fig. 3. (a) A generic n-way class G Doherty architecture with $n-2$ V_{DD}s resulting in n efficiency enhancement peaks, and (b) desired current drive strengths of the main and the peaking amplifier for case n = 3 and α_1 = 2.

digital Doherty PA (D4DPA) is proposed that can theoretically maintain optimal matching for enhanced efficiency up to 9 dB PBO. It achieves a maximum output power (P_{out}) of 7.3 dBm at 4.75 GHz with peak drain efficiency (DE) of 48% and system efficiency (SE) of 31%. It also achieves a 2.2× DE improvement compared to normalized class B PA at 12.8 dB PBO at 5.25 GHz, and a DE of 34% for a 1 MSym/s 16 QAM RF waveform.

This paper is an expansion of [28], and it offers increased detail in analysis, extensive simulations, and additional measurements of the proposed D4DPA, compared to the conference version. Section II provides an in-depth analysis of the advantages offered by the nested architecture for current mode digital PAs with low output power. The design of the D4DPA is discussed in Section III with the help of an asymmetric Doherty architecture that achieves efficiency enhancement at an arbitrary back-off level. The implementation and simulations of the PA along with the matching networks and quadrature hybrid are presented in Section IV. Continuous wave (CW) and modulation measurements are shown in Section V, and conclusions are drawn in Section VI.

II. Nested Doherty Architecture for Low Output Power Digital PAs

Presenting an optimal load to the PA is crucial to achieve maximum voltage swing on the transistor's drain, and thus maximum efficiency. For a class B PA, the presented impedance is optimal only at the maximum output power. As the output power decreases, the voltage swing also decreases, leading to degradation in efficiency. The traditional Doherty architecture overcomes this challenge and improves efficiency through 6 dB PBO. This architecture is composed of a main amplifier, a peaking amplifier, and an impedance inverter. At maximum output power, the main and the peaking amplifier work collectively to present the optimal impedance. At 6 dB PBO, the peaking amplifier turns off completely, and the inverting network doubles the impedance presented to the main amplifier. This re-maximizes the voltage swing and leads to efficiency enhancement, as shown in Fig. 1(d). Thus, such an architecture leads to 2 efficiency enhancement peaks; however, the efficiency degrades beyond the second peak.

To improve performance in deep PBO, multiple PA blocks and multiple inverter networks can be used to form a nested Doherty architecture, as depicted in Fig. 1(c). As the amplifier is pushed in PBO, the PA blocks start turning off sequentially from PA_n to PA_2. With each PA block turning off, the efficiency of the amplifier ideally boosts back to its maximum value due to the optimal impedance presented by the inverter networks. Thus, an n-way architecture with n PA blocks and $n-1$ inverter networks produces n efficiency enhancement peaks, as shown in Fig. 1(d).

The nested Doherty architecture, for this work, is implemented using current mode digital PA blocks. Current mode based digital PAs [12], [29]–[31], and current mode based digital Doherty PAs [16] have been demonstrated to operate at high frequencies ($>$ 3.5 GHz) with some of the highest reported drain efficiencies at high output powers in the literature. They have the potential to offer some of the same advantages for low output power PAs as well [4], [7]. Such a digital PA consists of multiple unit cells, as shown in Fig. 2. Each unit cell is composed of a final output stage that is usually driven by a set of digital buffers. Ideally, the power lost in the buffers would be relatively low compared to the power lost in the output stage to achieve high system efficiency. However, as frequency increases, the power lost in these buffers also increases linearly as CV^2f. Additionally, for low output powers, the PAs typically employ lower V_{DD}s ($< 1V$) to improve drain efficiency, but this limits their voltage gain, which further increases the relative power dissipated in the buffers. Therefore, the power lost in the buffers cannot be ignored for the proposed applications.

The buffer power dissipation becomes especially crucial in deep PBO, and the use of a nested Doherty architecture can help improve system efficiency, especially in comparison to other efficient PBO architectures, including the V_{DD} switching class G Doherty PA shown in Fig. 3. This improvement, particularly in lower output power applications such as IoT nodes, can be highlighted using two different models with increasing accuracy: 1) ideal transistor model, where switching the V_{DD} does not affect current drive of the output stage, and 2) Drain source voltage (V_{ds}) dependent transistor model, where current drive is affected due to non-linearity of the transistors. Both scenarios assume ideal lossless matching networks, and they both neglect the additional power lost due to the switches of the class G Doherty architecture.

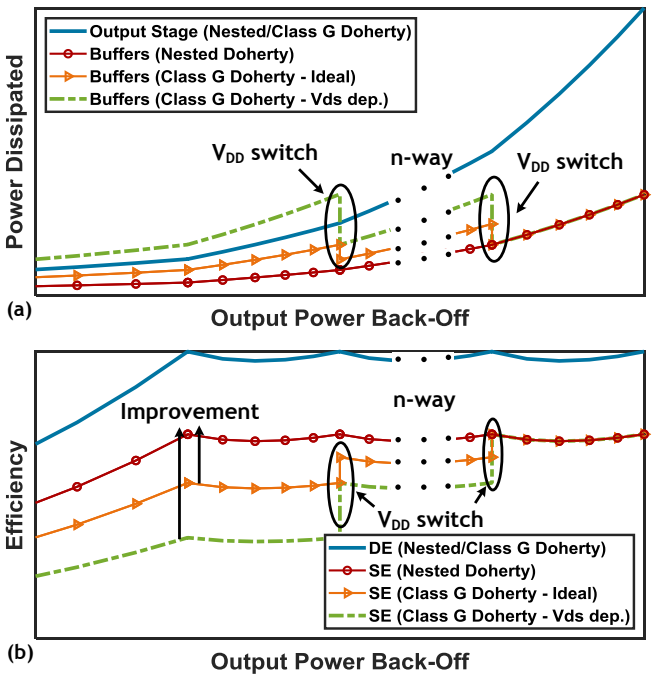

Fig. 4. Comparison of nested Doherty with class G Doherty architecture in power back-off using the ideal and the V_{ds} dependent transistor model. (a) Power dissipation trend in the output stage and buffers. (b) Drain efficiency of the output stage and system efficiency trend of the whole PA.

A. Ideal Transistor Model

For the nested Doherty architecture, as each PA block is turned off, the digital buffers within that PA block can be turned off as well. Thus, the power lost in the buffers is reduced proportionally to the reduction in the output power, as illustrated in Fig. 4(a). Therefore, when the drain efficiency enhancement is achieved, the system efficiency also returns to its maximum value, as shown in Fig. 4(b).

In contrast, the system efficiency of class G digital Doherty architecture degrades in back-off. This architecture operates by switching its supply to a lower V_{DD} in deep PBO, as shown in Fig. 3(a). However, to satisfy the Doherty behavior and achieve drain efficiency enhancement, the power lost in the digital buffers is not reduced proportionally to the reduction in output power. For example, a simple implementation of a class G Doherty PA, depicted in Fig. 3(b), shows that when

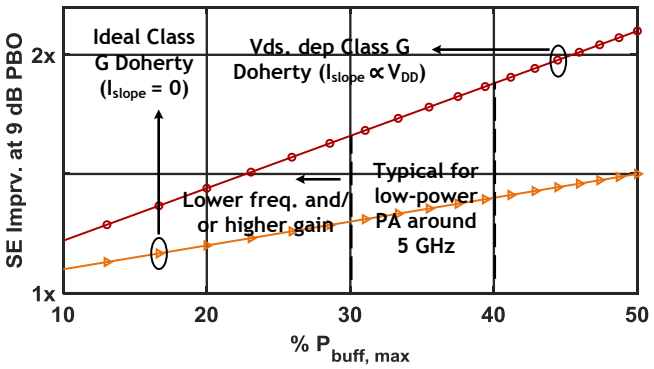

Fig. 5. Improvement offered by nested Doherty PA over class G Doherty PA dependent on the relative buffer power consumption at 9 dB PBO. Losses in the output matching network and the switches of class G are ignored.

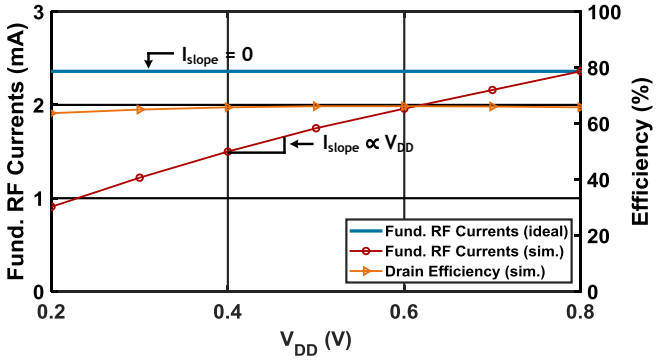

Fig. 6. An example showing the effect of lowering V_{DD} on a common source stage driven with a constant amplitude voltage swing. Simulation performed in a general purpose 65nm CMOS process with optimum impedance presented at each V_{DD} value to obtain full swing at the output.

the output power is reduced by 6 dB, the main and the peaking PA desire half their maximum currents. This implies that half the number of digital cells need to be "on". So even though the output power drops by a fourth, power dissipated by the buffers is only halved, thereby increasing relative losses through the buffers. This issue can be extended to an n-way architecture with $n-2$ V_{DD}s, and the resulting reduced system efficiency due to increase in n is represented in Fig. 4(a)

The efficiencies in PBO of the two architectures are compared in Fig. 4(b). The jumps in the system efficiency, for the class G Doherty PA, occur when the V_{DD} switches to a lower value, and thus higher power is consumed in the buffers. The improvement offered by the nested Doherty PA over class G Doherty PA depends on the relative power lost in the buffers, which is defined as follows:

$$\%\ P_{buff,max} = \frac{P_{buff}}{P_{buff} + P_{output\ stage}} \times 100 \Bigg|_{Pout,max} \quad (1)$$

The above metric is defined at maximum output power level to enable comparison between the two architectures. From simulations in a 65 nm CMOS process at 5 GHz and output stage V_{DD} of 0.55 V, the expected power lost in the buffer accounts for about 30% to 40% of the total power dissipation. This results in a system efficiency improvement of 1.3× to 1.4× for the nested Doherty architecture at 9 dB PBO, as shown in Fig. 5.

B. Drain-Source Voltage (V_{ds}) Dependent Transistor Model

For PAs with low V_{DD} ($< 1V$), the current drive of the transistor is severely affected when the V_{DD} is lowered even further. This current drive depends on the input voltage swing provided to the gate of the device. Since the transistors are driven by digital buffers, the amplitude of this voltage swing remains constant, regardless of whether the V_{DD} of the output stage is lowered. Therefore, in deep PBO, portions of the input swing can exceed V_{DD} and push the transistor in the triode region leading to reduced RF transconductance and thereby, reduced current drive. To overcome the current drive reduction and to achieve enhanced drain efficiency, more digital cells need to be turned "on", which further increases the relative power dissipated in the buffers. For an n-way class G Doherty architecture, as n increases, the buffers can potentially

dissipate more power than the output stage in PBO, as shown in Fig. 4(a). This severely affects system efficiency.

In comparison, the nested digital Doherty architecture does not encounter this issue because the V_{DD} always remains constant. Fig. 6 depicts an example simulation performed in a 65 nm CMOS process on a common source stage, to show the effect of V_{ds} dependency on current drive. Taking this simulation and Equation (1) into account, the improvement offered by the nested Doherty architecture is calculated. It has the potential to improve the system efficiency by approximately 1.6× to 1.9× at 9 dB PBO, shown in Fig. 4(b) and Fig. 5.

It is important to note that the efficiency of the output matching network (passive efficiency) in a nested Doherty architecture degrades with PBO; however, the passive efficiency of a class G Doherty architecture enhances back to its maximum value when the V_{DD} is switched [20]. Therefore, the output matching network of the nested digital Doherty architecture needs to be designed with care to achieve the improvements described in the above sections.

III. Design of a 4-way nested Doherty PA

In this work, a 4-way nested Doherty architecture is implemented to achieve efficiency enhancement in 3 dB increments through 9 dB back-off. The 3 dB increment also helps the PA ideally maintain its efficiency close to the maximum value through the whole enhancement range.

The design of the proposed 4-way PA can be explained through an asymmetric 2-way Doherty architecture that achieves efficiency enhancement at an arbitrary back-off level. This arbitrary level is dictated by two design parameters: 1) the characteristic impedance of the inverter network, and 2) the ratio of the main and peaking amplifier's maximum current drive. These parameters are constrained as

$$\frac{Z_{Tline}}{Z_0} = \alpha_1 \tag{2}$$

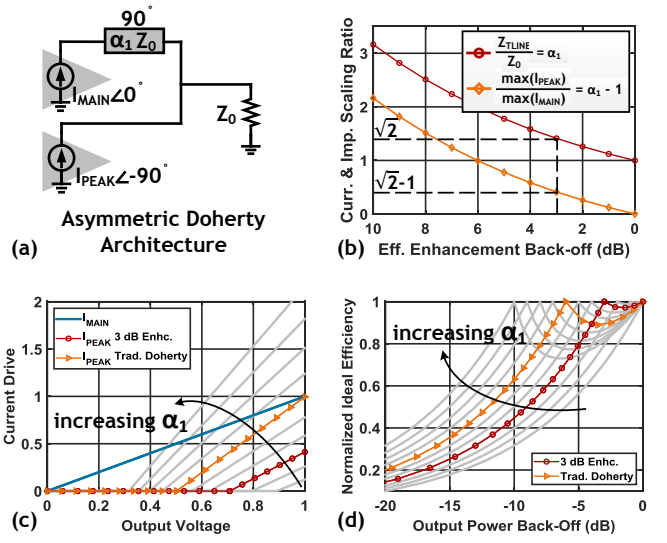

Fig. 7. (a) Asymmetric Doherty architecture designed using (b) scaling ratios to generate the inverting network impedance and (c) current drive strengths of the main and peaking amplifier that result in (d) efficiency enhancement at an arbitrary back-off level.

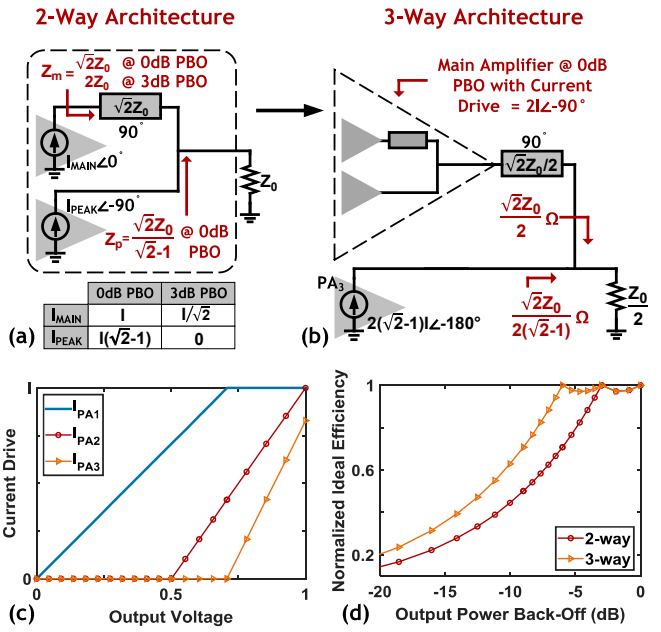

Fig. 8. (a) Asymmetric 2-way Doherty architecture that enhances efficiency through 3 dB PBO, which extends to (b) a 3-way architecture through current drive strengths shown in (c) to achieve (d) efficiency enhancements at 3 dB and 6 dB PBO.

$$\frac{\max(I_{Peak})}{\max(I_{Main})} = \alpha_1 - 1 \tag{3}$$

where α_1 denotes the back-off level on a linear scale where efficiency enhancement is achieved [32]. Consequently, α_1 also denotes the back-off level where the peaking amplifier turns off. Equations (2) and (3) can be intuitively explained through Fig. 7. Here, the current profile of the main amplifier is left constant, while that of the peaking amplifier is varied, along with the characteristic impedance of the inverter network. The resulting current profiles of the peaking amplifier and the resulting back-off efficiency curves are depicted in Fig. 7(c) and (d), respectively. These curves lead to efficiency enhancement from 1 dB PBO to 10 dB PBO in 1 dB steps.

In order to achieve efficiency enhancement at 3 dB PBO, the asymmetric Doherty architecture can be designed with

$$\alpha_1 = \sqrt{2} \implies Z_{Tline1} = \sqrt{2}Z_0 \tag{4}$$

$$\max(I_{Main}) = I \tag{5}$$

$$\max(I_{Peak}) = I(\sqrt{2} - 1) \tag{6}$$

as depicted in Fig. 7(b). At maximum output power level, the two amplifiers work collectively, and the inverting network ensures that optimal impedances are presented to both the amplifiers. These impedance values, mentioned in Fig. 8(a), lead to maximum efficiency. In back-off, the current drives of both the amplifiers decrease according to Fig. 7(c), and at 3 dB PBO, the peaking amplifier turns off completely, while the current drive of the main amplifier decreases by a factor of $\sqrt{2}$. However, the inverting network boosts the impedance presented to the main amplifier by the same factor of $\sqrt{2}$ to maximize the voltage swing, resulting in efficiency enhancement at 3 dB PBO, as depicted in Fig. 8(d).

To further improve the performance in back-off, this concept can be extended to a 3-way architecture through nesting. As shown in Fig. 8(b), PA_1 and PA_2 can be combined and considered as the “main" amplifier with current drive of 2I, at 0 dB PBO. Now, the overall architecture looks very similar to the 2-way architecture, except that the “main" amplifier has twice the current drive strength. So the rest of the design parameters are scaled accordingly:

$$\alpha_2 = \sqrt{2} \;/\; 2 \quad \Longrightarrow \quad Z_{Tline2} = (\sqrt{2}Z_0) \;/\; 2 \tag{7}$$

$$\max(I_{PA3}) = I(\sqrt{2}-1)\times 2 \tag{8}$$

The resulting impedances, at 0 dB PBO, are mentioned in Fig. 8(b). As expected, these impedances are half of those from the 2-way architecture, since the equivalent current drive strength has been doubled. From 3 dB PBO onward, PA_3 turns off, leading to the same design as that of the 2-way architecture, which results in another efficiency enhancement peak. Overall, the 3-way architecture obtains three efficiency peaks, as illustrated in Fig. 8(d).

This concept is further extended to a 4-way nested architecture, as presented in Fig. 9(a), where each amplifier block is biased individually to generate the RF current drives, as shown in Fig. 9(c). These values for current drives are obtained by extension from the 3-way architecture, where

$$\alpha_3 = \sqrt{2} \;/\; 4 \quad \Longrightarrow \quad Z_{Tline3} = (\sqrt{2}Z_0) \;/\; 4 \tag{9}$$

$$\max(I_{PA1}) \;=\; \max(I_{PA2}) \;=\; I \tag{10}$$

$$\max(I_{PA3}) = I\times 2 \tag{11}$$

$$\max(I_{PA4}) = I(\sqrt{2}-1)\times 4 \tag{12}$$

The impedances seen by the amplifiers during back-off are plotted in Fig. 9(d), and they lead to 4 efficiency enhancement peaks through 9 dB PBO as depicted in Fig. 9(b). Here, $Z_0/4$ corresponds to 50 Ω to avoid the need for additional impedance transformation at the output.

IV. Implementation and Simulations

The proposed D4DPA is implemented in a general purpose 65 nm CMOS process, as a proof-of-concept. As mentioned in Section III, presenting the optimal impedances is crucial to achieve high efficiency, especially in back-off. To prevent the matching network from de-tuning due to the parasitics of the wirebonds, a differential architecture is implemented. This provides a virtual short on-chip for the fundamental frequency, so the matching network is not solely reliant on bypass capacitors.

Although the transmission lines, shown in Fig. 9(a), can be implemented using either a high-pass equivalent or a low-pass equivalent LC network, the high-pass equivalent offers two advantages: 1) reduced total number of inductors through consolidation, and 2) reduced inductance values. The high-pass equivalent LC, along with the inductors used to resonate the drain capacitance and provide biasing, lead to an output matching network design with 10 inductors, as depicted in Fig. 10. However, various inductors can be consolidated, such as L_1, L_2, and L_{res2} can be reduced to simply L_{eq2}. Overall,

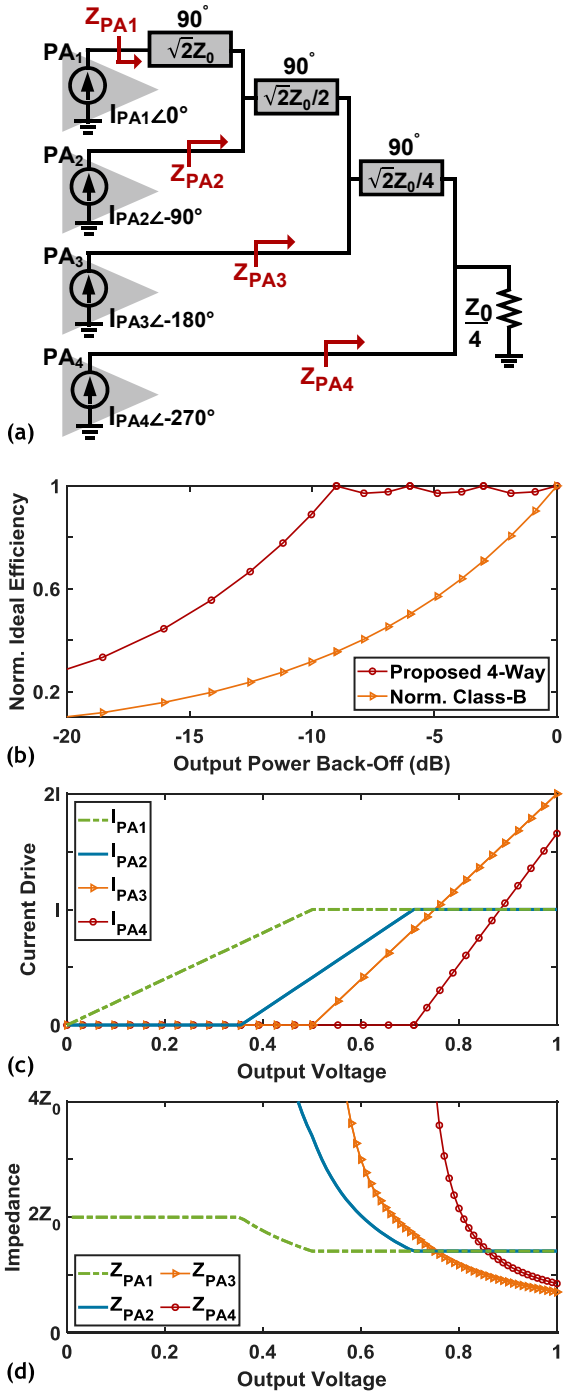

Fig. 9. (a) Proposed 4-way Doherty PA architecture to maintain optimal matching through 9 dB PBO, yielding (b) efficiency enhancements by (c) scaling RF current drives to (d) produce the desired optimal output impedances.

consolidation helps reduce the total inductors down to just 4, thereby reducing the area of the chip. Additionally, some of the inductors necessary for drain capacitance resonance are large ($>$ 10 nH) due to the small size of the transistors, as they are meant for outputting low power levels. Consolidation, due to the use of high-pass equivalent, reduces the inductance values and makes them feasible to be implemented on-chip around 5 GHz [33]. Note that the high-pass equivalent network produces a delay of $\angle 270°$, as opposed to $\angle 90°$ from the transmission lines. Therefore, input phases of each PA block are updated,

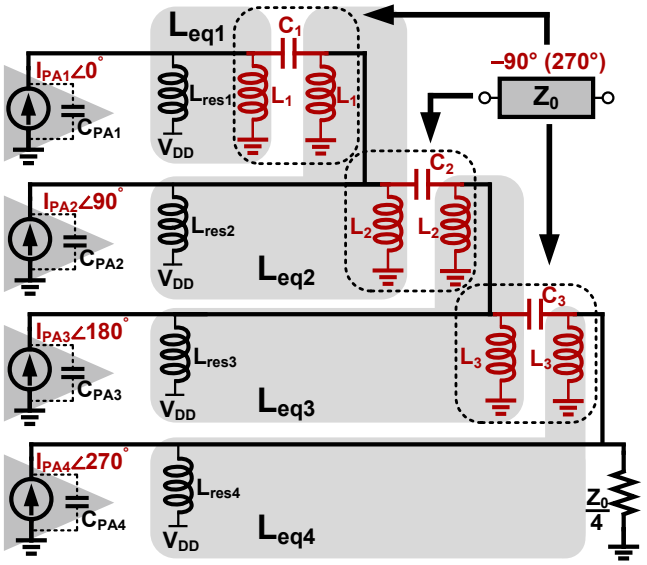

Fig. 10. Implementation of a 4-way Doherty output impedance matching network with on-chip lumped elements for transmission lines. Consolidation reduces the total number of inductors from 10 down to 4. The actual implementation is differential.

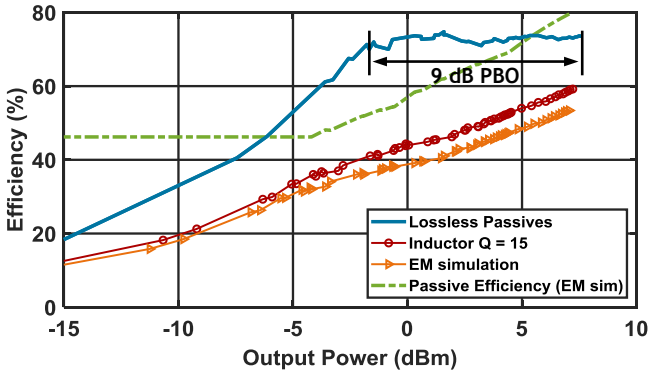

Fig. 11. Simulated drain efficiency and passive efficiency of the implemented D4DPA showing the effects of loss in passive output matching network.

as shown in Fig. 10, to maintain the impedance transformation described in Section III.

The overall performance of the PA is dependent on the implementation of the output matching network. In an ideal scenario with no loss in the passives, the PA achieves a drain efficiency around 70% throughout the whole 9 dB back-off enhancement range, as shown in Fig. 11. But on-chip inductors are lossy, and they typically obtain a quality factor of about 15 around 5 GHz. Further, they need to be connected to the digital PA blocks. These connections were implemented through transmission lines, and their effects were taken into account through an electromagnetic (EM) simulator using a method of moments (MoM) solver. The value of the inductors were then modified such that the desired inductance is presented after accounting for the transmission lines. The overall passive efficiency of the matching network and its effects on the performance are also depicted in Fig. 11. The degradation in the passive efficiency with PBO is the primary reason for the difference between the lossless and the lossy simulated drain efficiency plots. Finally, the network is also

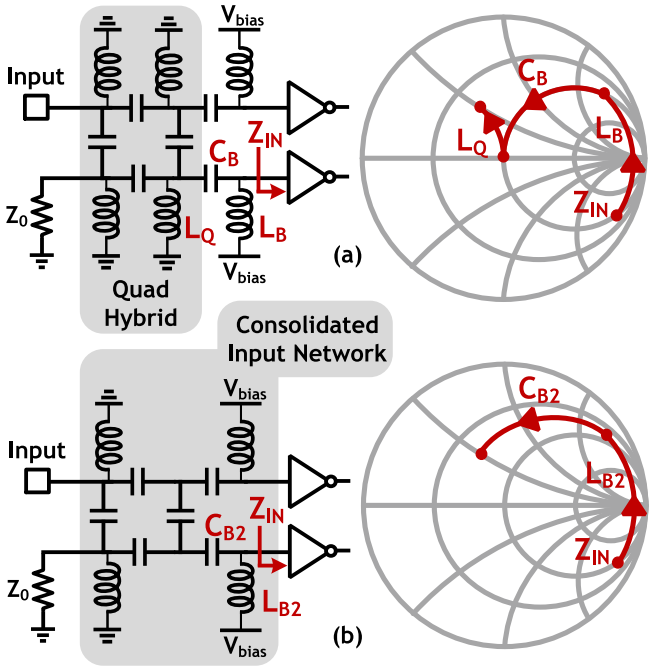

Fig. 12. (a) Implementation of a quadrature hybrid along with LC network to impedance transform and bias the RF inverters resulting in 6 inductors. (b) Consolidated quadrature hybrid and input matching network resulting in only 4 inductors. The actual implementation is differential.

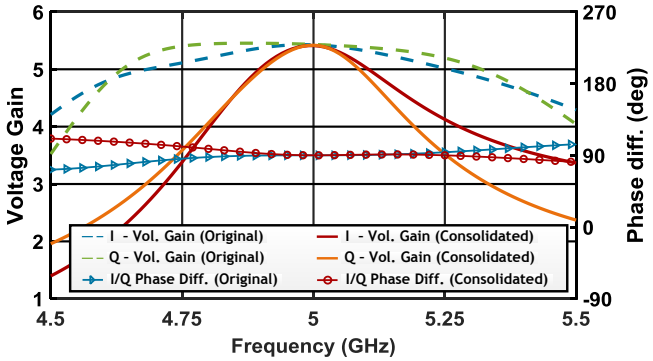

Fig. 13. Simulated frequency dependence comparison of voltage gain and quadrature phase generation for the input network before and after consolidation using ideal components.

simulated to capture the effects of inductor coupling, and it results in $< 1\%$ and < 0.15 dB change in drain efficiency and output power, respectively, for the entire back-off range.

The quadrature signals at the input of the PA are generated using a differential quadrature hybrid. This structure is followed by an LC network that serves two functions: 1) bias a set of differential inverters that drive the PA blocks, and 2) impedance transform the input of the inverters and provide 50 Ω to the output of the quadrature hybrid. This LC network can be combined with the quadrature hybrid to not only reduce the total number of inductors from 6 down to 4, but also retain the ability to provide dc biasing. Fig. 12(a) and (b) show the detailed description of the consolidation process, where L_B, C_B, and L_Q can be reduced to L_{B2} and C_{B2}.

Since the input network (quadrature hybrid + input buffer's matching network) is consolidated, its output now drives a large impedance presented by the gate of the inverter.

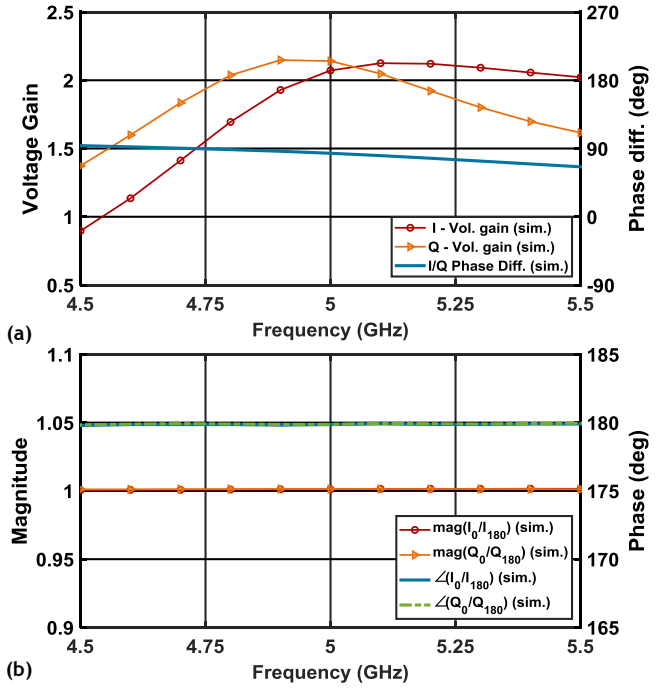

Fig. 14. EM simulated frequency dependence of the realized consolidated input network for (a) quadrature gain and phase generation, and (b) mismatch in differential magnitude and phase.

Thus, it is convenient to evaluate the performance of the consolidated input network through a voltage gain metric, rather than s-parameters. Fig. 13 shows the difference in simulated performance of the input network using lossless elements before and after consolidation. While consolidation makes the input network compact and lowers the value of the inductor L_{B2}, making it manageable to generate on-chip, it reduces the input network's bandwidth. Fig. 14 shows the simulated frequency dependence of the realized input network for voltage gain and quadrature phase generation, where the simulations were performed using an EM MoM simulator. The network achieves a peak voltage gain of 2.1 at 5 GHz and maintains a reasonable quadrature phase generation from 4.5 GHz to 5.5 GHz. This input network is connected to the pads through a long transmission line which reduces the peak voltage gain to 1.8. Although Fig. 14(a) exhibits a mismatch in the I and Q magnitude, the mismatch is reduced at the input of the PA's final stage, as the input network is followed by a set of digital buffers that act as limiters. Also, the quadrature phase deviation from the ideal 90° across frequency leads to a degradation in drain efficiency of only $< 1.5\%$ from 4.5 GHz to 5.2 GHz, and it increases to $< 4\%$ as the operating frequency increases to 5.5 GHz. Finally, Fig. 14(b) shows that the consolidated input network preserves differential magnitude and phase for the entire simulated band.

The D4DPA is composed of 4 PA blocks, and Fig. 15 shows a detailed diagram of one such block. Each PA block consists of 4-bit binary weighted unit cells with common source (CS) output stages. Every CS stage is driven by an inverter that is designed to present low impedance at its output during its operation to alleviate stability concern of the CS stage. The sizes of CS stage's LSB bits are mentioned in Fig. 15, and the

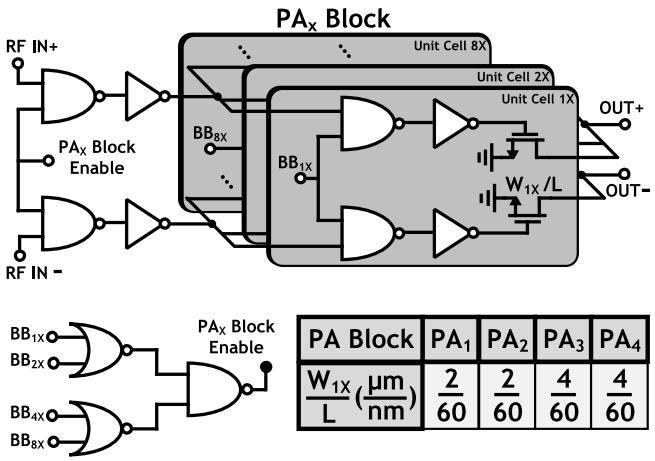

Fig. 15. Block-level schematic of each digital PA block along with the transistor sizes. The PA block can be turned off through "PA_x Block Enable" node controlled by a 4 input functional OR gate.

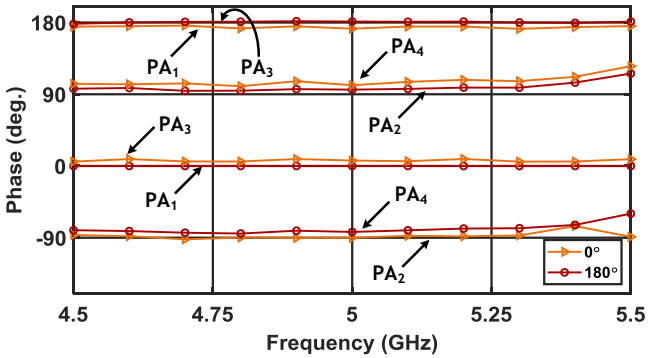

Fig. 16. Frequency dependence of differential quadrature phases at the input of the CS stage of 4 PA blocks for the MSB (x8 bit).

rest of the bits are sized proportional to their binary weights. Although the PA_3 and PA_4 blocks are sized the same, bits x1 and x2 for the PA_4 block are turned off when the D4DPA outputs maximum power. The resulting current generated by PA_4 is within 3.5% of the desired maximum current from Fig. 9(c). As seen from the lossless passives plot of Fig. 11, the chosen transistor ratios maintain high efficiency until 9 dB PBO. The baseband digital amplitude control (BB_{xx}) for the PA is implemented through NAND gates. To reduce the dynamic power dissipation, the baseband digital bits are also sent to a functional 4 input OR gate that automatically disables the entire PA block through the "PA_x Block Enable" control node, when all the digital inputs are set low.

Since the input network is followed by a set of digital gates which then connect to the CS stage, all the connections between them require careful layout to minimize degradation of the quadrature phases. Therefore, for reference, the frequency dependence of the quadrature phases at the input of the MSB (x8 bit) post layout for all the PA blocks are shown in Fig. 16. The overall block diagram of the implemented D4DPA with the consolidated differential input and output networks is shown in Fig. 17. Even after consolidation, the desired value for L_{eq1} is challenging to implement on-chip at 5 GHz. Therefore, additional capacitors are added in parallel to achieve the necessary inductance, as depicted in Fig. 17.

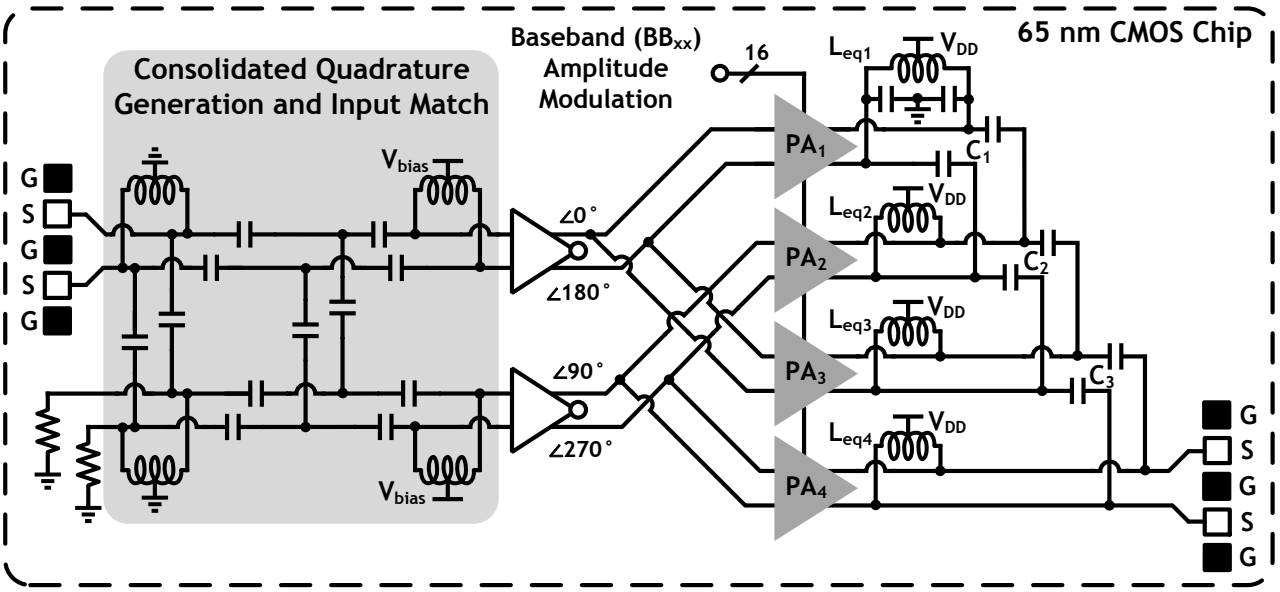

Fig. 17. Overall block diagram of the implemented differential 4-way digital Doherty power amplifier with consolidated output and input matching network and on-chip quadrature signal generation.

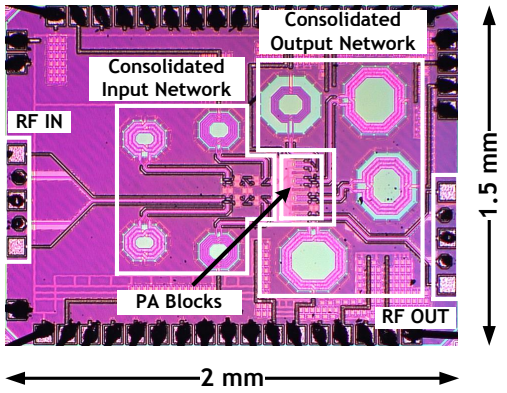

Fig. 18. Die photo of the PA realized in a 65 nm CMOS process.

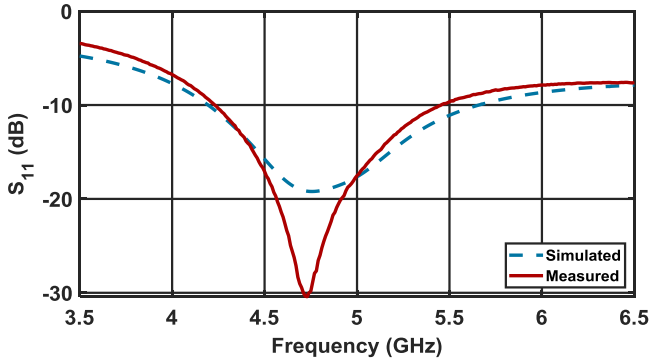

Fig. 19. Simulated and measured input reflection coefficient (S_{11}) of the PA.

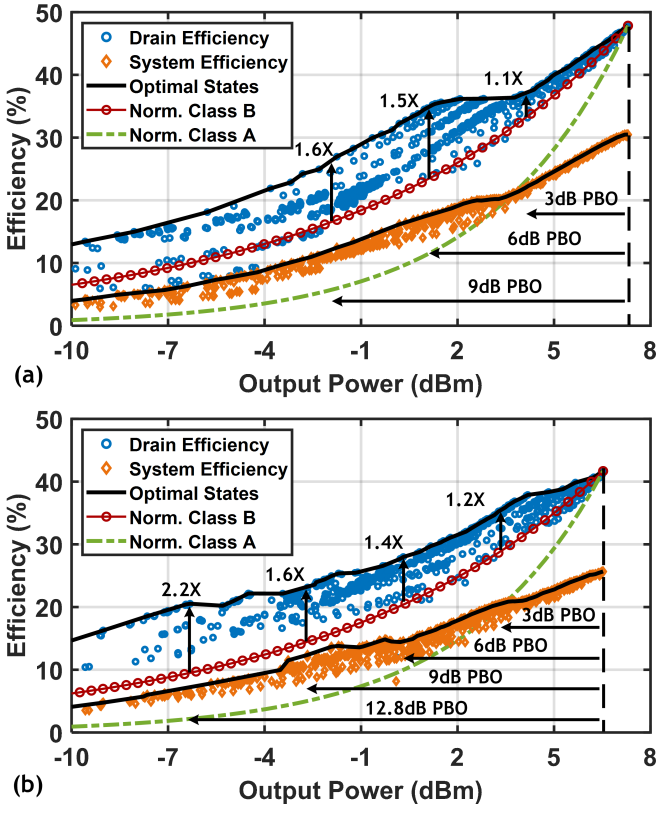

Fig. 20. Measured drain efficiency (DE) and system efficiency (SE) of the implemented PA at (a) 4.75 GHz and (b) 5.25 GHz compared to normalized class B and class A PAs.

V. Measurements

The die photo of the implemented PA is shown in Fig. 18. The simulated and measured input reflection coefficient (S_{11}) is shown in Fig. 19. The measured S_{11} is lower than -10 dB from 4.25 GHz to 5.45 GHz.

A. CW Measurements

The output CS stage is biased with a V_{DD} of 0.55 V to deliver low output power levels efficiently. A constant envelope differential signal is generated through an external balun and provided to the input of the chip. The 16 digital bits of the

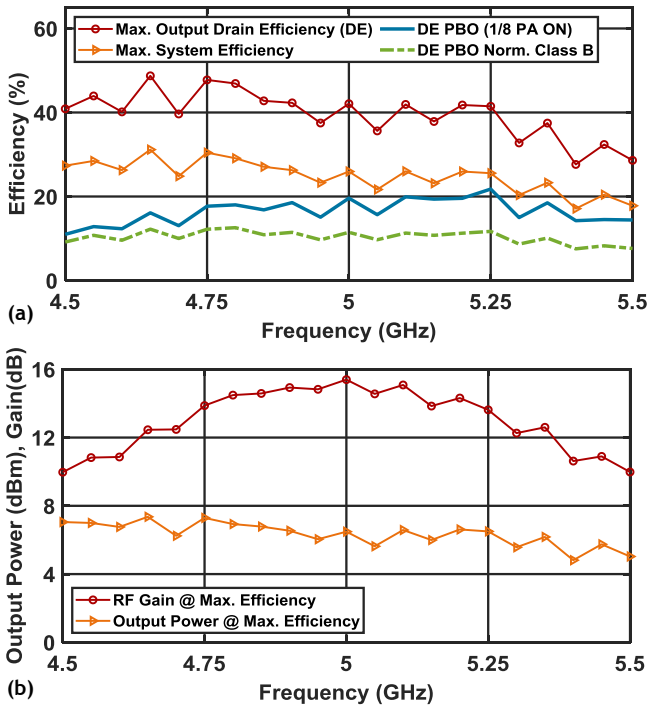

Fig. 21. Measured frequency dependence of the implemented PA for (a) DE, SE, (b) gain, and output power (P_{out}) at peak DE, where the input power is varied to maximize efficiency while still maintaining gain above 10 dB. DE performance is also shown when the PA is 1/8 turned on, and it is compared with normalized class B.

PA are controlled through an external pattern generator to vary the output amplitude levels. Fig. 20(a) and (b) show the drain efficiency and the system efficiency of the PA in power back-off at 4.75 GHz and 5.25 GHz and compare them to normalized class A and class B curves. Each of the circular and diamond points on the plot is a measured data point, and the optimal points that lead to maximum efficiency are highlighted as well. These optimal points were found through measurement and then set through a look-up table. Here, the system efficiency accounts for the power dissipated in the output stage as well as all the buffers. At 4.75 GHz, the PA achieves a peak drain efficiency of 48% with a peak output power of 7.3 dBm. The PA also obtains a DE of 37%, 35%, and 27% at 3 dB, 6 dB, and 9 dB PBO respectively, which corresponds to a 1.1×, 1.5× and 1.6× improvement compared to normalized class B. Similarly, at 5.25 GHz, the PA achieves a DE of 42% with P_{out} of 6.5 dBm. The PA also obtains a DE of 36%, 28%, 23%, and 20% at 3 dB, 6 dB, 9 dB, and 12.8 dB PBO respectively, which corresponds to a 1.2×, 1.4×, 1.6×, and a peak 2.2× improvement over normalized class B.

The maximum system efficiency at 4.75 GHz and 5.25 GHz is 31% and 26%, which implies that the buffers consume 35% and 38% of the total power dissipated, respectively. This emphasizes the need for a nested architecture, as explained in Fig. 5 under section II.

Fig. 21(a) and (b) show the frequency dependence of the PA for DE, SE, gain, and P_{out} at the maximum DE setting. The PA maintains the DE and SE above 35% and 20%, respectively, over the frequency range of 4.5 GHz to 5.25 GHz. Fig. 21(a) also shows the the frequency dependence of DE in back-off. It

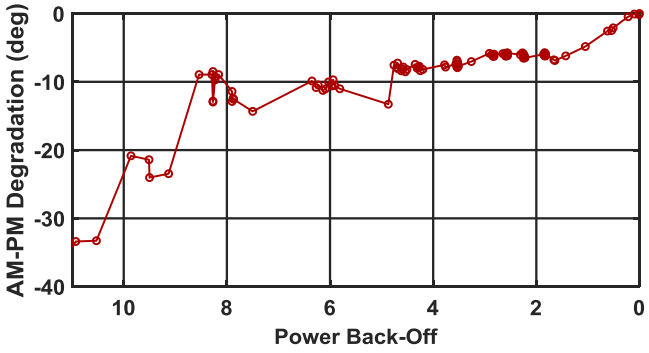

Fig. 22. Measured AM-PM degradation of the implemented PA at 5.25 GHz for the optimal drain efficiency points.

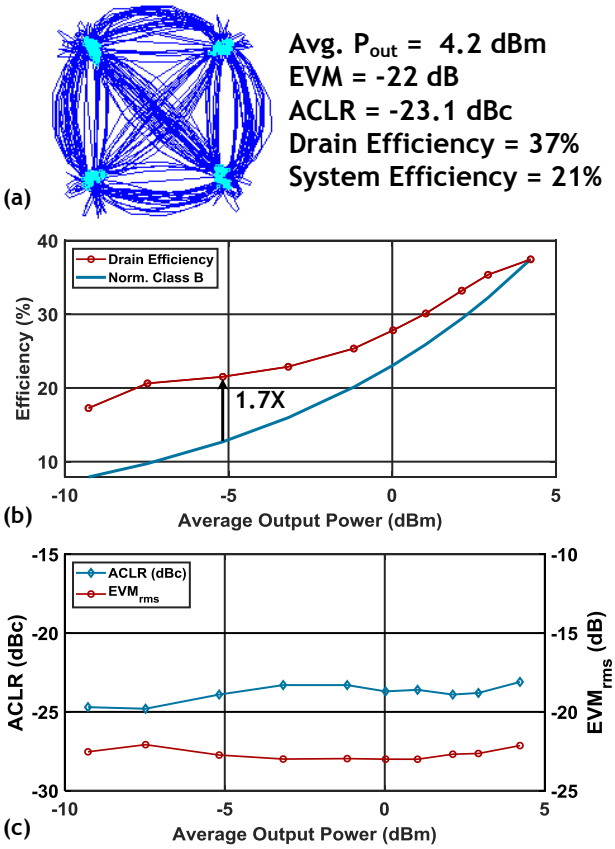

Fig. 23. For a 1 MSym/s QPSK waveform at 5.25 GHz, measured (a) constellation, (b) DE in PBO compared to normalized class B waveform, and (c) r.m.s. error vector magnitude (EVM_{rms}), and adjacent channel leakage ratio (ACLR) in PBO.

is measured for the setting that gives the maximum efficiency enhancement (PA is 1/8 turned on), and it is compared with the efficiency of the normalized class B PA for reference. The use of narrow band matching networks restricts the operating frequency, especially in PBO, to a small range. The optimum frequency of operation for the implemented PA to achieve efficiency enhancement in PBO is at 5.25 GHz. This explains the difference in the measured performance in PBO at 4.75 GHz and 5.25 GHz seen in Fig. 20(a) and (b). However, the PA still performs appreciably better than class B in PBO around 5.25 GHz as shown in Fig. 21(a). Additionally, the PA achieves a maximum gain of 15 dB at 5 GHz with a P_{out}

TABLE I
COMPARISON TO CMOS PAS WITH PBO EFFICIENCY ENHANCEMENT

	[20]		[21]	[34]	[35]	[26]	[16]	[15]	This Work	
V_{DD} Switching	Yes		Yes	No	No	No	No	No	**No**	
High-Power/ Low-Power	HP		HP	HP	HP	HP	HP	LP	**LP**	
Architecture	Class G Curr. Doherty		Class G Vlt. Doherty	Outphasing	MGTR Doherty	4-way SCPA Doherty	Doherty	2-way Doherty[#]	**4-way Doherty**	
CMOS Node	65 nm		45 nm SOI	40 nm	55 nm	40 nm	65 nm	28 nm	**65 nm**	
Die Size (mm^2)	3.2		n/a	2.5	6	0.8	2.1	0.525[@]	**3**	
Frequency (GHz)	3.71	4.3	3.5	5.9	5.8	1.5	3.82	2.15	**4.75**	**5.25**
$P_{out,max}$ (dBm)	26.7	26.1	25.3	22.2	27.2	21.4	27.3	-2*	**7.3**	**6.5**
Gain at $P_{out,max}$ (dB)	16	n/a	n/a	n/a	15*	n/a	16.8	n/a	**14**	**14**
CW Efficiency										
Peak DE | SE (%)	40.2 | n/a	36.2 | n/a	30.4[†]	49.2 | 34.9	24.5[†]	31.3[†]	30.2 | 27.5*	34* | 23*	**48 | 31**	**42 | 26**
3 dB PBO DE | SE (%)	34* | n/a	34* | n/a	26*,[†]	36* | 25*	21*,[†]	28*,[†]	28* | n/a	29* | 16*	**37 | 22**	**36 | 21**
6 dB PBO DE | SE (%)	37 | n/a	29.3 | n/a	25.3[†]	25* | 19*	13*,[†]	27.7[†]	22* | n/a	24* | 11*	**35 | 18**	**28 | 15**
9 dB PBO DE | SE (%)	32* | n/a	27* | n/a	19*,[†]	18* | 13*	8*,[†]	21*,[†]	16* | n/a	18* | 7*	**27 | 12**	**23 | 12**
RF Modulation										
Modulation	1 MSym/s 16 QAM		10 MHz 256 QAM	20 MHz 64 QAM	40 MSym/s 64 QAM	20 MHz 64 QAM	0.5 MSym/s 16 QAM	50 Mbps 16 QAM	**1 MSym/s 16 QAM**	
Average P_{out} (dBm)	20.8	20.1	17.1	16.4	20.6	15.2	21.8	-7.66	**3.1**	**1.9**
Modulated DE (%)	28.8	27.2	21.4[†]	23.3	9.4[†]	25.3[†]	22.1	n/a	**35**	**34**
ACLR (dBc)	-21[$]	-26.5[$]	<-45[††]	n/a	-33.2	-30.4[‡]	-21.8	-30.1	**-21.7**	**-21.4**
EVM (dB)	-24[$]	-30[$]	-40.1[††]	-30**	-32.8	-32.5[‡]	-25	-24.7	**-22.5**	**-20.5**

[#] Integrated in a transmitter
[$] After AM-PM Linearization
[@] Active area only
[††] AM-AM/-PM LUT
*Estimated from reported Fig.
**After DPD
[†] PAE
[‡] Look-Up Table

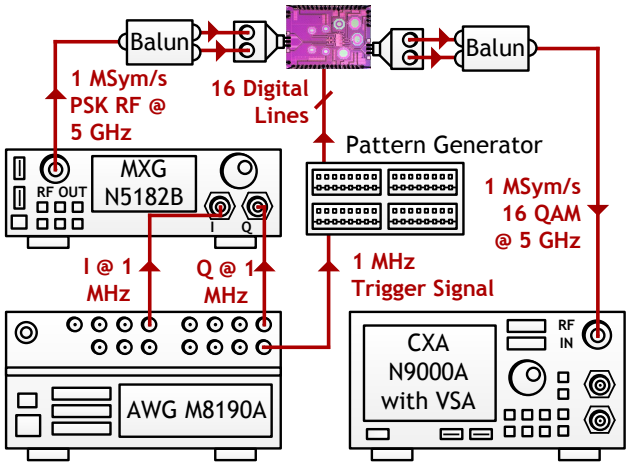

Fig. 24. Measurement setup for outputting a 16 QAM RF signal through the implemented PA.

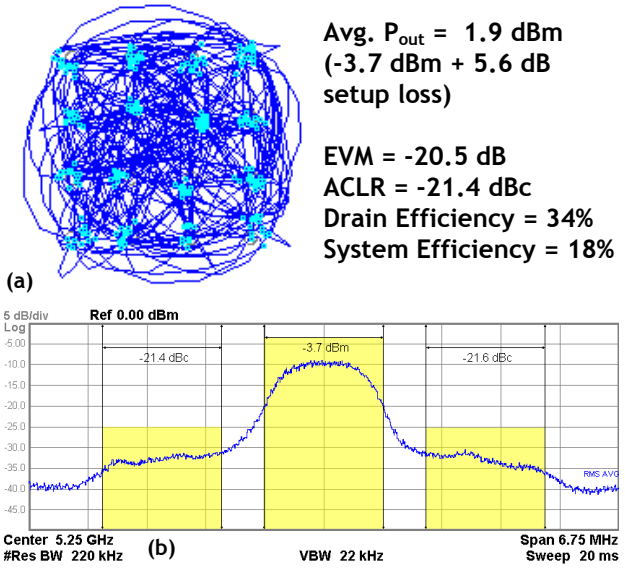

Fig. 25. Measured (a) constellation, EVM_{rms}, and (b) ACLR for a 1 MSym/s 16 QAM waveform at 5.25 GHz.

of 6.5 dBm. Since the performance of the input network of the PA is frequency dependent, as shown in Fig. 14, the input power provided to the PA is varied with frequency to maximize efficiency, while still maintaining gain above 10 dB. Therefore, even though the gain lowers, the output power stays relatively constant, within $\pm$ 1 dB from 4.75 to 5.35 GHz, as depicted in Fig. 21(b).

The digitally switched on and off unit cells of a current mode PA changes the output capacitance that it presents to the load. This results in an amplitude to phase non-linearity that is captured in an AM-PM measurement, and it degrades as the PA is pushed in PBO. The static AM-PM measurement at 5.25 GHz is depicted in Fig. 22. The code words that corresponded to the optimal drain efficiency points were used for this measurement, and it shows a maximum degradation of 33° up to 11 dB PBO. This is the primary reason that the modulation capability of the implemented PA is limited to 16 QAM. To perform higher-order modulation schemes, an AM-PM linearization would be needed (not implemented in this work.)

B. RF Modulated Measurements

To perform QPSK and 16 QAM measurements, a phase shift keyed (PSK) RF signal is generated through a vector signal

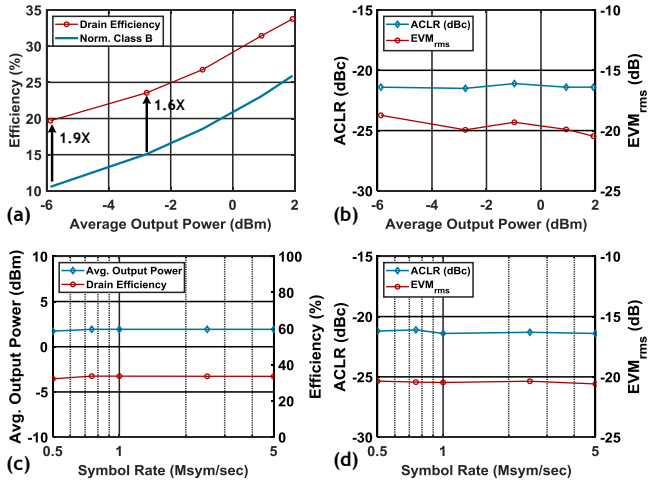

Fig. 26. For a 1 MSym/s 16 QAM waveform at 5.25 GHz, measured (a) DE in PBO compared to normalized class B waveform, and (b) EVM_{rms} and ACLR in PBO. (c) P_{out}, DE, (d) ACLR, and EVM_{rms} are measured for robustness with respect to symbol rate.

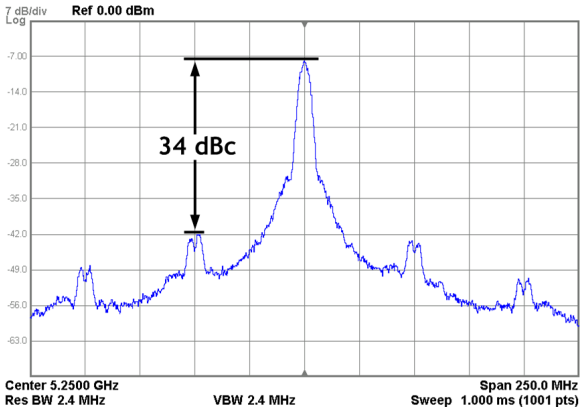

Fig. 27. Far-out spectrum for a 5 MSym/s 10× oversampled 16 QAM waveform at 5.25 GHz.

generator (VSG) and provided to the RF input of the PA. The PSK data is oversampled at 10× for all the measurements.

The QPSK measurement results for a 1 MSym/s waveform at 5.25 GHz are shown in Fig. 23. The PA achieves an average P_{out} of 4.2 dBm with a DE of 37% and SE of 21%. It also achieves an r.m.s. error vector magnitude (EVM_{rms}) of -22 dB and adjacent channel leakage ratio (ACLR) of -23.1 dBc. Further, the digital controls of the PA are used to vary the power levels in back-off. The PA obtains a DE improvement of 1.7× at 9.4 dB PBO and it maintains its EVM and ACLR below -22 dB and -23 dBc, respectively, over the entire measured back-off range.

The measurement setup for 16 QAM is shown in Fig. 24. An M8190A arbitrary waveform generator (AWG) is used to generate baseband I/Q signals with a desired symbol rate which is then provided to an N5182B VSG to get up-converted to RF. The AWG also generates a trigger signal at the symbol rate that is used to synchronize the up-converted PSK signal with the digital control bits, so the amplitude and the phase change occur simultaneously.

For a 1 MSym/s 16 QAM measurement at 5.25 GHz, the PA achieves an average P_{out} of 1.9 dBm with a DE of 34% and SE of 18%. It also achieves an EVM_{rms} of -20.5 dB and ACLR of -21.4 dBc. The biggest limitation to reduce EVM_{rms} is the AM-PM non-linearity that causes the inner constellation points to rotate with respect to the outer points, as illustrated in Fig. 25. This degradation gets worse in PBO for the code words that correspond to optimal drain efficiency, as shown in Fig. 22. Since no AM-PM linearization or digital pre-distortion (DPD) is applied in this work, the look-up table of code words is used to trade-off some optimal drain efficiency points for the ones that exhibit improved AM-PM to lower P_{out}, while maintaining EVM_{rms} close to -20 dB, as depicted in Fig. 26(a) and (b). Further, the PA is also tested at maximum output power with symbol rates from 0.5 MSym/s to 5 MSym/s for robustness, and no major changes in DE, P_{out}, EVM_{rms}, and ACLR are observed, as shown in Fig. 26 (c) and (d). Since the targeted application for the implemented PA is low-power ad-hoc sensor network nodes, the layout of the digital lines and the baseband circuitry were designed to be able to demonstrate a modulation capability of 1 MSym/s, and they limit the modulation performance of the PA at higher bandwidths.

Fig. 27 depicts the far-out spectrum of the PA for a 5 MSym/s 16 QAM measurement at 5.25 GHz. Since the RF input of the PA is driven with a 10× oversample rate, sampling images occur 50 MHz apart. These images are below -34 dBc.

VI. Conclusion

This work demonstrates a differential digital 4-way Doherty PA that achieves efficiency enhancement up to 9 dB PBO. The PA has been implemented in a 65 nm CMOS process and achieves a P_{out} of 7.3 dBm at 4.75 GHz with peak DE and SE of 48% and 31%, respectively. Table I compares the results of this work to other efficiency enhancement state-of-the-art low-power (LP) PAs ($P_{out,max} < 10$ dBm), high-power (HP) PAs with operating frequency higher than 3.5 GHz, and 4-way Doherty PAs. The implemented PA achieves competitive peak DE and SE, while performing better than all non-V_{DD} switching PAs in DE PBO. To the best of the authors' knowledge, this is the first paper that demonstrates a PA with efficiency enhancement in deep PBO (> 6 dB) for sub 10 dBm output power applications.

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