A 366 nW, -74.5 dBm Sensitivity Antenna-Coupled Wakeup Receiver at 4.9 GHz with Integrated Voltage Regulation and References

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***Abstract*— This paper describes a highly-integrated, supply-robust, event-driven wakeup receiver achieving <-74 dBm sensitivity using a custom antenna at 4.9 GHz or <-68 dBm sensitivity when matched to a 50 Ω source at 5.3 GHz, both across a supply voltage range from 1.2 V to 1.5 V while consuming 244 nA dc current in 65 nm CMOS technology. Voltage regulators, voltage and current references are all integrated on-chip operating from the same single battery supply. A novel slot antenna is proposed to directly match to the high impedance input of the envelope detector and eliminate losses associated with the bond-wire match.**

***Keywords*— Antenna, wakeup receiver, missed detection rate, sensitivity, ultra low power**

I. Introduction

Sub μW-level wakeup receivers (WuRxs) enable event-driven Internet of Things (IoT) applications to allow for always-alert operation even as the rest of the node sleeps to conserve power. As these IoT nodes are remotely placed and mass deployed, their power sources can vary significantly in voltage, and much of the voltage regulation and dc reference functionality that might be implemented off-chip in higher power systems must be integrated on-die with the WuRx, requiring it to be independently tolerant to supply voltage variation and produce all needed voltage and current references from that unreliable supply. It must also simultaneously maintain low current consumption to maximize efficiency, while maximizing sensitivity to enable longer ranges from the transmitter. One area where sensitivity is lost in many low power WuRxs is in matching from a 50 Ω input to the high impedance on-chip environment conducive to ultra-low power detection [1], [2], [3].

This work presents a supply-robust WuRx with <-74dBm sensitivity when connected to a custom antenna at 4.9GHz and <-68 dBm sensitivity when matched to a 50 Ω source at 5.3GHz across supply voltage (1.2 V to 1.5 V) with 244 nA current. This is achieved by 1) integrating voltage regulators, current and voltage references on chip that are robust to variation in battery voltage, 2) designing a directly matched high impedance antenna with an inductive impedance component that conjugate matches to the the RF input of the chip, 3) maintaining a dc coupled baseband path that allows for asymmetric Code Division Multiple Access (CDMA) codes with large cross-correlation to reduce the rate of false wakeups, 4) including an ultra low power integrated crystal oscillator driver that provides a stable baseband clock, 5) an ultra low power strong-arm latch comparator with digital capacitive digital-to-analog converter (CAPDAC) threshold tuning, and 6) a 63 bit digital correlator with programmable error tolerance to increase the total code space. While prior work in multi-GHz, sub μW WuRxs have shown that achieving sensitivities beyond -65 dBm is possible [1], [2], including some with a codesigned antenna [4], [5], they have required external bias voltages and were demonstrated only at a single precise supply voltage.

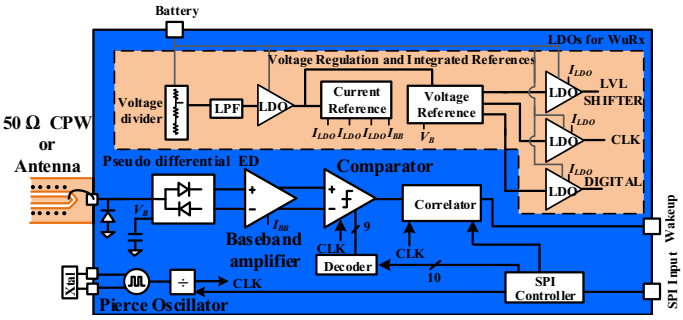

Fig. 1. Block diagram of the proposed wakeup receiver.

II. WuRx Architecture

A. Receiver

The proposed receiver is shown in Fig. 1. Robustness to supply variation is achieved through the use of fully integrated, current references (Fig. 2(a)), voltage references (Fig. 2(b)) and low drop-out (LDO) voltage regulators to derive the supply and biases for the receiver. The first LDO connected to the supply generates a fixed bias voltage which is used to generate the voltage and current biases for the rest of the system, and has a simulated quiescent current of 5 nA. A sub-threshold, leakage current-based voltage reference exploiting the difference in threshold voltages between low voltage threshold (LVT) and native device types is used to generate a temperature compensated reference with improved line sensitivity and power supply rejection ratio (PSRR) [6]. Simulation results show a 70% reduction to supply variation. The nano-watt current reference uses a complementary to absolute temperature (CTAT) voltage generated from a stack of diode-connected transistors to produce a temperature compensated current source with improved line sensitivity [7]. This current is used as a reference to generate all the currents in the WuRx as shown in Figure 2(a).

Two matching and packaging solutions are presented in this paper. The first is a bond-wire match to 50 Ω at 5.3 GHz. The second is a custom designed, directly matched

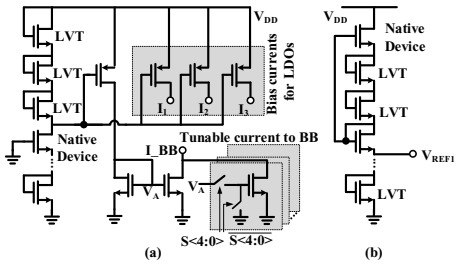

Fig. 2. Schematic of (a) current reference and (b) voltage reference.

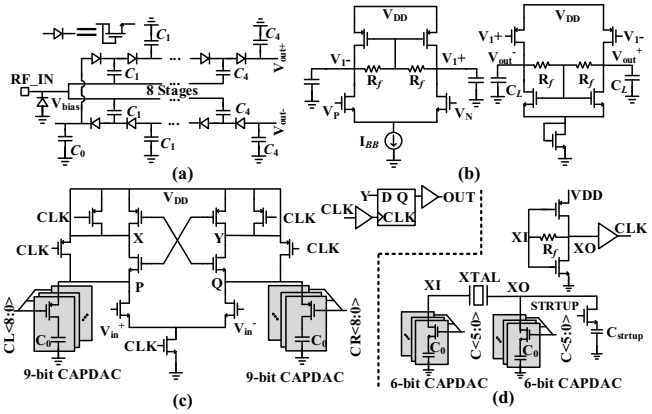

Fig. 3. Schematic of (a) envelope detector, (b) baseband amplifier, (c) comparator and (d) Pierce oscillator.

antenna at 4.9 GHz that will be discussed in more detail below. The input impedance of the envelope detector (ED) and bondwire inductance are used to provide the match at 5.3 GHz. The wakeup signal is a 63 bit on-off-keyed (OOK) signal with a bit rate of 64 Hz. The differential output of the 8-stage pseudo-differential Dickson envelope detector helps to minimize the effect of the kickback noise at the comparator input. The 2-stage baseband amplifier gain can be tuned through digital control by actuating the current through the first stage of the baseband amplifier (Fig. 3(c)). The baseband amplifier is dc-coupled to the comparator and has a simulated gain of 49.6 dB.

The strong-arm latch comparator (Fig. 3(c)) utilizes 9-bit CAPDACs for threshold control (-130 mV to 130 mV), and samples at 4x the bitrate to avoid requiring synchronization with the transmitter. Due to the dc-coupling with the baseband, long sequences of ones and zeros can be transmitted without being filtered, enabling asymmetric, large cross-correlation within the code. The comparator threshold is set manually through the digital SPI interface to achieve the desired false positive rate from the comparator of approximately 2%, a tradeoff between the false wakeup rate and the sensitivity of the receiver with and without interferers.

A 63-bit, 4x oversampling correlator bank is used with programmable error threshold compares the reference code with the comparator output and issues a wakeup if the error tolerance is met. The system clock is based on a Pierce oscillator as shown in Fig. 3(d). The crystal has a Q>10000 at its resonant frequency at 32.768 kHz and the clock frequency is stable across the supply voltage range. The crystal oscillator is

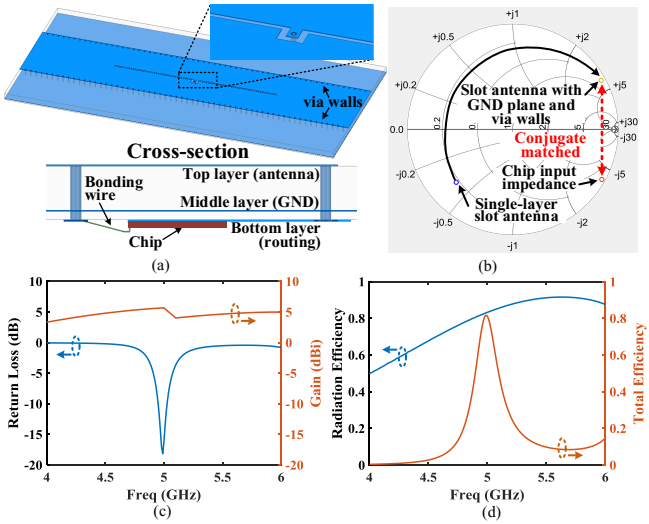

Fig. 4. (a) Structure of the proposed slot antenna, (b) impedance matching between the antenna and the WuRx chip, (c) simulated return loss and gain, and (d) efficiency of the antenna.

divided by a programmable counter to derive the 64 Hz clock matched to the bit rate of the receiver.

B. Antenna

To maximize power transfer from free-space electromagnetic radiation into the RF input of the receiver, a novel slot antenna with designable output impedance and high efficiency is proposed and shown in Fig. 4(a). The slot antenna is fabricated on a three layer printed circuit board (PCB) as shown in the cross-section view. In the top layer, a symmetric slot is fabricated with an excitation port in the center. In the middle layer, a metal ground layer is placed under the slot antenna, connecting to the top layer through via walls on both sides of the slot. These vias provide a parallel inductance on the antenna, modifying its impedance from being slightly capacitive into something that is inductive, with high resistance, as seen in Fig. 4(b). The impedance of the antenna can be designed by changing the size of the slot and the distance of the vias from the slot to achieve impedance matching between the chip and the antenna. This enables a direct conjugate match with the capacitive input of the WuRx. The receiver chip is epoxied on the bottom layer and connected to the excitation port of the slot antenna on the top layer through a via and wire bonding. The PCB is fabricated with a low-loss substrate (Rogers 4003C) with a slot antenna length of 30.6 mm.

The antenna has a simulated return loss of 16.1 dB between the antenna and the chip and a gain of 5.7 dBi at 5 GHz (Fig. 4(c)). The simulated radiation efficiency of the antenna is 83% at 5 GHz in Fig. 4(d), and the total efficiency is 81% when considering impedance mismatch with the receiver chip.

III. Measurement Results

The WuRx chip was fabricated in 65 nm CMOS process occupying an area of 4.0 mm^2. Fig. 5 shows the die photo, photos of the 50 Ω and antenna PCBs and the antenna test setup. The setup for the wireless measurement is shown in

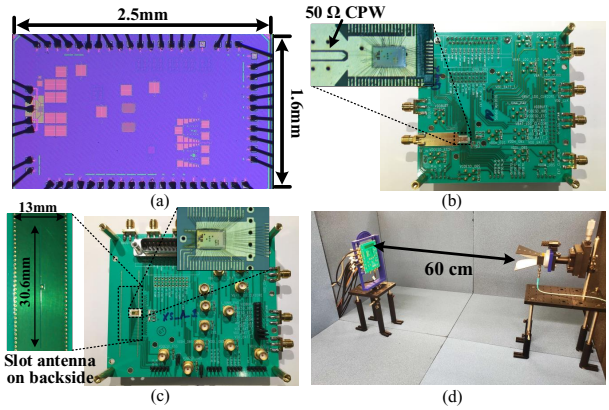

Fig. 5. The photos of (a) chip die, (b) PCB of WuRx with 50 Ω CPW, (c) PCB of WuRx with slot antenna, and (d) wireless measurement setup.

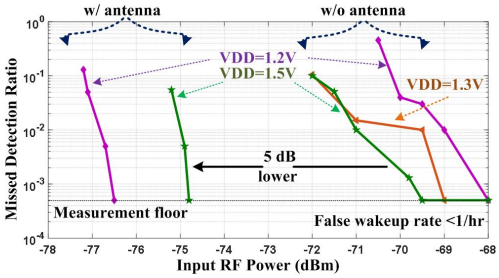

Fig. 6. Measured missed detection rate versus input RF power of the WuRx with and without antenna.

Fig. 5(d) with the transmitting horn antenna placed 60 cm away from the WuRx board.

When matched to a 50 Ω input, the WuRx achieves a sensitivity of <-68 dbm at 10^{-3} missed detection rates and false wakeup rate of <1 wakeup/hr across supply variation from 1.2 V to 1.5 V, with a maximum sensitivity of -69.5 dBm at 1.5 V (Fig. 6). The wakeup code is a 63-bit asymmetric Kasami code 4x over-sampled with a bit rate of 16 bps. The wakeup receiver has a total dc current draw of 187 nA at 1.2 V and 244 nA at 1.5 V supply with individual block consumption shown in Figure 7. The on-chip clock draws a current of 77 nA for a 1.5 V supply and has <1 mHz variation in frequency and a standard deviation of <3 mHz across power supply.

The comparator offset is manually tuned for ≈2% false positive rates and is fixed for a given power supply. A Bit Error Ratio (BER) of 10^{-3} is observed at the output of the comparator for -69.5 dBm sensitivity at 1.5 V supply. BER measurement at the output of the comparator is used to test the interferer rejection. The Signal to Interference Ratio (SIR) is observed with the RF input signal 3 dB above the sensitivity with 10^{-3} BER. In-band continuous wave (CW) at 3 MHz and 12 MHz offsets, and out-of-band interferers at 10 Mbaud 16QAM at 750 MHz, 2.4 GHz and 5.8 GHz are used to test the interference robustness of the wakeup receiver. The receiver achieves 7.6 dBc CW in-band SIR at 3 MHz offset. The relative interference power across frequency band is shown in Fig. 8.

When packaged with the antenna, the frequency response of the antenna, ED and baseband amplifier chain is shown in

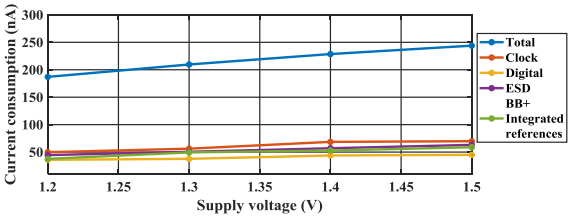

Fig. 7. Block level and total dc current consumption across supply voltage.

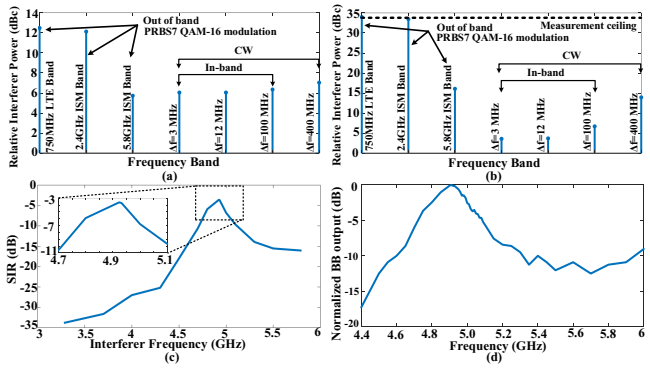

Fig. 8. Measured WuRx robustness to interference at BER=10^{-3} (a) with 50Ω match, (b) with antenna, (c) SIR versus frequency with antenna, and (d) baseband amplifier output versus frequency for antenna. Measurement ceiling due to signal generator maximum output power.

Fig. 8(d). The antenna is matched at 4.92 GHz with a 3-dB bandwidth of 270 MHz. The antenna shows a good suppression for adjacent bands especially for the crowded band below 4.6 GHz. The sensitivity for this setup is defined as the power an isotropic antenna would collect for the minimum free-space power flux that can be detected by the WuRx [4]. Sensitivities of -74.5 dBm and -76.5 dBm observed with supply voltages of 1.5 V and 1.2 V respectively, as shown in Fig. 6. For in-band CW interferers, the SIR is 3.6 dBc at 3 MHz offset and is >15 dBc for out-of-band interferers. Robustness to other interference sources is shown in Fig. 8. The work is compared with other multi-GHz, sub-μW WuRx with better than -60 dBm sensitivity in Table I.

Table 1. Comparison with multi-GHz sub-μW WuRx

	This Work		**[4]**		**[2]**	**[5]**
Input Match	50Ω	Ant.	50Ω	Ant.	50Ω	Ant.
V_{DD} Range (V)	Single 1.2-1.5		Single 0.4		2x 0.5/1	3x .1/.5/.8
V_{DD} Tol. (%)	22		0		0	0
Integrated Supply Regulation	LDOs, V&I Refs.		N/A		N/A	N/A
Sensitivity (dBm)	-68	-74.5	-64	-69.5	-68	-61.5
Freq (GHz)	5.3	4.9	9		2.2	2.4
Power (nW)	366		7.3	22.3	28.2	365
Data Rate (bps)	16		33.3		250	2500
FOM (dB)*	110.1	116.4	116.7	122.2	125.5	112.9
Clock Arch.	Xtal		Relax.		Ring	Relax.
Technology (nm)	65		65 & 180		65	65
Die Area (mm^2)	4.0		14 & 450		3.9	1.875

*FOM= $-P_{sensitivity,dB}$ + 5log(R_b)-10log(P_{dc}/1mW)

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