A low noise current readout architecture with 160 dB transimpedance gain and 1.3 MHz bandwidth

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ABSTRACT

This paper proposes a low-noise readout circuit with a noise floor of 11 $fA_{rms}/sq(Hz)$ and a bandwidth of 1.3 MHz. The novel electrostatic discharge (ESD) leakage current cancellation stage allows the circuit to detect sub-pA range current input. A total trans-impedance gain of 160 dB is obtained by a current preamplification stage with a 100 × current gain followed by a transimpedance amplifier (TIA) with a 1 Mohm feedback resistive gain. The reader is designed in a 0.18 μm CMOS process and consumes 5.6 mW from a 1.8 V supply.

1. Introduction

There is a growing trend to sense very low levels of current in many diagnostic applications such as biosensing [1–3]. Current levels in nanoamperes (nA) or even picoamperes (pA) are harder to detect using CMOS circuitry due to electronic circuit noise. Several sense amplifier circuits have been developed for low current sensing. For example, integrator or transimpedance amplifier (TIA) are employed to convert the current signal into a voltage signal, followed by quantization of the converted voltage signal. However, with the current in the pA range, if the integration method is adopted, it would take a long time to accumulate the small current into a measurable voltage signal [4]. If a TIA is employed, the feedback resistance must be large enough (i.e.gigaohms range) to obtain high gain, and there is a trade-off between achieving high dynamic range and achieving low input-referred current noise. Moreover, such a large feedback resistor must be externally connected. Otherwise relying on the high value active pseudo resistor used in the feedback loop [5–9], it is very hard to set or control, since its resistance is inversely proportional to the input current, it will lead to a variable current gain and bandwidth [10].

In most applications such as in nanopore sequencing, the small current signals need to be amplified at high speed with bandwidths in excess of 1 MHz. Current conveyor is commonly employed for current amplification; however, the conventional current conveyor is not suitable for the small current amplification since the bias current of the conveyor leads to large input referred current noise [11,12]. No-bias current conveyor was previously reported for low-noise current sensing [13]. However the noise levels achieved may still be prohibitive for low current sensing. A wide input dynamic range current readout was presented featuring a matched double-MOS architecture around an amplifier to obtain current amplification [14]. However, capacitors with the same current ratio are needed to increase the bandwidth. In this paper, a current preamplifier with a flat gain is proposed to obtain bidirectional current amplification. Electrostatic discharge (ESD) diodes offer protection by providing current path for unwanted electrostatic discharge events. However, they are rather large in area and can carry significant leakage currents under normal operating conditions. As the input current signal scales down to the pA range, the leakage current (up to 10 nA) from the ESD diodes may dominate the input current. Even worse, the leakage current is not constant that can increase with the temperature. None of the circuits discussed in literature address the leakage current issue from the input ESD diode. In fact most designs avoid the use of ESD altogether for input nodes considerably compromising yield. In this article, we propose an approach to compensate the leakage current from the input ESD diode using a dummy ESD diode with active biasing. The architecture is implemented in 0.18 μm CMOS process to achieve a total gain of 160 dB in trans-impedance and noise level of around 11 $fA_{rms}/sq(Hz)$.

2. Low-noise current readout architecture

2.1. Current amplification

The current preamplifier consists of a PMOS and an NMOS transistors M_{P1} and M_{N1} that are connected in the feedback loop of the amplifier as in Fig. 1. The drain nodes of M_{P1} and M_{N1} are connected to *Gnd*

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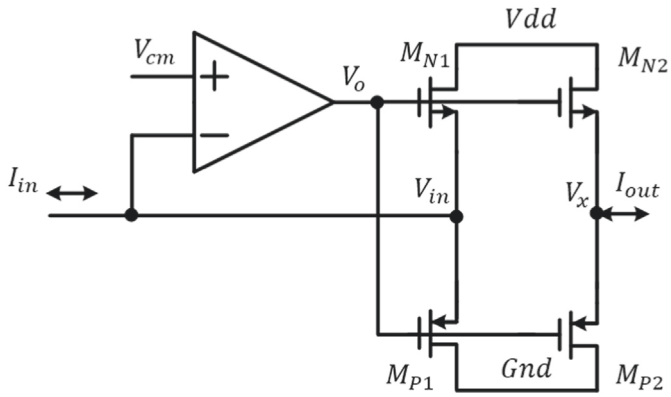

Fig. 1. Current preamplifier.

and *Vdd*, respectively. The source nodes of M_{P1} and M_{N1} are connected as the input node V_{in}, which has a common mode potential of V_{cm}. The amplifier regulates its output voltage V_o according to the input current I_{in} through the negative feedback loop to bias the transistors M_{P1} and M_{N1}. The output voltage V_o of the amplifier also couples the gates of the transistors M_{P2} and M_{N2}. The source nodes of M_{P2} and M_{N2} are shorted at node V_x as the output of the current amplifier. For reading the output current I_{out}, the node V_x connects to a following stage, which is a TIA or an integrator. It keeps V_x at the same voltage potential as node V_{in}. Therefore transistor $M_{N(P)1}$ and $M_{N(P)2}$ have the same V_{gs} and V_{ds},which ensures that transistor $M_{N(P)2}$ will carry the same current as $M_{N(P)1}$. This architecture is known as an "inverted current mirror". When the input current flows into the node V_{in}, the feedback amplifier adjusts the output voltage V_o such that the V_{gs} of $M_{N(P)1}$ is negative, allowing the input current to flow into transistor M_{P1}. Transistor M_{N1}, M_{N2}, M_{P1}, and M_{P2} share the same V_{gs}.Thus M_{N1} and M_{N2} are off, and M_{P2} "effectively copies" the input current, which can be amplified by sizing aspect ration of M_{P2} with respect to M_{P1}. Similarly, if the input current flows out of the node V_{in}, M_{P1} and M_{P2} are off, and M_{N2} "effectively copies" the input current and amplifies by sizing aspect ration of M_{N2} with respect to M_{N1}. This allows for bidirectional current amplification.

Note that at the input node V_{in}, the input impedance is $1/Ag_{m_{N1}}$ or $1/Ag_{m_{P1}}$. The high DC gain of the amplifier reduces the input impedance at node V_{in}. At the output node V_x, the output impedance is $1/g_{m_{N2}}$ or $1/g_{m_{P2}}$. For the small current signal, $g_{m_{N2}}$ and $g_{m_{P2}}$ are very small such that the output impedance at node V_x is still large. The inverted current source M_{N2} or M_{P2} is still a good current source with high output impedance. The node V_x couples to a virtual ground with a very low impedance provided by the following TIA or integrator. Therefore, the current from the M_{N2} and M_{P2} can easily be acquired and measured by the subsequent stage.

Transistors operate in the subthreshold region and are therefore sensitive to the drain source V_{ds} differences given that V_{ds} is less $3V_{th}$ [15]. The large V_{ds} bias of $M_{N1(2)}$ and $M_{P1(2)}$ makes them insensitive to the V_{ds} variation, which has a better matching than the current conveyor with low V_{ds} bias. In addition, the bi-directional current amplification is built with only 4 transistors. Compared with the current amplifier architecture using 20 transistors [13], this architecture has much lower input-referred current noise contribution.

2.2. ESD leakage current cancellation

It is essential in all silicon realizations to include ESD protection. Typical ESD circuits consists of large diodes. However, such ESD diodes contribute their own leakage current, which can sometimes dwarf the small levels of input current signal. This is among the most significant remaining challenge in low current readout circuits for practical applications. To understand our proposed compensation scheme, we elucidate briefly the functioning of these ESD diodes. The diode has a well-defined relationship between bias voltage and the diode current as in Fig. 2(a). The ESD input diode composes of two diodes connected in series between the power rails. For this application, the input node is at half *Vdd*, and they are both reverse biased. In Fig. 2(b), I_{N1} is the reverse current from N-diode DN_1, I_{P1} is the reverse current from P-diode DP_1. The difference between current I_{N1} and I_{P1} is the uncompensated diode leakage current I_{l1} that sneaks in or out of the readout circuit, as shown in Equation (1). The P-diode and N-diode have different leakage current behaviors with the process, voltage, and temperature (PVT) variations, leading to a variable leakage current. It fundamentally limits the sensitivity of the current sense amplifier circuitry.

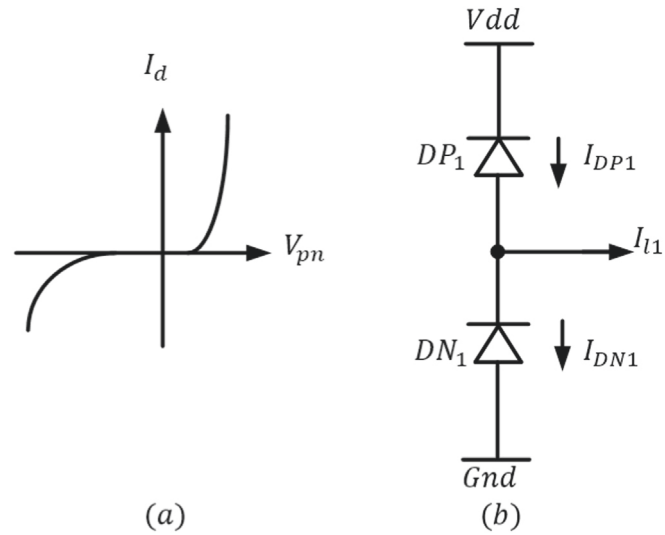

Fig. 2. Source of leakage current in ESD diodes.

$$I_{l1} = I_{DN1} - I_{DP1} \tag{1}$$

This paper proposes a novel leakage current compensation approach as in Fig. 3. It includes the addition of dummy ESD diodes (P-diode D_3 and N-diode D_4) to cancel the leakage current from the original ESD diodes (P-diode D_1 and N-diode D_2). The leakage currents I_{l1} is from the original ESD diodes DN_1 and DP_1. The sum current $I_{in} + I_{l1}$ flows into transistor M_{P1}, and transistor M_{P2} mirrors the current with a 1:1 ratio. M_{N1} and M_{N2} are off. Respectively, the dummy P-diode DP_2 and N-diode DN_2 generate the leakage current I_{N2} and I_{P2}, respectively, leading to a net leakage current of I_{l2} as in (2). Current $I_{in} + I_{l1}$ flows out of node V_x to transistor M_{P2}, while current $I_{in} + I_{l2}$ and I_x flow into node V_x. I_x is the current flows from M_{N3}, which is mirrored to M_{N4} with a ratio of 100. Transistor M_{P3} and M_{P4} are off. Based on Kirchhoff's Current Law (KCL), the current I_x is shown in (3).

$$I_{l2} = I_{DN2} - I_{DP2} \tag{2}$$

$$I_x = I_{in} + I_{l1} - I_{l2} = I_{in} + (I_{DN1} - I_{DN2}) + (I_{DP1} - I_{DP2}) \tag{3}$$

Note that the leakage current from P-diodes I_{DP1} and I_{DP2}, and the leakage current from N-diodes I_{DN1} and I_{DN2} can track with each other under different PVT variation. Equation (3) brings a second-order leakage current cancellation, which would have a smaller net leakage current than that from Equation (1).

To verify the leakage current cancellation, Fig. 4 compares the leakage currents of the current readout circuit without and with the ESD leakage current compensation circuit in Fig. 3. From Monte Carlo simulation, the net leakage current from the reader with leakage compensation circuit is much less than that without leakage compensation circuit as in Table 1.

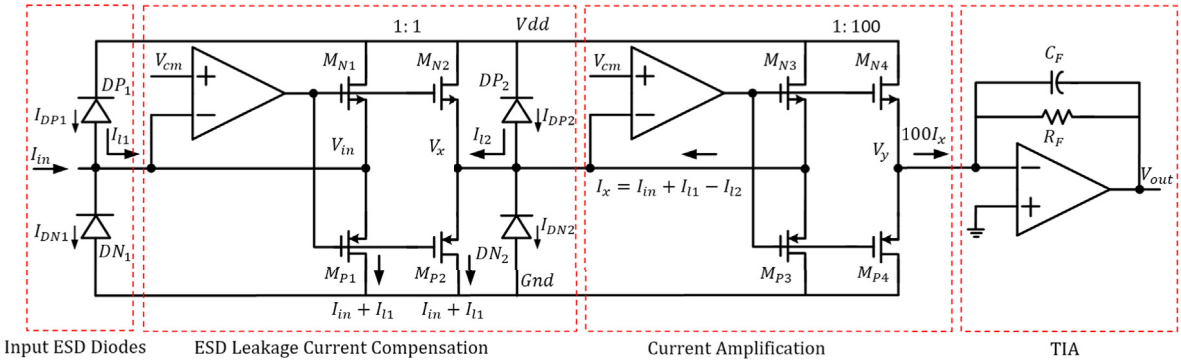

Fig. 3. Proposed leakage current compensated readout circuit.

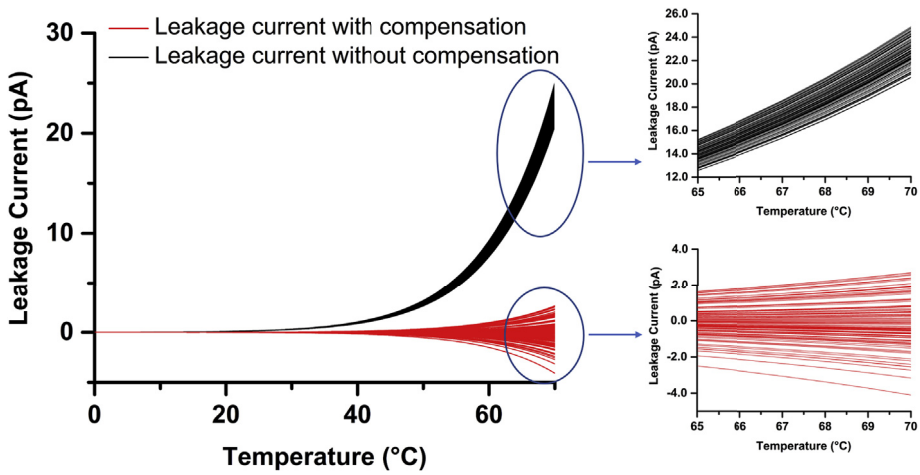

Fig. 4. Monte Carlo Simulation of leakage current of the uncompensated and compensated circuit.

Table 1
Monte Carlo Simulation results (100 times).

Temperature	w/o compensation: average value (standard deviation)	w compensation: average value (standard deviation)
10 °C	26 fA (2 fA)	0.1 fA (2.7 fA)
40 °C	960 fA (46 fA)	1.1 fA (58 fA)
70 °C	23 pA (1 pA)	5 fA (1.4 pA)

2.3. Operational amplifier (OP-amp) design

The op-amp used in the feedback loop composes of a pre-amplification stage and a two-stage miller compensation amplifier in Fig. 5.

2.4. Loop stability analysis

The small current in the source follower of M_{N1} or M_{P1} results in a low-frequency pole P_1 at node V_{in} and the source follower of M_{N1} or

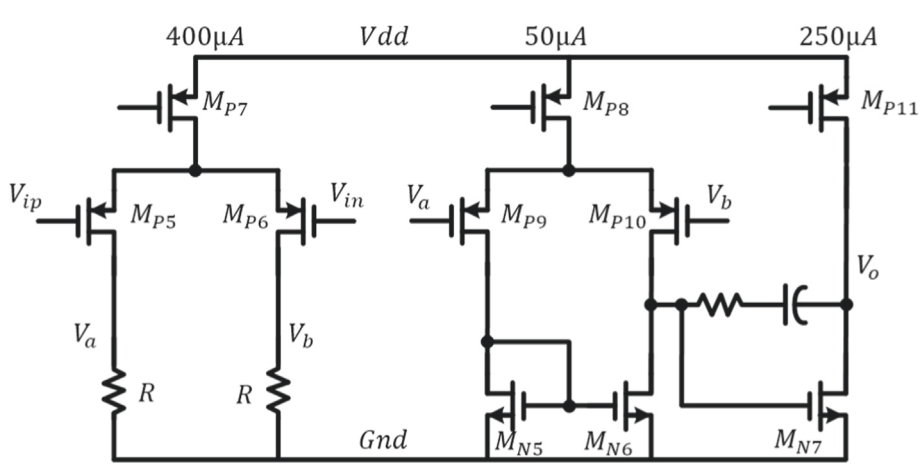

Fig. 5. Low-noise amplifier.

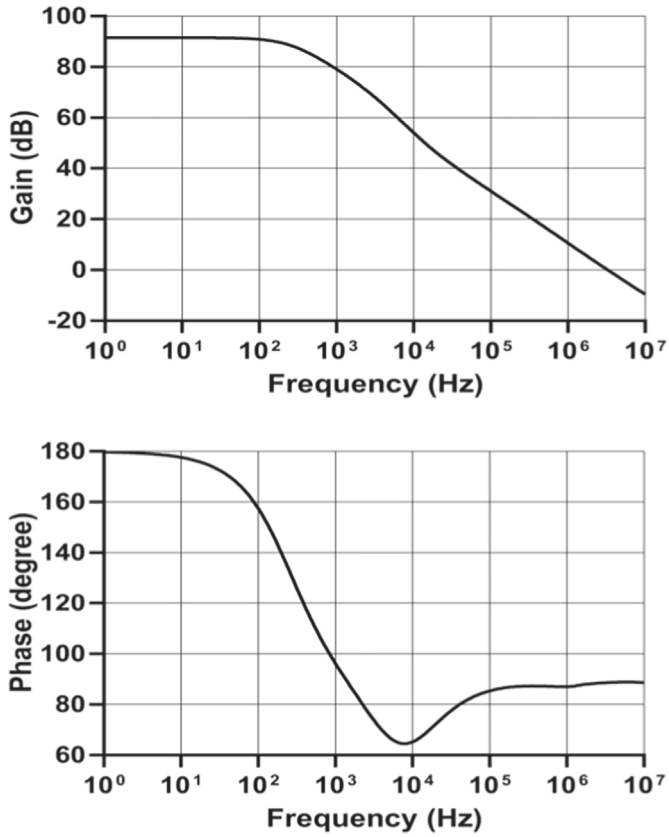

Fig. 6. Frequency response of the loop.

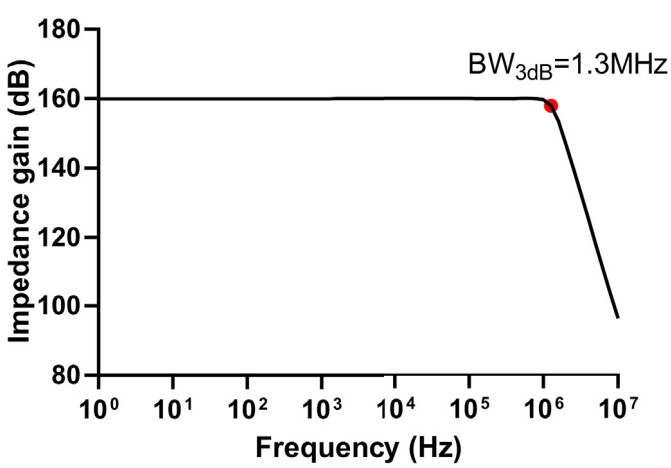

Fig. 7. 3 dB bandwidth is 1.3 MHz.

M_{P1} also brings a low-frequency zero Z_1 to compensate the pole P_1. If Z_1 and P_1 are within the unity-gain bandwidth, the loop could still be stable. The frequency response of the current mirror loop with the op-amp is shown in Fig. 6. The unity-gain bandwidth is 1.6 MHz, and the phase margin is 88°.

2.5. Gain of the TIA

A 1 M ohm Poly resistor serving as the feedback resistor is used. Since the preamplification current gain is 100, then the total impedance gain is 160 dB. Fig. 7 shows the 3 dB bandwidth impedance gain is 1.3 MHz.

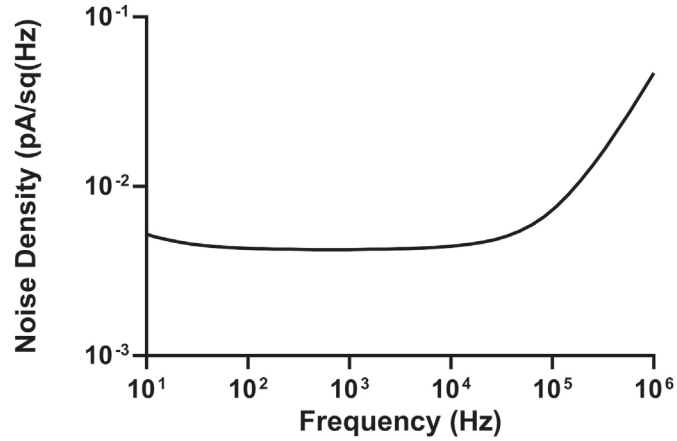

Fig. 8. Input referred current noise density.

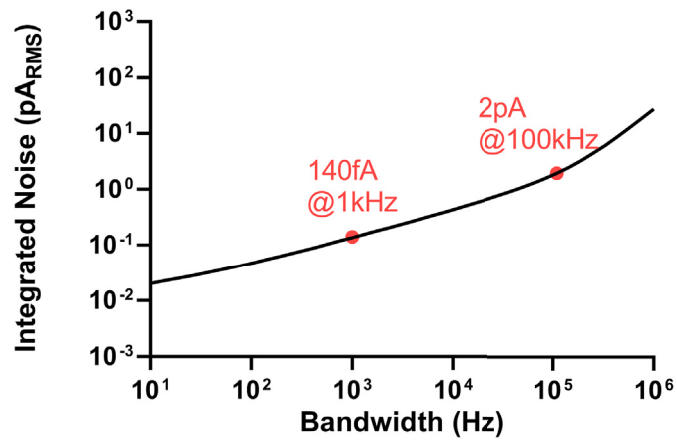

Fig. 9. Input referred integrated noise level.

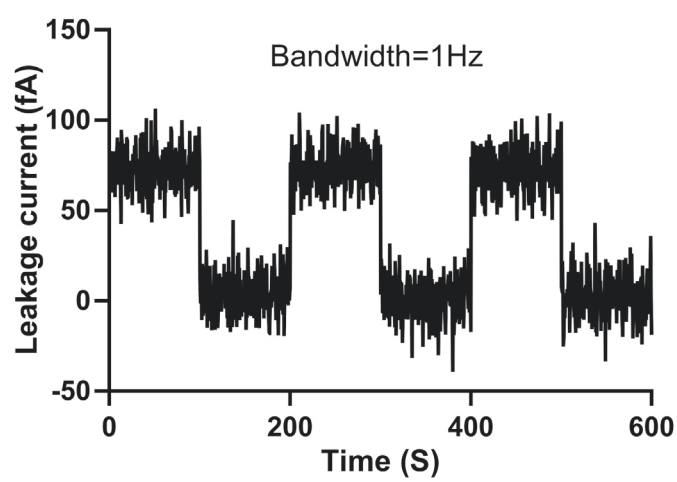

Fig. 10. Recovered 70 fA 0.005Hz current signal.

2.6. Noise contribution analysis

The input referred current noise at the input is given by:

$$i_{eq}^2 = qI_{in} + (2\pi f C_{in})^2 (e_n)^2 \tag{4}$$

$$e_n^2 = \frac{16kT}{3gm_{M_{P5}}} + \frac{8kT}{(gm_{M_{P5}})^2 R} + \frac{2K}{WLC_{ox}f} \tag{5}$$

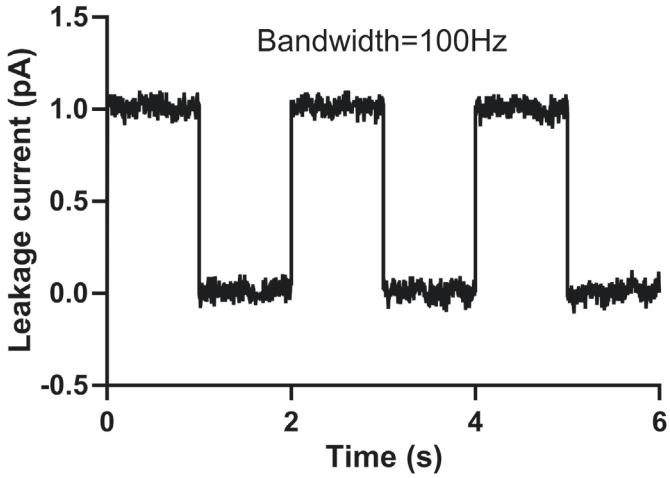

Fig. 11. Recovered 1 pA 2Hz current signal.

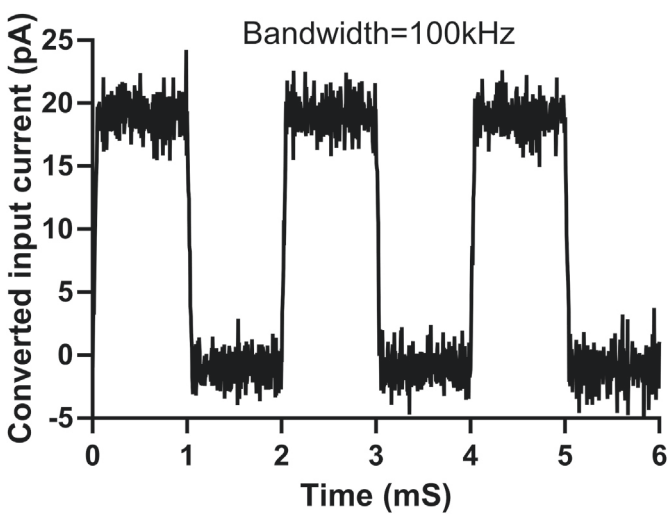

Fig. 12. Recovered 20 pA 500Hz current signal.

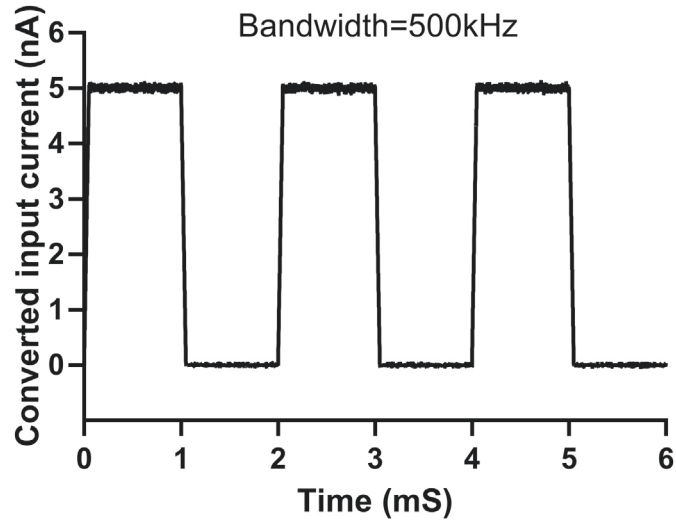

Fig. 13. Recovered 5 nA 500Hz current signal.

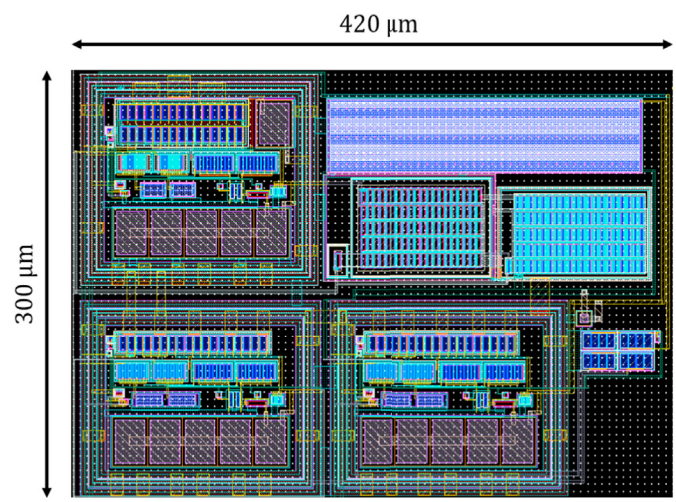

Fig. 14. The layout of the current reader in 0.18 μm CMOS process.

The equivalent input current noise is shown in Equation (4). qI_{in} is the shot noise from $M_{P(N)1}$ operating in the subthreshold region. The voltage noise e_n^2 from the op-amp of the ESD leakage current compensation stage over the input capacitance C_{in} sets the minimal noise of the circuit when the input current I_{in} is small. In Equation (5), the pre-amplification stage has the dominant noise contribution. k is Boltzmann constant, and K is a process related constant which influences the flicker noise. The input-referred current noise density was simulated as shown in Fig. 8, and its integrated noise density is shown in Fig. 9. The integrated noises are 140 fA at 1 KHz and 2 pA at 100 KHz, respectively.

3. Quantization

A square wave of input current signal 70 fA 0.005 Hz, 1 pA 2 Hz, 20 pA 500 Hz, and 5 nA 500 Hz square wave inputs are injected at the input node, in a simulated test bench. Figs. 10–13 present the recovered current signals for 70 fA 0.005 Hz, 1 pA 2 Hz, 20 pA 500 Hz, and 5 nA 500 Hz square wave inputs, with the quantized bandwidth of 1 Hz, 100 Hz, 100 kHz, and 500 kHz, respectively. Fig. 14 shows the layout of the current reader.

Table 2 lists the literature summarizes the proposed readout circuit

Table 2
Table of comparison with relevant architecture.

	[4]	[5]	[16]	[17]	[18]	This work[a]
Technology (μm)	0.18	0.35	0.09/0.5	0.35	0.18	0.18
Power supply (V)	1.8	3	2.5/1	3.3	3.3	1.8
Noise floor ($fA_{rms}/sq(Hz)$)	11.6	4	0.235	6	5	11
Signal bandwidth (MHz)	1.4	4	0.005	0.05	0.0039	1.3
Dynamic range (dB)	155.1	95.9	68.5	74.5	74	100
Area (mm^2)	0.091	0.34	0.065	0.14	0.5	0.126
Power consumption (mW)	9.4	13.5	0.4	76	23	5.6

[a] Simulation Results at 27 °C.

performance and compares it with other recent state-of-the-art demonstrations.

4. Conclusion

This paper presents a low-noise current readout circuit for biomedical current sensing applications. The readout circuit consists of an ESD leakage current cancellation circuit, a bidirectional current amplification stage, and a TIA stage. The leakage current cancellation approach allows the sensor to have high sensitivity even in the presence of leakage current from the ESD diodes making this circuit quite practical in real application. The use of multiple stages enables very high transimpedance gain, and very low input-referred noise. This design also operates at high speeds (MHz), making this an attractive design for readout from most biosensors and nanopore sequencing platforms.

Author statement

Wei Wang: Conceptualization, Methodology, Validation, Original draft preparation, Validation, Data curation, Writing- Original draft preparation, Resources. Wenxin Zeng: Writing - Review & Editing, Resources. Sameer Sonkusale: Conceptualization, Supervision, Writing-Reviewing and Editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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References

[1] Jacob K. Rosenstein, Meni Wanunu, Christopher A. Merchant, Marija Drndic, Kenneth L. Shepard, Integrated nanopore sensing platform with sub-microsecond temporal resolution, Nat. Methods 9 (2012) 487–492.

[2] Adrian Balan, Bartholomeus Machielse, David Niedzwiecki, Jianxun Lin, Peijie Ong, Rebecca Engelke, Kenneth L. Shepard, Marija Drndić, Improving signal-to-noise performance for DNA translocation in solid-state nanopores at MHz bandwidths, Nano Lett. 14 (12) (2014).

[3] Marco Crescentini, Marco Bennati, Marco Carminati, Marco Tartagni, Noise limits of CMOS current interfaces for biosensors: a review, IEEE Transactions on Biomedical Circuits and Systems 8 (2) (2014) 278–292.

[4] Shanshan Dai, Rukshan T. Perera, Zi Yang, Jacob K. Rosensteing, A 155-dB dynamic range current measurement front end for electrochemical biosensing, IEEE Transactions on Biomedical Circuits and Systems 10 (5) (2016) 935–944.

[5] Giorgio Ferrari, Fabio Gozzini, Alessandro Molari, Marco Sampietro, Transimpedance amplifier for high sensitivity current measurements on nanodevice, IEEE J. Solid State Circ. 44 (5) (2009), pp. 1609-161.

[6] Jacob K. Rosensteina, Meni Wanunu, Christopher A. Merchant, Marija Drndic, Kenneth L. Shepard, Integrated nanopore sensing platform with sub-microsecond temporal resolution, Nat. Methods 9 (5) (2012) 487–492.

[7] Mark M.R. Ibrahim, Peter M. Levine, CMOS transimpedance amplifier for biosensor signal acquisition, in: IEEE International Symposium on Circuits and Systems, 2014.

[8] Sungkil Hwang, Michael Trakimas, Sameer Sonkusale, A low-power asynchronous ECG acquisition system in CMOS technology, in: 32nd Annual International Conference of the IEEE EMBS, 2010.

[9] Sungkil Hwang, Kofi Aninakwa, Sameer Sonkusale, Bandwidth tunable amplifier for recording biopotential signals, in: 32nd Annual International Conference of the IEEE EMBS, 2010.

[10] Mark M.R. Ibrahim, Peter M. Levine, A 170-dB CMOS TIA with 52-pA input-referred noise and 1-MHz bandwidth for very low current, IEEE Trans. Very Large Scale Integr. Syst. 25 (5) (2017) 1756–1766.

[11] Dongsoo Kim, Brian Goldstein, Wei Tang, Fred J. Sigworth, Eugenio Culurciello, Noise analysis and performance comparison of low current measurement systems for biomedical applications, IEEE Transactions on Biomedical Circuits and Systems 99 (1) (2012) 52–62.

[12] Sungkil Hwang, Sameer Sonkusale, CMOS VLSI potentiostat for portable environmental sensing applications, IEEE Sensor. J. 10 (4) (2010) 820–821.

[13] Hamed Mazhab Jafari, Roman Genov, Chopper-stabilized bidirectional current acquisition circuits for electrochemical amperometric biosensors, IEEE Transactions on Circuits and Systems I: Regular Papers 60 (5) (2013) 1149–1157.

[14] Wei Wang, Sameer Sonkusale, An approach for a wide dynamic range low-noise current readout circuit, J. Low Power Electron. Appl. 10 (3) (2020).

[15] Luís H.C. Ferreira, Sameer R. Sonkusale, A 60-dB gain OTA operating at 0.25-V power supply in 130-nm digital CMOS process, IEEE Transactions on Circuits and Systems I: Regular Papers 61 (6) (2014) 1609–1617.

[16] Junjie Lu, Jeremy Holleman, A wideband ultra-low-current on-chip ammeter, in: IEEE Custom Integrated Circuits Conference (CICC), 2012.

[17] Brian Goldstein, Dongsoo Kim, T. Jian Xu, Kyle Vanderlick, Eugenio Culurciello, CMOS low current measurement system for biomedical applications, IEEE Transactions on Biomedical Circuits and Systems 6 (2) (2012) 111–119.

[18] Marco Bennati, Federico Thei, Michele Rossi, Marco Crescentini, Gennaro D'Avino, Andrea Baschirotto, Marco Tartagni, A sub-pA $\Delta\Sigma$ current amplifier for single molecule nanosensors, in: IEEE International Solid-State Circuits Conference (ISSCC), 2009.