A Millimeter-Scale Computing System with Adaptive Dynamic Load Power Tracking

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A computing system has been continuously miniaturized, and larger number of small IoT devices become a part of our ubiquitous lives. Recently, the size of the systems reached down to a millimeter scale, and they demonstrate new sensing approaches in ecological, biomedical, and security applications [1]–[3]. As an example, Fig. 1(a) shows a millimeter-scale layer-stacked system, constructed by vertically stacking bare die, maximizing the planar circuit area for a given volume. This platform miniaturizes a computing system down to a millimeter scale mainly by avoiding individually packaged discrete components [4]. The miniaturization results in reduced battery capacity, limiting energy available for the integrated circuits. For example, a 9.8-mm^2 thin-film lithium battery stores charge of only 15μAh, allowing the average current draw of 21nA (84nW) for system lifetime of 1 month [5]. The lithium battery provides higher voltage (e.g., 4V) than what a standard CMOS transistor can tolerate, requiring a high-efficient Power Management Unit (PMU) that converts the battery voltage to lower voltages (e.g., 1.5V). Due to size constraint, PMUs for the small systems have been designed with on-chip capacitors instead of bulky discrete inductors [4],[6].

For low average power consumption, the system employs a duty-cycled operation and turns off majority of circuits in sleep mode. The PMU must efficiently convert power while consuming 10–100s of nW in sleep mode and 10–100s of μW in active mode. [4] down-converts the battery voltage using a capacitive DC-DC converter with a ladder topology. It adjusts a conversion ratio from 1/3 to 2/5 in lower battery voltage range and sets the switching frequency to manually chosen values between sleep and active modes. For high power conversion efficiency, it requires dedicated control for dynamic digital circuit operations across temperatures and battery voltages. [6] employs a recursive capacitive DC-DC converter [7] that reconfigures conversion ratio with fine resolution and regulates the output voltage to 1.2V. It adaptively controls the switching frequency of the power converter in a feedback fashion by monitoring the output voltage. For sudden load current change from sleep to active mode, it detects voltage drop more than a threshold and maximizes the switching frequency. Smaller threshold reduces the output voltage drop but imposes a greater risk that falsely triggers the fast switching frequency from noise during sleep mode, resulting in significant energy loss. Thus, it is essential to develop a PMU that down-converts the battery voltage to a constant voltage with high power conversion efficiency across temperatures and battery voltages, without any energy loss from output voltage noise.

This paper proposes a millimeter-scale multi-layer-stacked computing system that tolerates significant load current change between low-power sleep mode and high-performance active mode. It reliably supplies power to load circuits in different layers by rapidly boosting the output driving strength responding to an active-mode request from any layers. Also, the circuit adaptively controls switching frequency of its power converters for dynamic frequency scaling and against supply and temperature changes, by employing a replica of an oscillator for a processor. The proposed design is fabricated in a 180 nm process and integrated with other layers for a millimeter-scale system. It reliably transits to active mode with load power change of up to 6,083× and improves the system power conversion efficiency by up to 37% (3.2× improvement) compared with constant switching frequency.

Fig. 1(b) shows the conceptual operation of the proposed PMU. It converts varying battery voltage (3.6–4.2V) down to regulated 1.5 V and 0.7 V for digital logics, using recursive [7] and a 2:1 capacitive DC-DC converters. In sleep mode, it slowly adjusts the switching frequency by monitoring the output voltage [6] for low load current (10s of nA), dissipating low quiescent power for high efficiency. It switches its mode from sleep to active by being synchronized with bus communication. In the system, any layer can initiate the transition from sleep to active mode. This feedforward transition is applicable to a typical IoT system since transition to active mode is well characterized in such a system and its driving strength of PMU can be adjusted in advance. It helps avoid false transition to high switching frequency and guarantees robust operation without significant energy loss against output voltage noise. Once the mode transition request is received by PMU, it accelerates the switching frequency proportional to the clock frequency of the processor and layer controller, which dominates power consumption at the power domains of 1.5V and 0.7V in active mode. It maintains high power conversion efficiency by updating the PMU switching frequency to balance switching and conduction losses.

The drive strength of PMU is adaptively adjusted by 1) using a feedback loop in sleep mode and 2) using a canary oscillator in active mode (Fig. 2). In sleep mode, the feedback loop compares output voltage of the converter to the reference voltage (V_{REF}) and adjust switching frequency. Due to its slow response time and short active duration (<100ms), the feedback cannot be used in the active mode. Also, as sleep-mode quiescent current is set low to achieve high efficiency, fast sleep-to-active transition is difficult when there is an instant load current increase. Thus, the proposed PMU injects charge to C_{CTRL} using a switched-capacitor circuit (M_{P1}, M_{P2}, and C_{UP}), and the voltage-controlled oscillator (VCO) runs at a frequency proportional to the switching frequency of load circuits. Since the clock signal for the load circuits is generated in a different layer (P&M, Fig. 1(a)), the same oscillator design is replicated in PMU layer and always configured the same (e.g., # of delay cell, frequency division ratio). It also tracks operating frequency of the load current against battery voltage or temperature changes.

Fig. 3 depicts the detailed PMU operation when system transits between sleep and active. A layer wakes up the system by pulling down its $DATA_{OUT}$ while holding CLK_{OUT} high. The change propagates through the following layers, and PMU increases the switching frequency *f*(SW) of the power converter once its $DATA_{IN}$ becomes low. It makes the driving strength of the power converter strong and ready to power the load circuits. As receiving the wakeup message, the layers begin to consume significantly higher power (I1 + I2). The PMU output voltages (*O1* & *O2*) are maintained due to the already increased drive strength. In active-to-sleep transition, *f*(SW) becomes lower after the sleep message puts the system in sleep and reduces the load power.

The proposed PMU is fabricated in a CMOS 180nm process (Fig. 7(a) and integrated with other layers for a 4.5mm^3 temperature/light sensing system (Fig. 7(b)). Fig. 4 shows the measured PMU performance in active mode. The processor operating frequency of 383kHz–2.28MHz changes the load power from 50.1 to 409μW for combined *O1* and *O2* (Fig. 4(a)). The transition between sleep and active mode is verified at the system level. For varying load power, the proposed adaptive PMU switching frequency achieves power conversion efficiency of 54–62%, which is higher than one with constant switching frequency by up to 37% (3.2× improvement) (Fig. 4(b)). It maintains its efficiency of 54–62% across battery voltages from 3.6 to 4.2 V (Fig. 4(c)) and 60–62% across temperatures from 0 to 85 °C (Fig. 4(d)), without any dedicated adjustment for the variations. Fig. 5 shows the measured PMU performance in sleep mode. While the load power changes from 41nW to 30μW for *O1* (41nW–21μW for *O2*), the feedback loop regulates the output voltages in 5.8% (8.5%) and maintains the efficiency of 51–72% (46–61%).

Fig. 6 summarizes the performance of this work and compares it with the previous PMUs for a miniature system. This work and [6] provide adaptive switching power frequency both for active and sleep modes. Compared with [4], they do not require dedicated switching frequency control for any load changes. Compared with [6], this work transits from sleep to active mode using a robust, synchronized way, without a risk of falsely increasing switching frequency due to output noise and thus wasting energy in sleep mode. This work also verifies its PMU efficiency across *VBAT*s and temperatures.

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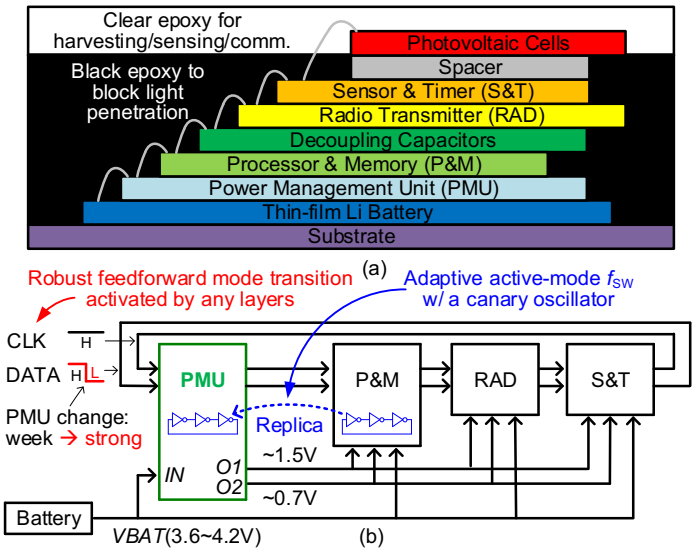

Fig. 1. Millimeter-scale computing system. (a) System diagram; (b) Proposed power management operation.

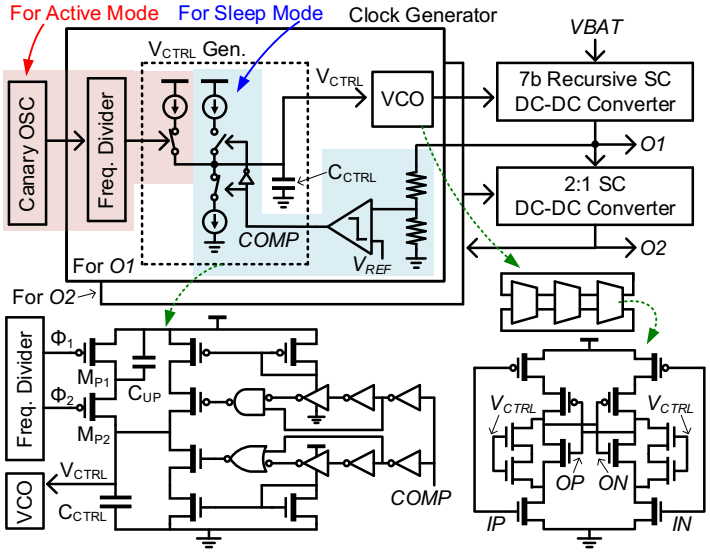

Fig. 2. Proposed adaptive PMU switching frequency with a canary oscillator for active mode and a feedback loop for sleep mode.

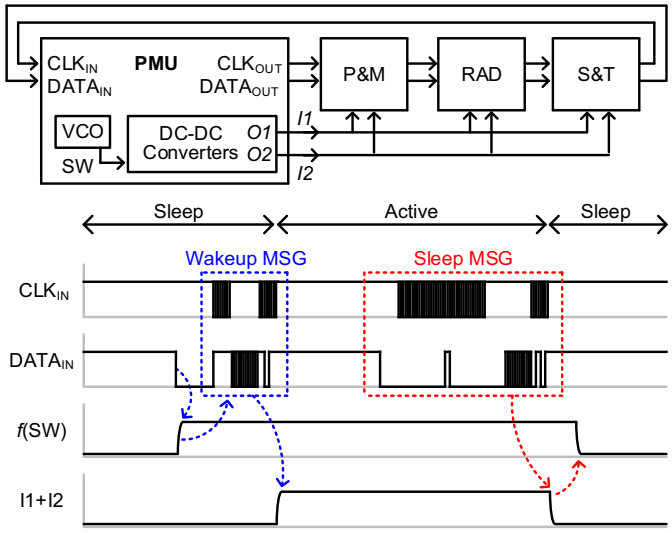

Fig. 3. Proposed transition procedure of switching frequency of DC-DC converters between system sleep and active modes.

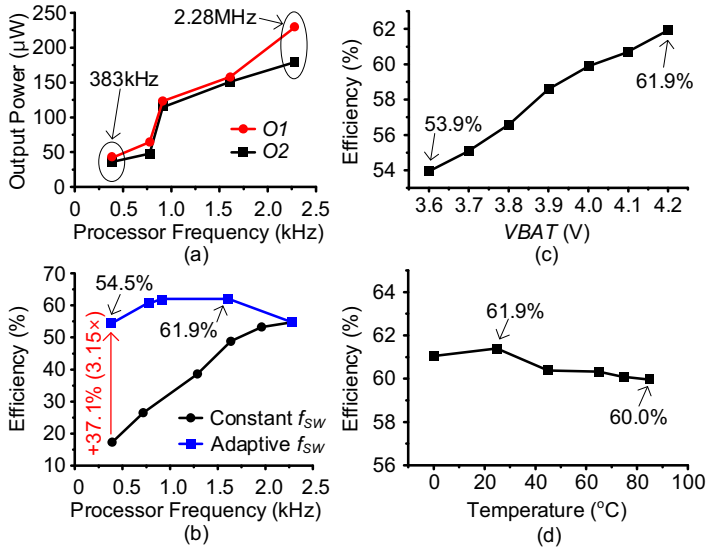

Fig. 4. Measured PMU in active mode. (a) Output power vs. freq.; (b), (c), (d) Efficiency vs. frequency, *VBAT*, and temperature.

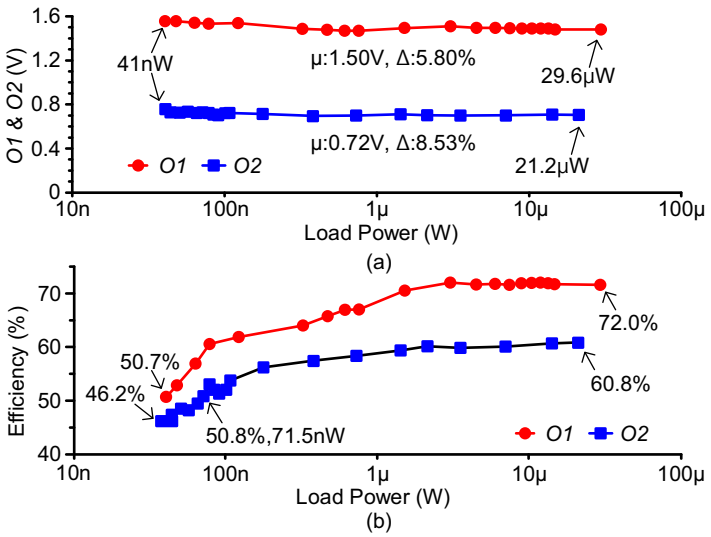

Fig. 5. Measured PMU in sleep mode. (a) Output voltages vs. load power (Combined *O1* & *O2*); (b) Efficiency vs. load power.

Parameters	This work	[4]	[6]
Process (nm)	180	180	180
Topology	7b Binary, 2:1	6:1	7b Binary, 2:1, 1:3
V_{BAT} (V)	1.5 ~ 4.2	3.6 ~ 4.2	0.9 ~ 4.2
V_{OUT} (V)	0.7, 1.5	0.6, 1.2	0.6, 1.2, 3.3
Converter Clock (Active Mode)	Adaptive w/ a canary OSC	Feedforward w/ constant OSC	Feedback w/ droop detectors
Converter Clock (Sleep Mode)	Feedback by monitoring V_{OUTS}	Feedforward w/ constant OSC	Feedback by monitoring V_{OUTS}
Robust Mode Transition w/ Output Noise	Yes	Yes	No
Efficiency vs. V_{BAT} & Temp.	54–62% (3.6-4.2V), 60-62% (0-85°C)	N/A	N/A
P_{OUT} @ Efficiency > 50%	72nW–21μW*, 79–409μW**	5–22nW*, 10–20μW**	5nW–500μW
System Integration	Yes	Yes	No

* Sleep mode, ** Active mode.

Fig. 6. Performance summary and comparison.

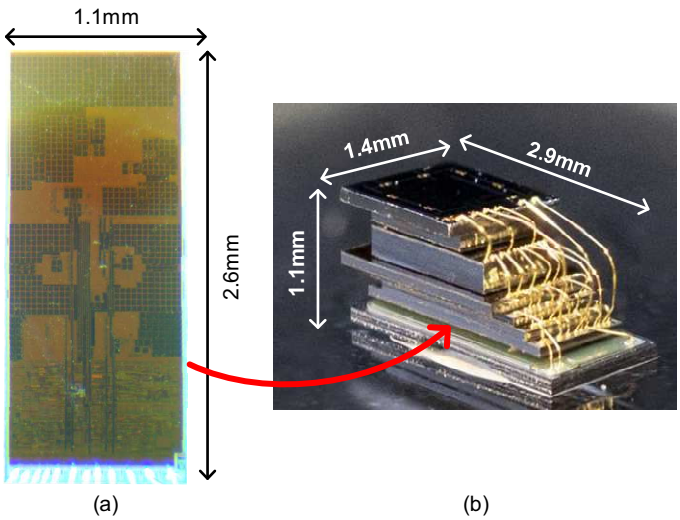

Fig. 7. Photographs of die and system: (a) PMU chip; (b) Millimeter-scale temperature/light sensing system with the proposed PMU.

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