Large-Scale Focused Helium Ion Beam Lithography

Jay C. LeFebvre and Shane A. Cybart, *Senior Member, IEEE*

***Abstract*—Focused ion beam sources have recently been commercialized and are increasingly utilized for applications in nanotechnology. There is a desire to pattern large designs, millimeter in scale, while still achieving sub-nanometer resolution in the smallest features. However, focused helium ion beams are restricted to fields of view of roughly 100 micrometers. Recently, we have developed an automated process for layout designs with feature sizes from sub-nanometer to millimeter scales, using Raith lithography software in a Zeiss Orion Plus helium ion microscope. The technique relies on stitching writefields together and incorporating automated focusing algorithms in the Raith software. This procedure was demonstrated by scaling and automating the process of producing ion-damaged Josephson junctions in arrays in the high-temperature superconducting material $YB_2C_3O_{7-\delta}$. We demonstrate that the automated process reduces operator input while maintaining consistency at the smallest resolutions.**

***Index Terms*—Focused ion beam, HTS, josephson junction.**

I. Introduction

FOCUSED ion beam (FIB) technology is a promising candidate for the development of nanotechnology due to its sub-nanometer beam spot size. FIBs have applications in many fields providing a unique tool for imaging [1], milling [2], [3], resist exposure [4], [5] and ion beam assisted deposition [6], often achieving nanometer length scales. However, the technology remains relatively new and advanced lithography techniques remain undeveloped.

Recently, it was reported that a helium focused ion beam (He-FIB) is suitable for the fabrication of planar Josephson junctions in high transition temperature superconducting (HTS) cuprate $YBa_2Cu_3O_{7-\delta}$ (YBCO) [7]. Josephson junctions exhibit the quantum mechanical tunneling of superconducting charge carriers across a thin barrier between two superconducting electrodes. High-quality Josephson junctions have a high-potential barrier that is constrained to a length scale smaller than the superconducting coherence length. Exposure of HTS cuprates, such as YBCO, to ion irradiation was shown to cause a decrease to the critical temperature and an increase to the material resistivity proportional to the ion irradiation fluence. At a certain ion irradiation fluence, the cuprates undergo a transition from metallic to insulating properties [8]. Consequently, a He-FIB provides a controlled way to pattern the electrical properties at the nanometer scale in cuprate materials. This is crucial for localizing damage to a Josephson barrier below the length scale of the superconducting coherence length, which is reported to be on the nanometer scale in YBCO [9].

In the field of superconducting devices, there is motivation to develop techniques that are scalable to many junctions. For example, applications such as voltage standards and Josephson arbitrary waveform synthesizers rely on the fabrication of many junctions in series [10]. Recently, it was demonstrated that series arrays of long planar Josephson junctions are high-bandwidth, high-dynamic range magnetometers [11]. It was concluded that in order to achieve performance goals, the number of junctions arrayed in series would need to be increased by an order of magnitude greater than the series junction arrays presented in the article. This motivated the development of a new technique that would automate the process of achieving that increase in fabricated Josephson junctions across a large working area with a He-FIB.

The He-FIB provides a consistent platform for fabricating planar Josephson junctions with controllable placement. However, these junctions are sensitive to the beam spot size and deviations caused by stigmation, defocusing, stage mechanical vibration and stage drift which alter the junction properties and must be tuned precisely for high-quality junctions. Furthermore, a software limitation of the pixel resolution restricts the field of view to within a 100 μm^2 area so that minimum point-to-point pixel spacing is on the order of the beam spot size. This technical constraint threatened the feasibility of He-FIB patterning of larger and more complicated designs. In order to increase the scale of the design, a new control technique is necessary.

Raith ELPHY is a nanolithography upgrade kit that can interface with FIBs allowing for advanced control of the tool. The ELPHY attachment can be programed to control FIB parameters, stage control and nanolithography patterning. Lithography patterns are submitted in the conventional GDSII format, which then can be automated by organizing the FIB processing in batch job automation via scripting or ordering by position list. This software was utilized to develop a robust process for large scale lithographic designs involving a He-FIB.

We demonstrate a technique that utilizes the Raith lithography software ELPHY Multibeam connected to a Zeiss Orion Plus He-FIB for the automated processing of large-scale patterned areas. With an automated process, we will show that we are

Manuscript received November 25, 2020; accepted January 31, 2021. Date of publication February 4, 2021; date of current version February 26, 2021. This work was supported in part by Air Force Office of Scientific Research under Grant FA9550-20-1-0144, in part by National Science Foundation under Grant 1 664 446, and in part by UCOP MRPI under Award 009 556-002. *(Corresponding author: Jay LeFebvre.)*

Jay C. LeFebvre is with the Department of Physics, University of California Riverside, Riverside, CA 92521 USA (e-mail: jlefe001@ucr.edu).

Shane A. Cybart is with the Department of Electrical, and Computer Engineering, University of California Riverside, CA 92521 USA (e-mail: cybart@ucr.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TASC.2021.3057324.

Digital Object Identifier 10.1109/TASC.2021.3057324

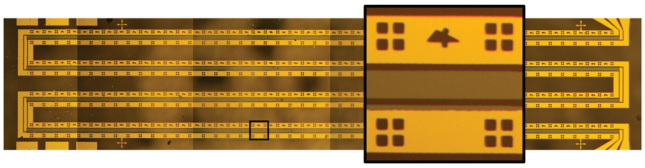

Fig. 1. Optical microscope image of the chip geometry for process testing. A single 100 μm writefield was enlarged for viewing the focusing structures and the YBCO electrode with an aperture opening for ion irradiation. At each corner, the crosses are necessary for automated alignment and focusing with the Raith ELPHY software.

able to expand the patterned area without significantly inducing deviations to the patterned elements, compared to previous manual techniques.

II. Experiment

Samples were fabricated for testing the large-scale He-FIB technique. We began our fabrication process for testing samples with a wafer of 35-nm thick YBCO grown via thermal reactive co-evaporation on a sapphire substrate and capped with 200 nm of gold grown $in\text{-}situ$ for electrical contacts. These wafers were commercially purchased from Ceraco GmbH [12]. The wafer was diced into 5-mm ^{2} chips, spincoated with photoresist, and then exposed with a Microtech LaserWriter laser lithography pattern generator. This process was done in order to define the large scale electrodes of the sample with a minimum feature size of 1 μm. After the photoresist was developed, the electrodes were isolated via an ion milling process using a broad beam of Argon ions.

Prior to writing with the He-FIB, a second lithographic process would need to be performed. Apertures in the gold cap layer were opened by chemically etching the gold away with Ki^+ etch. This second lithography process leaves the YBCO layer exposed for He-FIB irradiation, and is necessary because the He-FIB would not penetrate the gold cap layer. The results of the sample fabrication process can be viewed in Fig. 1.

In order to facilitate the Raith software for automated lithography, a pattern was specifically designed to meet the necessary requirements for a robust automated process. The design pattern was created by tiling together a series of 100 μm^2 areas such that each will become a writefield for the He-FIB. Each writefield is within acceptable restrictions for the field of view as determined by pixel resolution and within tolerances of spot distortion due to beam panning. Within each writefield, it is required that four crosses are lithographically defined. Raith software can interface with these crosses for automated alignment and focusing. Also, an aperture through the gold layer to the YBCO is opened in each writefield, exposing the middle electrode where the He-FIB will irradiate the YBCO. The two outer electrodes serve as magnetic field control lines, and contain the lithographically defined alignment marks. Finally, each writefield has a unique shape custom designed to be robust against lithographic defects and readily identifiable as a binary numbering system as an aid for determining stage location in the event of a pause during automated processes. Outside of the writefields, four global alignment marks were included near the corners of the sample for the creation of a three-dimensional coordinate map of the working area for matching with the He-FIB stage encoders. Each electrode in the writefield is continuously connected throughout each writefield and the entire sample to two contact pads for wirebonding to ground during He-FIB processes. It is important that all electrodes have low-impedance connections to ground because He-FIB images are produced by detecting secondary charged particles. A charged sample will reduce the He-FIB image contrast and may also deflect the charged beam. These layout geometry features can be viewed in Fig. 1.

The process of creating Josephson junctions with a He-FIB is straightforward. The He-FIB is scanned passing in a line across the entirety of the YBCO electrode width. The ion fluence on the material causes defects and dislocations in the material structure, creating the Josephson barriers. The Josephson junction properties are dependent on the beam parameters as well as the ion fluence. The He-FIB parameters are a 35 keV accelerating voltage and. 5 pA current. Additionally, the manufacturer claims a. 5 nm diameter spot size; however, this value is highly dependent on measurement methods as well as operator skill to optimize beam spot size. We estimate the practical beam spot diameter to be 3 ± 1 nm [13]. For this experiment, a He^+ fluence of 6×10^{16} ions/cm^2 was introduced to produce the Josephson barriers. For optimal Josephson junction performance at reasonably high-temperature applications, we design for junctions that operate at around $T_C/2$ which typically result in superconductor-normal-superconductor junctions.

For comparison, I will describe a manual process for writing Josephson junctions arrays previously utilized for writing with a He-FIB. Henceforth, I will refer to this process as the manual process. Without sophisticated patterning software, manual driving of the stage was necessary to align and focus at points near the writefield. The beam parameters were optimized at these points before moving to the writefield. Imaging with He-FIB introduces a small fluence of ion irradiation, and unplanned exposure to YBCO needs to be minimized in order to prevent degradation of the material. This process is repeated for each subsequent writefield and requires user input and concentration throughout.

Conversely, taking advantage of the sophisticated Raith lithography software, only the manual alignment and focusing process is required at the global alignment markers. Then, by creation of a single set of commands (referred to as a position list) writefields can be tiled and defined, following the design philosophy of the lithography pattern. Consequently, the He-FIB scanning process can be run in a single user input. Part of the input instructions to ELPHY program is a GDSII file, which is presented in Fig. 2. The sample geometry is drawn in the solid gray layer. Using alignment marks defined on this layer it is possible to map from the software to the stage encoders. The layer indicated by hatched pink relays where to use sample geometry for an automated alignment and focusing algorithm to the program. The green layers indicate instructions for exposure by the He-FIB. Writefields are then generated as indicated by the dotted red outline. The program will control the driving, focusing, and He-FIB exposure for all writefields in the position list. This automated process drastically reduces the need for

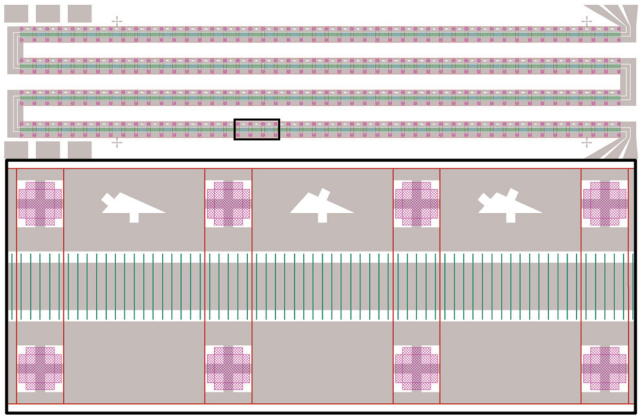

Fig. 2. Images of the GDSII pattern file that can be input as a portion of the directions for the automated write process. Top is the whole patterned device. Bottom is a detailed view of the three writefields outlined in black on the top image. Gray indicates patterned material, the green lines are the junction write locations, hatched pink is an indicator for the automated focusing lithographic features and the red lines outline the writefields.

manual user input and effectively stitches together the writefields for patterns of increased complexity. This will be referred to as the automated process. Effectively, we reduced the needed user input from O(N) to O(1) in Big O notation, where N is the number of necessary writefields for a given layout design.

Samples fabricated by each of the previous methods were compared. For both methods, long junction arrays were fabricated with junction widths of 20 μm, and inter-junction spacing of 5 um. Both were fabricated with similar beam parameters and doses. For the manual process, a junction array with 300 Josephson junctions was made while the automated process produced arrays of 2640 junctions. Each sample was fabricated in roughly the same duration of time. Discussion of the device performance will be limited to the properties related to their fabrication. For more discussion on the flux transducing properties of these devices, we advise you to this source [11].

In Fig. 3, the current-voltage properties of each device are presented at their respective optimized operating temperatures. For the determination of the device parameters, a resistively-shunted junction array model fit was used [11]. The normal state resistance (R) of the device scales as one would expect. However, from the fit there is a unexpected increase in critical current (I_C) which may be the result of measuring at a lower temperature and differences in dosage or material. Each sample was fabricated on separate Ceraco wafer runs and different He-FIB trimmer formations with significant time in between. The 300 and the 2640 junction array had 27% and 30% deviations in I_C respectively. Although fabricated in a different geometry and with different ion beam doses, four junction arrays with several hundred junctions in series written with the manual He-FIB technique were reported to have a $\sim$25 % I_C deviation [11]. The deviations of the junction parameters are used to estimate the deviation in the smallest elements of our pattern. Importantly, the fit suggests that there is not a significant worsening of the junction I_C deviation between the manual and the automated processes.

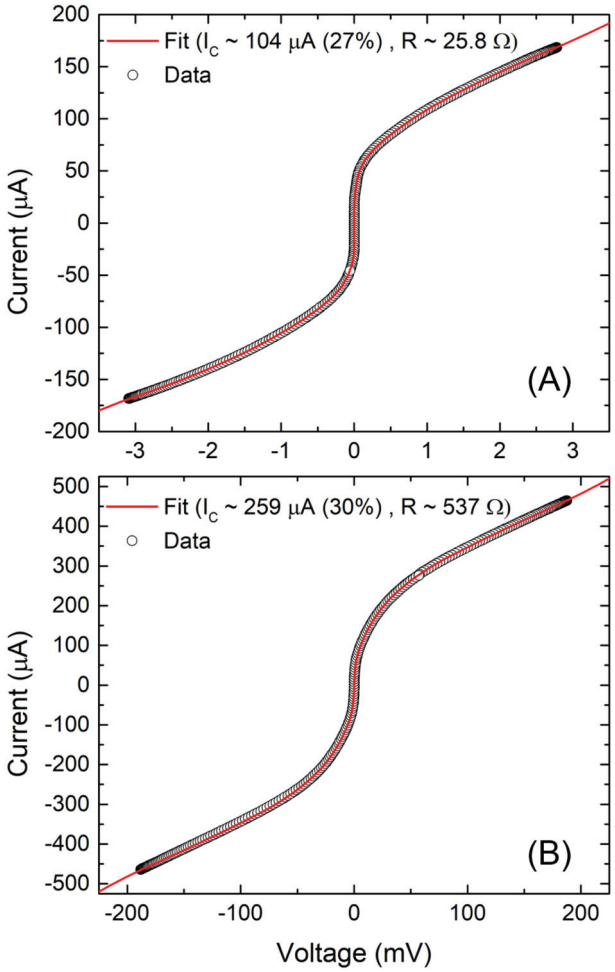

Fig. 3. Current-voltage characteristics (data in black circles) for each device with corresponding resistively-shunted junction array model fit (red line). A) is an array of the manual process with 300 junctions in series and is measured at 57 K and estimated 27% I_C deviation. B) Array fabricated with the automatic process with 2640 junctions and is measured at 51 K and estimated 30% I_C deviation. The fits indicate no significant worsening of I_C deviation between the two techniques.

We can partially account for this relatively high deviation in I_C from the limitations of the fitting model because it does not take into account thermal noise. Additionally, some deviation may be caused by the time-scale deviation in the beam parameters. For example, the beam current varies on long and short time scales, and while the long scale may be accounted for by measuring the beam current shortly before the write process for each field of view, we currently don't have the capability to measure the beam current during exposure. We can estimate deviations due to short time scale, which occurs at the time-scale of exposure (about 80 seconds per writefield), by measuring the deviation of total charge during a pulsed ion beam exposure which is 8%. Moreover, deviations to beam spot size and shape throughout the lithography process as the sample is moved to each writefield may contribute to junction parameter deviation. Finally, material properties may also contribute to the deviation of junction properties. Junction properties are innately tied to the material order parameter, which is known to be unconventional in YBCO.

Understanding these deviations in junction properties may yield information about the material itself but more investigation is warranted.

III. Conclusion

We have achieved scaling up the number of Josephson junctions in a series array by a factor of 10 and the lithographic total writefield size by a factor of 100 without a significant increase to the deviations of the patterned properties. These techniques lend themselves to scaling up other nanotechnology processes that are being investigated in FIB research fields.

However, the He-FIB process still produces junctions with a high deviation in parameters. For further improvements to He-FIB junction devices, improvements must be made for more consistent results. Suggestions for improvement include development of techniques for $in\text{-}situ$ measurement of beam current and material properties under exposure of the He-FIB.

Acknowledgment

The authors would like to thank the members of ONELAB for their insightful comments and support.

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