Coordination of Protection and Ride-through Settings for Islanded Facility Microgrids

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2021 IEEE Energy Conversion Congress and Exposition (ECCE) | 978-1-7281-5135-9/21/$31.00 ©2021 IEEE | DOI: 10.1109/ECCE47101.2021.9595450

***Abstract*—Proliferation of power electronics and distributed energy resources (DERs) into the electrical power system (EPS) enables improvements to the network's resilience against sudden-inception short circuit electrical faults through redundant electrical pathways in meshed configurations and multiple possible distributed generation locations. However, successful operation of fault detection, isolation, and recovery in islanded mode is challenging as protection coordination must include not only the distribution equipment, but also the DERs. Assessment of resilience for candidate EPS architectures against short circuit faults must be performed to understand the trade-offs between network resilience and complexity. This paper proposes a design process, which can be used towards assessing microgrid resilience, by coordinating protection and ride-through settings to maximize the recoverability of a meshed islanded AC microgrid. The design process is demonstrated through a case-study.**

***Index Terms*—Power System Protection, Microgrid, Low Voltage Ride-through, IEEE Standard 1547, Distributed Power Generation.**

I. Introduction

The exponential proliferation of power electronics into the electrical power system (EPS), enables islanded microgrids and provides the potential for meshed distribution networks with multiple DERs. By providing multiple power flow paths through ring or meshed architectures and multiple DER locations, the network can deliver the right amount of power to the right location at the right time, even in a highly degraded state. Each potential DER provides a design consideration which may affect the resilience of an EPS. Furthermore, power electronics enable dc distribution for new networks and hybrid ac/dc distribution system to connect new networks to existing ones. Then, within dc and hybrid ac/dc distribution systems, power conversion topologies and protection schemes have their own trade-offs, such as fault handling capability versus power density, which must be accounted for and which add more dimensions to the design space.

This work was partially sponsored by the NAVFAC Naval Shore Energy Technology Transition and Integration (NSETTI) program and by the National Science Foundation, Grant No. 1439700

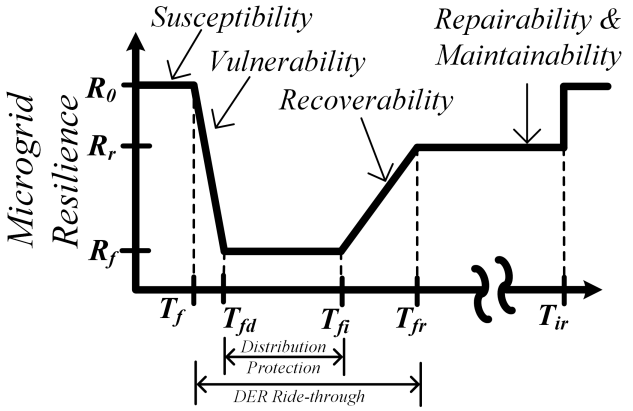


Fig. 1. Microgrid resilience with respect to fault recovery

A. Relating Resilience Taxonomy to Fault Detection, Isolation, and Recovery

As a result, to perform a fair comparison across candidate EPS architectures, we need to quantify resilience with metrics and established taxonomy. It should be recognized that in a similar endeavor, the field of computer architecture, the debate on Reduced Instruction Set Computer (RISC) versus Complex Instruction Set Computer (CISC) architectures could not be fairly compared until a set of metrics for computational performance were agreed upon in the mid 1980s [1]. However, quantification of microgrid resilience, and resilience of power electronic-based distribution networks in general, is still an emerging area of research [2]. Resilience may be thought of as the prevention of and response to high impact, low probability events, such as sudden-inception short-circuit electrical faults. Similar to concepts of dependability and survivability from communication and shipboard networks [3]–[6], resilience can be broken down into an set of quantifiable attributes such as, but not limited to: *susceptibility, vulnerability, recoverability, maintainability and repairability*.

Fig. 1 shows a qualitative curve of microgrid resilience over time in response to faults showing relationships between resilience attributes and events during fault detection, isolation,

and recovery process. *Susceptibility* is the ability to avoid failures. An example of improving this attribute is moving overhead cabling underground. *Vulnerability* is the ability to detect failures, and is applicable during the period between the time a fault is applied (T_f) and fault detection time (T_{fd}). For example, this attribute could be affected by the protective relaying settings, which may require a minimum amount of fault current to work, something which may be challenging in pure power electronic-based ac networks. *Recoverability* is the networks ability to recovery from a fault, which includes the time for fault isolation (T_{fi}), the time required for the distribution system protection to isolate the faulted branch of the network, and fault recovery (T_{fr}), the time required for the network to return nominal quality of power. The distribution equipment is active between fault detection and fault isolation, while the DERs go into ride-through between fault inception and fault recovery. This time may be affected by adjusting protection settings on distribution equipment or ride-through settings on DERs, or with the addition of energy storage to supply the network in post-fault recovery. *Repairability and maintainability* are the network's ability to be repaired and maintained, respectively. For example, an overhead cable is easier to repair than an underground cable. Quantification of this attribute as it relates to islanded microgrid resilience has been performed in [7].

B. Islanded Microgrid Protection and DER Fault Ride-through Coordination Challenges

Although quantification of resilience is out of the scope of this work, the quantification of the network's response to faults, both terms of post-fault recovery time and post-fault power availability, can be used as inputs to feed into a larger resilience assessment framework. To do this, the protection settings for the network have to be designed, and ride-through settings for the DERs have to be set to understand how the network can perform fault detection, isolation, and recovery, and to understand which DERs will remain connected post-fault. However, designing the protection for an islanded microgrid may be complex due to [8]:

1) operation in both grid-connected and islanded mode;
2) possible ring or meshed EPS architectures with bi-directional power flow;
3) DERs connected at various locations within the EPS;
4) DERs may or may not be active at the time of fault inception;
5) significant differences in fault currents characteristics between synchronous generator-based DERs, a combination of synchronous generator-based and inverter-based DERs, or just inverter-based DERs;
6) Allocation of protective functionalities between distribution equipment and power conversion equipment.

Little guidance has been given to the last point, as the convergence of power electronic-based DERs and conventional power systems into meshed networks is relatively new and requires acumen in both fields. DERs are required to meet ride-through and grid-supporting requirements per IEEE Standard 1547-2018 [9] when in grid-connected mode.

According to intentional islanding-mode, under section 8.2 of [9], DERs "shall trip" when subject to under voltage (UV) and under frequency (UF) as defined in sections 6.4 and 6.5, respectively. However in [9], ride-through requirements for only grid abnormalities are addressed, and abnormalities that can occur in islanded operation are not covered by this standard. With only mandatory "shall trip" settings and no ride-through settings, DERs in islanded mode may trip during load transients or prematurely during faults before the protection scheme can isolate the faulty branch. Premature tripping of DERs may significantly change the momentary generation capacity and may overload remaining connected DERs, leading to cascading failures and possible system blackout. Alternatively, without any trip settings, DERs may continue to operate under abnormal conditions, which can lead to DER equipment damage and other safety issues.

Recent works present protection schemes of islanded ac microgrids in the presence of inverter-based DERs [10]–[13], but have not taken LVRT capabilities into the account. [14] and [15] investigate LVRT controls for photovoltaic (PV) generation system, but are for grid-connected systems. In [16] system recovery and LVRT capability are both investigated for a grid-connected PV system, which has different requirements than an islanded microgrid. [17] presents a protection scheme and coordination settings considering LVRT through capability of the inverter-based DGs, but is a radial microgrid as opposed to a ring bus.

C. Novel Contribution and Paper Organization

The goal of this paper is to fill the gap identified in the above sections on the topic of microgrid resilience, and implementation of protective features in an islanded EPS. We investigate the recoverability from faults of an islanded ac microgrid with a ring bus structure, and both synchronous generator-based and inverter-based DERs. We also show that the coordination between power distribution protective-relaying settings and power conversion ride-through setting must be considered to maximize the recovery of the network as both impose limitation on each other, where the DER must ride-through the fault-isolation time of the protection scheme, and while simultaneously, the protection scheme must isolate the fault within the DERs ability to ride-through, and recover from, the fault.

We present a novel step-by-step process in Section II to design a microgrid's protection scheme. This section also introduces an example of industrial EPS as a case-study. Section III presents a fault characterization of the network, which will be used in Section IV to design and coordinate directional relay settings for the ring bus. Then, Section V implements category III LVRT from IEEE Standard 1547-2018 [9] with momentary cessation in the PV farm's controls to maximize the DERs connected during system recovery.

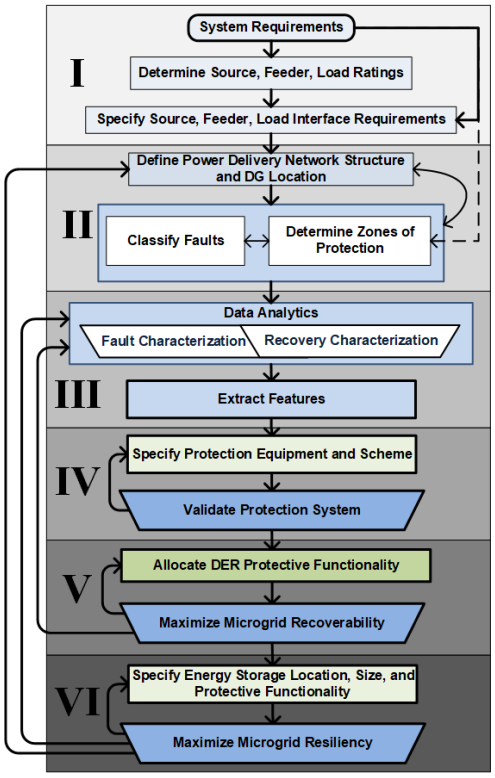


Fig. 2. Microgrid protection design process.

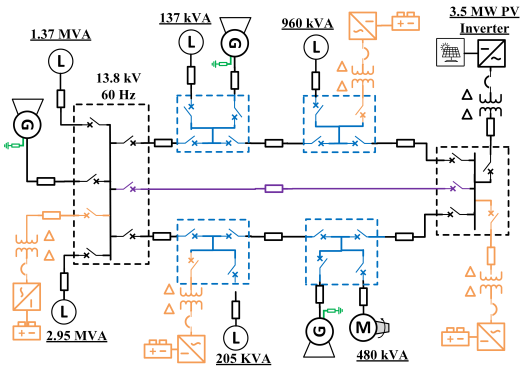


Fig. 3. Configuration options for Islanded AC Microgrid.

II. Microgrid and the Protection Design Process

Fig. 2 shows the process for systematically designing microgrid protection and is made in an effort to streamline protective design for complex networks. This iterative process was first proposed in [18], and modified for microgrid resilience.

Fig. 3 shows the islanded micogrid under consideration. The black lines represents the existing network of an industrial facility with critical loads. The facility is seeking to improve the resilience of their network in islanded mode, and assess possible infrastructure improvements such as: additional switchgear to improve fault discrimination capability around the ring bus (blue lines), a redundant pathway between the centralized gensets (left generator in Fig. 3) and the PV farm

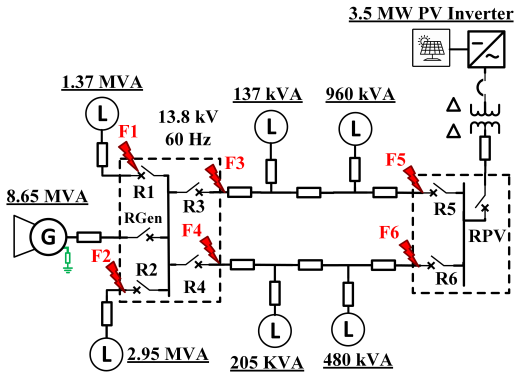


Fig. 4. Present Islanded AC Microgrid

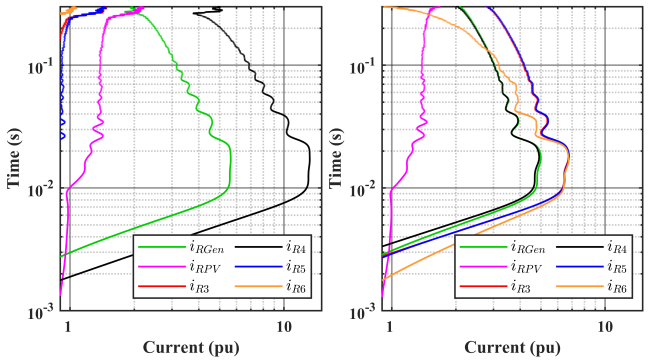
(purple lines), distributed energy storage (orange lines), and distributed genset locations (top and bottom generators in Fig. 3). However, first, the existing system must be benchmarked to later understand the resilience-cost trade-offs for each option.

Fig. 4 is the result of execution of steps I and II (from Fig. 2) through discussions with the industrial partner. Presently, the microgrid contains four 2.25 MVA / 1.725 MW diesel gensets, totaling 9 MVA / 6.9 MW in the centralized location. The facility can implement load-sheading during islanded-mode, to reduce the total load to 6.7 MVA, about 75% of the genset's capacity. The loads vary in power factor ratings from 0.85 to 0.95, and were sized using historical data. Cable lengths were determined from the facility one-line diagrams and physical layout. Recently, the facility has installed a 3.5 MW solar PV farm to reduce energy costs, which is located 3.5 km away from the diesel gensets.

III. Fault Characterization

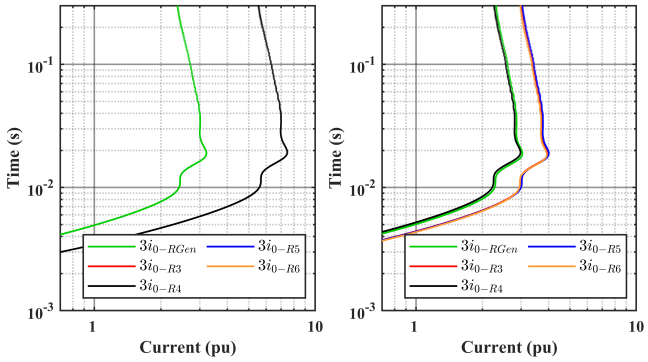
To properly assess the network during fault transients (steps III and IV) and post-fault states (step V), inertial dynamics, fault dynamics, and fault recovery enabling controls of synchronous and inverter-based DERs must be included. The diesel genset model contains engine delays, mechanical inertial dynamics, governor controls, IEEE DC1A exciter with automatic voltage regulator (AVR), and 5th-order salient-pole dq model of the synchronous machine. The PV inverter is modeled as 2-level 3-phase inverter with LCL filter and grid interfacing delta-delta transformer. All the DERs utilize state machine-based control structures to ensure sequential operation of grid connection, ramping up/ramping down, ride-through, and participation in fault recovery efforts. The circuit breakers are also equipped with state machines, which simulate opening/closing actuation. The opening time of the breakers is set to three 60Hz cycles + 20%, or 60 ms.

The model is simulated in Matlab/Simulink with the SimPower Systems blockset. The SimPower Systems blockset synchronous machine does not have an accessible neutral point, so a zig-zag transformer was added to the output of the machine, forming a low impedance grounded system, both to provide a path for, and to limit, the ground fault current.



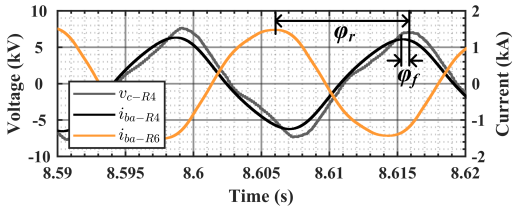
(a) (b)

Fig. 5. Inverse-time curves for RMS i_b current at locations (a) F4, (b) F6.

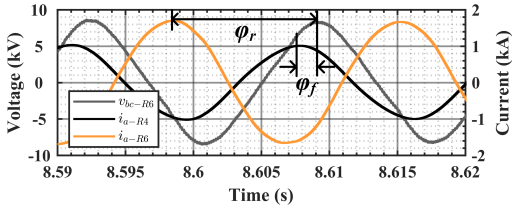


(a) (b)

Fig. 6. Inverse-time curves for RMS of $3i_0$ current at locations (a) F4, (b) F6.



(a)



(b)

Fig. 7. Phase angle characterization for (a) LL and (b) LG faults at F6 location.

Fault characterization is performed on this network by applying Line-to-Line (LL) and Line-to-Ground (LG) faults at the locations shown in Fig. 4 without any protective features active. This implies 12 simulation runs to characterize the fault response of the network at all the location, and further simulation runs will be needed to test and validate protection and ride-through settings for steps IV and V in Fig. 2. This leads to conflicting simulation requirements of: 1.) small time-steps; 2.) detailed DERs to capture control responses and filter dynamics; 3.) potentially many DERs locations and network configurations; 4.) long run-times due to slow internal dynamics of synchronous machines; 5.) many iterations to perform validation and verification throughout the design process. To accelerate the simulation process and address these conflicting requirements, the model was compiled and executed on an OPAL-RT 5600 industrial pc in simulation-mode (non-real-time). The platform is controlled through a Python API to iterate through possible fault locations and types, and is also used to validate settings determined in Sections IV and V. For this work, LG faults were applied to phase a, and LL faults were applied to phase a and b.

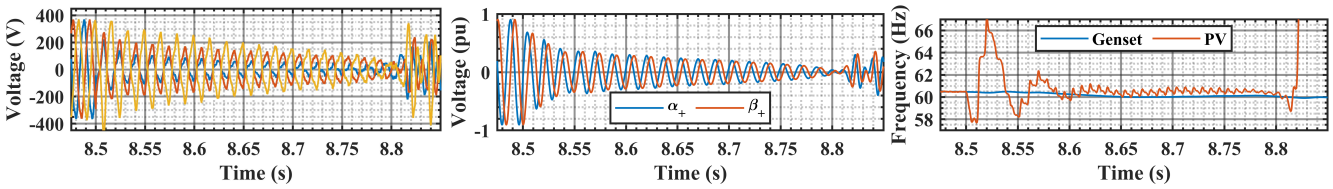
Fig. 5 shows the per-unit (pu) RMS currents measured at each relay location for LL faults at locations F4 and F6, and is plotted on inverse-time curves. Only phase b RMS current (i_b) is plotted, since both phase a and b currents are similar. Likewise, Fig. 6 shows the RMS of $3i_0$, where i_0 is the zero sequence current, measured at each relay location for LG faults. The generator relay (RGen) pu is the current rating of the generator, and the pu of the relays on the ring bus (R3-R6) and the PV relay (RPV) are the current rating of the ring bus/PV farm. i_0 was not plotted for RPV, as the transformer blocks the flow of zero sequence current. The curves are slightly offset for visibility.

The fault currents are dominated by the sub-transient and transient dynamics of the generator, while the PV farm contributes a little, almost negligible, fault current to the network during LL faults. The fault current at F4 only flows from the left side of the ring bus through RGen and R4, while fault current at F6 flows in both directions, through the RGen-R4 path and through the RGen-R3-R5-R6 path. The cabling between the top and bottom parts of the ring bus are of similar but not exactly the same distances. This is why the fault current magnitudes at F6 through R3 and R4 are close but not exactly the same.

Because the fault current flows from two directions, directional sensing will be required for the protection scheme. Directional sensing is performed by taking an unfaulted voltage and one current measurement. For a LL fault between phase a and b, the angle for forward direction (ϕ_f) was determined by comparing v_c and i_{ba} ($i_b - i_a$). For a LG fault for phase a, the angle is determined by comparing v_{bc} and i_a. The forward zone of the relay is then $\phi_f \pm 90°$.

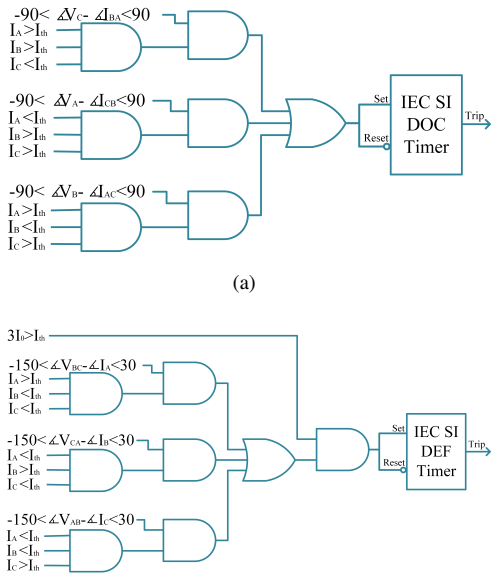
The reverse zone of the relay (ϕ_r) is 180° offset from ϕ_f. Fig. 7a shows characterization for LL faults, which will be used for directional overcurrent (DOC) relays. Fig. 7b characterizes the phase angle for LG faults to be used by directional earth fault (DEF) relays. The forward zone is set to $0° \pm 90°$ for DOC relays and $-60° \pm 90°$ for DEF relays.

Lastly, inverter-based DERs can only ride-through to the extent to which the PLL can maintain synchronization with



(a) (b) (c)

Fig. 8. LL fault at F6: (a) PV v_{abc}, (b) $v^{+}_{\alpha\beta}$, and (c) frequency.



(a)

(b)

Fig. 9. Relay trip logic: (a) DOC, and (b) DEF.

TABLE I
DOC AND DEF RELAY SETTINGS.

Relay	I rated (A)	DOC TMS	DEF TMS
RGen	363	0.019	0.08
RPV	159	0.007	N/A
R1	74	inst.	inst.
R2	167	inst.	inst.
R3	159	0.015	0.04
R4	159	0.015	0.04
R5	159	0.00175	0.001
R6	159	0.00175	0.001

the positive sequence voltage. Fig. 8a shows the voltage collapsing during a LL fault at F6. Positive sequence voltage was extracted in the stationary reference frame ($v^{+}_{\alpha\beta}$) using multiple second-order generalized integrators (MSOGI) presented in [19], and shown in Fig. 8b. As $v^{+}_{\alpha\beta}$ approaches zero, the PLL no longer maintains synchronization, as no positive sequence voltage is present to synchronize with. The loss of synchronization is shown in Fig. 8c by the frequency going outside normal bounds around 310 ms after the fault.

IV. PROTECTIVE RELAY DESIGN

Following the fault transient characterization, the protection design can be performed (step IV). IEC 60255 standard inverse (SI) curves were used for current-time calculations for the DOC and DEF relay settings, where the SI curves are governed by [12]:

$$t = TMS\frac{0.14}{(I/I_s)^{0.02}-1} \tag{1}$$

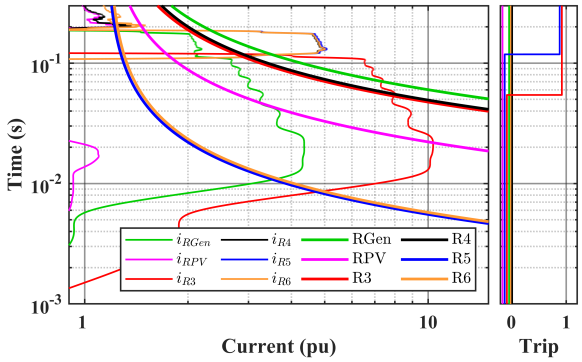
where TMS is Time Multiplier Setting, I is the RMS current in pu, and I_s is the pick up current in pu.

The curves where adjusted to account for the 60 ms opening time of the breaks. The forward direction assumes current is flowing from left to right of the network. R3 and R4 are set to operate in the forward direction, and R5 and R6 are set to operate in the reverse direction. As the magnitudes of fault current at F3 and F4 were similar, the settings of R3 and R4 are assumed to be the same, and similarly with R5 and R6. However, as there is only one source fault current that can flow through parallel branches, some subtleties need to be considered in the coordination of relay settings. If the settings of R4 and R6 are set at the same levels and a fault occurs at F6, then not only will R4 and R6 trip, but also R3 will trip due to the secondary fault current path of RGen-R3-R5-R6. R5 would not trip, as the fault current at F6 would be in the forward direction. Additionally, if a fault occurred at F5, not only R3 and R5 trip, but also R4. Because of this, settings for R3/R4 were increased sufficiently to allow for R5/R6 to trip, the breakers to open, with some additional margin, as the RMS calculation takes half to one cycle to update.

For faults at F3/F4, R3/R4 would trip, causing the fault current to flow around the ring bus through the opposite branch, subsequently tripping R5/R6. Lastly, RGen is set above R3/R4 to ensure it does not trip while the breakers of F3/F4 are opening.

Fig. 9 shows the logic implemented for DOC and DEF relays to account for magnitude and direction. The final settings are tabulated in Table I. The pickup current for DEF was set to 0.15 pu of rated current, as sufficient zero sequence current is only present under fault conditions. The pick up currents for DOC relays were all set to 1.15 pu.

Fig. 10 and Fig. 11 show fault currents overlayed with the relay's time-trip curves and the relay's trip signals for each fault location for LL and LG faults, respectively. The relay's trip signal go high after the trip conditions are met, and are



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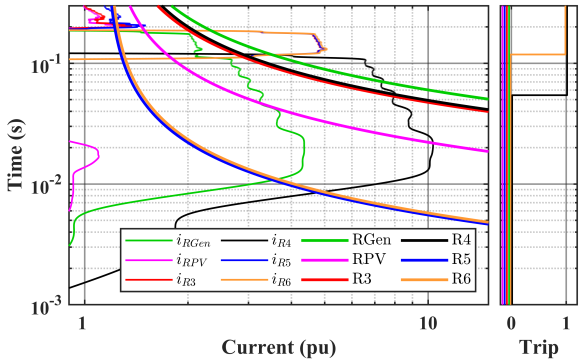

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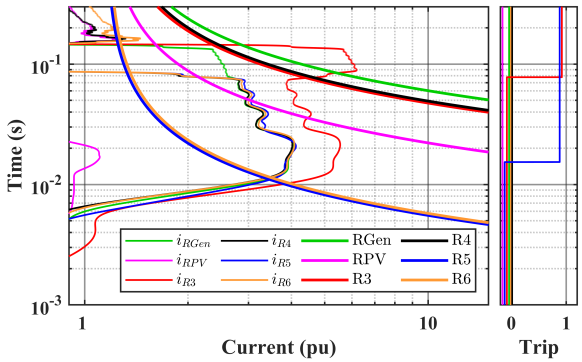

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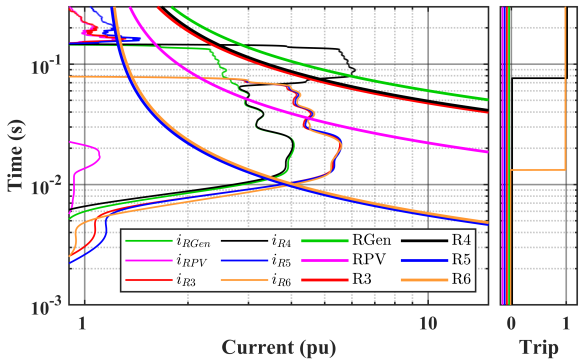
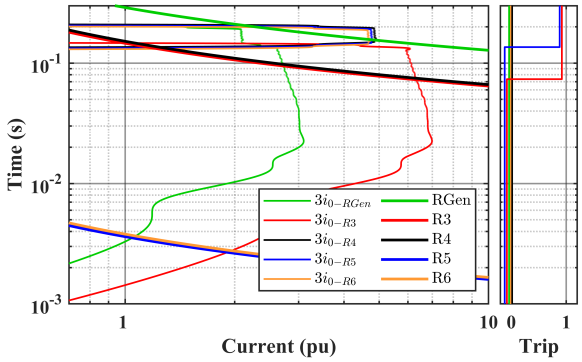


(d)

Fig. 10. Inverse-times curves of RMS i_b current with DOC relay settings (left) and relay trip signals (right) at locations: (a) F3, (b) F4, (c) F5, (d) F6.



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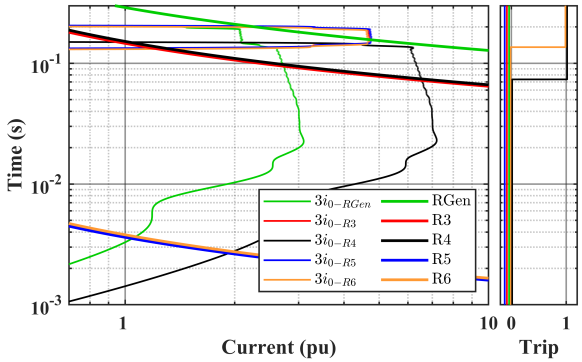

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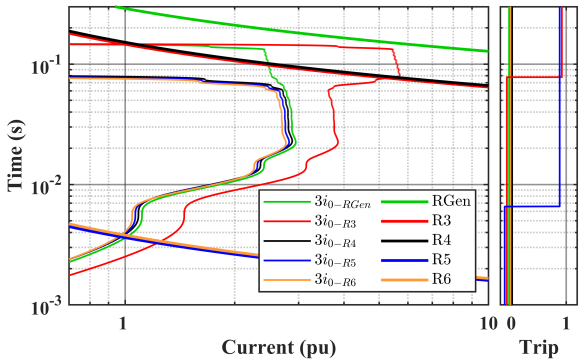

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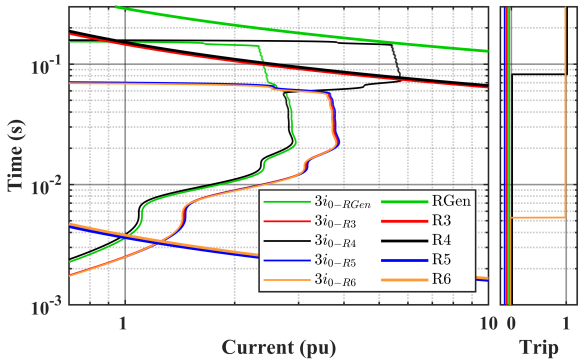

(d)

Fig. 11. Inverse-times curves of RMS $3i_0$ current with DEF relay settings (left) and relay trip signals (right) at locations: (a) F3, (b) F4, (c) F5, (d) F6.

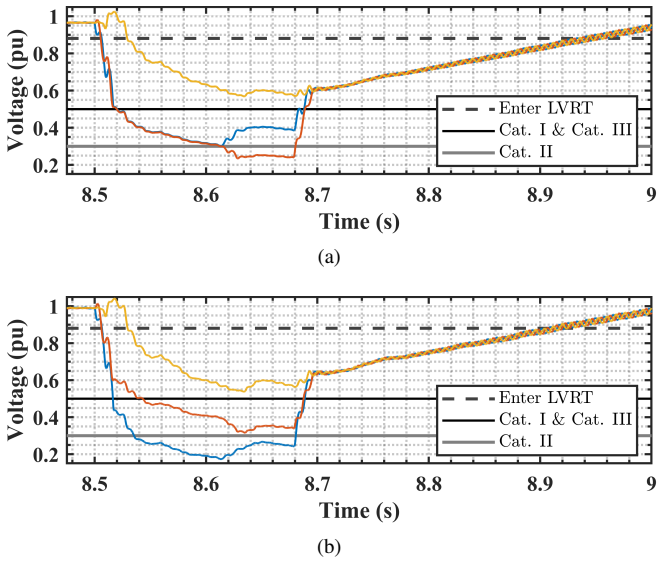

Fig. 12. RMS pu voltage during FDIR process against IEEE Standard 1547-2018 lower limits across all 3 categories for: (a) genset, and (b) PV.

color coated to match the relay measurements and time-trip curves. As can be seen in the figures, both the protection settings and the direction conditions correspond to the correct set of relays to trip, according to associated fault location and fault type.

For example, Fig. 10d shows the R6 trip signal going high shortly after the fault current intersects the time-trip curve for LL fault at F6. Then after the breaker opens, the current stops flowing through R3-R5-R6 path and the current increases in the R4 path, causing the R4 relay to correctly trip. Fig. 10c shows the same behavior but with the R5/R3 relays at F5. Likewise, similar behavior is seen in Fig. 10a and Fig. 10b, but with the R3/R4 relays tripping first, then R5/R6 relays. Similar behavior occurs for LG faults throughout Fig. 11.

V. Low Voltage Ride-through Settings

With the protection setting implemented, LVRT settings can be selected and tested (step V). Fig. 12 shows the RMS voltage in pu for the genset and PV while the protection scheme is isolating the fault, and is plotted against IEEE Standard 1547-2018 lower limit lines. RMS was shown to be accurate compared to other peak detection methods in the presence of harmonics, specifically when used for the voltage abnormalities in IEEE Standard 1547-2018 [20].The voltage response is shown for a LL fault at F4, since LL faults have the lower transient voltages and faults at F3/F4 have longer relay trip times.

The assumption that the DERs must trip if the voltage falls below the limit is understandable from an initial read-through, but careful understanding of the terminology and examination of the footnotes in [9] are required. Category (Cat.) I and category II ride-through have lower limits lines of 0.5 pu and 0.3 pu, respectively. The standard recommends "Cease to Energize" if voltage falls below the lower limit. Category

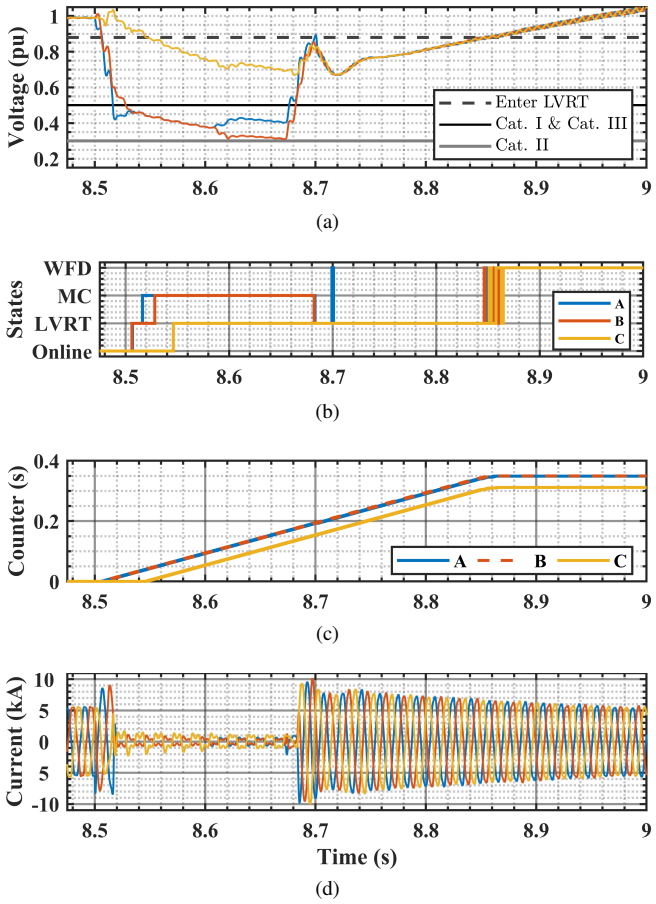

Fig. 13. PV category III LVRT state machine: (a) v_{abc} RMS pu, (b) states, (c) counter, and (d) i_{abc}.

III also has a lower limit line of 0.5 pu, but recommends momentary cessation (mc) with a minimum ride-through time of 1 s. "Cease to Energize" can be misleading as "This does not necessarily imply disconnection, isolation, or a trip of the DER. This may include momentary cessation or trip," while momentary cessation is to "Temporarily cease to energize an EPS, ... with the capability of immediate Restore Output of operation when the applicable voltages and the system frequency return to within defined ranges." [9].

Because the voltage levels dip below the limit lines for all three categories, momentary cessation should be considered. Momentary cessation is not possible for the genset as the fault current from the genset is used for the fault location, and the system would go dark. Momentary cessation is possible for the PV farm as it does not contribute to fault current used for fault location, but is not required. However, it seems wasteful for the PV farm to continue to output power into a fault without benefit to the system. Also, momentary cessation would reduce thermal stress on the power electronics during overcurrent condition induced during the fault.

For the PV farm, momentary cessation would imply temporary stop to gating of the power electronic system, which can easily be implied. The allowable time for momentary cessation

is not specified, and for this work is assumed to be the time listed in category III minimum ride-through time for 1 s.

To execute LVRT, a state machine was implemented which transitions from the Online state to the LVRT state in the presence of voltage abnormalities, then to the Momentary Cessation state if the voltage dips below 0.5 pu. The PV inverter stops gating until the voltage returns to 0.55 pu, the frequency is between 55 to 65 Hz, and the $|v^{+}_{\alpha\beta}| \geq$ 0.2 pu. The state machine then transitions to the Wait For Disturbance (WFD) state to allow for sufficient time to pass between disturbance events to reset the ride-through counter, as specified in Section 6.4.2.5 [9]. IEEE Standard 1547-2018 specifies the lowest voltage phase should be taken into account, so a state machine is implemented for each phase, where the outputs for fault or momentary cessation are OR'ed in the control system.

Fig. 13 shows the PV performance using category III ride-through as the state machines for each phase cycle through different states in response to the voltage abnormality. The PV can be seen entering and leaving the Momentary Cessation state in Fig. 13b and the output current is reducing in Fig. 13d on the low voltage side of the transformer, while the protection system isolates an LL fault at F4. The remaining current is from the interaction between the network and the LCL filter. The protection system isolates the fault (T_{fi}) around 200 ms after fault inception and recovers from the fault (T_{fr}) around 400 ms.

VI. Conclusion and Future Work

This work introduces a step-by-step methodology to design and validate protection settings in distribution equipment and ride-through settings in DERs. The design process was demonstrated successfully on an islanded ac microgrid with a ring-bus structure with both inverter-based and synchronous machine-based DERs. This work shows that for islanded microgrids, where the voltage transients during faults can be significant, LVRT settings may need to be increased to category III ride-through and may need to include momentary cessation operation into the controls. The former increases the ride-through time of DERs while the protection system operates and the latter enables DERs, that would otherwise trip due to low voltage levels, to remain connected and participate in system recovery.

With the network baselined, the network improvements discussed in Section II can be also be executed through this design process and benchmarked against the baseline network. Lastly, the outputs of this work will be used to feed into a larger effort to quantify resilience of microgrids (step VI of Fig. 2).

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