Virtual Prototyping Process For Assessment of Medium Voltage Grid-Connected Solid State Transformer Implementations

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***Abstract*—This paper presents a unique Virtual Prototyping Process (VPP) that allows for metaheuristic optimization of the building block based Power Electronic Converter systems. The VPP allows for exploration of a range of design space variables, including voltage levels, power semiconductor device technology and thermal management approach against competing objectives such as power density, efficiency and specific cost given electrical and environmental constraints. A unique feature of proposed VPP is compilation of lower voltage building blocks into a much higher voltage rated system and inclusion of allocations for insulation systems, thermal management, accessibility, busing/interconnections and frame/structure/chassis. This approach enables understanding of these practical considerations on power density. This paper presents a use case of a Medium Voltage ac (MVac) to Low Voltage dc (LVdc) solid state transformer.**

***Index Terms*—High-Frequency Transformer, Wide band gap semiconductors, AC-DC power converters, Virtual prototyping, Genetic algorithms.**

I. Introduction

The emergence of commercially viable Wide Band Gap (WBG) power semiconductor modules has presented tremendous possibilities for power electronics-based energy conversion and distribution in medium voltage grids. The packaging of WBG power semiconductors into electrical systems that interface directly to the medium voltage grid (without an intervening isolation transformer) is driving new paradigms in the areas of magnetics 14 design, dielectric materials, insulation systems, and thermal management. However, Power Electronic Converter (PEC) equipment manufacturers, electrical system developers and other stakeholders face many choices regarding focus in technology investments whether the promised capabilities, particularly those associated with energy efficiency, can be achieved at a system level. The combination of virtual prototyping with multi-objective optimization has been introduced and applied to power electronic conversion system analysis in order to (1.) assess increases in power density, efficiency and specific cost (power per cost) that can be achieved with new topologies, modulation schemes and WBG power semiconductors [1]; (2.) concurrently optimize within thermo-electrical, thermo-mechanical and electromagnetic design domains; and (3.) assess the merit of one topology versus another [2]. This paper describes a Virtual Prototyping Process (VPP) tailored to assessment of PEC-based medium voltage electrification systems made up of common, multi-use building blocks, as described in Fig. 1. The approach is well suited to shipboard electrical systems [3]–[5]. The aim of the approach has been to enable the assessment of a range of design space variables, such as medium voltage distribution levels, component selection, thermal management approach, etc. In this paper, the VPP of Fig. 1 is applied to discover which commercial 1200V WBG Silicon Carbide (SiC) MOSFET multi-chip power module(s) are the best choice for design of a common use Power Electronic Building Block (PEBB). This PEBB is used specifically to build up a Medium Voltage ac (MVac) to Low Voltage dc (LVdc) Input Series Output Parallel Solid State Transformer (ISOP SST) for applications such as multiple electric vehicle (multi-eV) fast charging [6]–[8] and dc microgrids.

The VPP enables exploration of a range of design space inputs that are important to stakeholders in future electrical infrastructural changes, ground-up installations and building projects. Assessment of the best design, for a given application, system or market requires multi-disciplinary design optimization against competing objectives, i.e., efficiency (η), power density (ρ), and specific cost (σ). For building-block based systems, the VPP relies upon Pareto-optimal design explorations and co-design of thermal management systems with PEBBs, MF transformers, inductors, dc link capacitors, EMI filters and other Lowest Replaceable Units (LRUs). Practical considerations are also considered, such as accessibility and maintainability of LRUs and the creepage and clearance of electrical interconnecting assemblies when lower voltage rated comprising the system are connected in series to support direct, transformerless connection to the MVac system voltage. The proposed approach is especially helpful in highlighting

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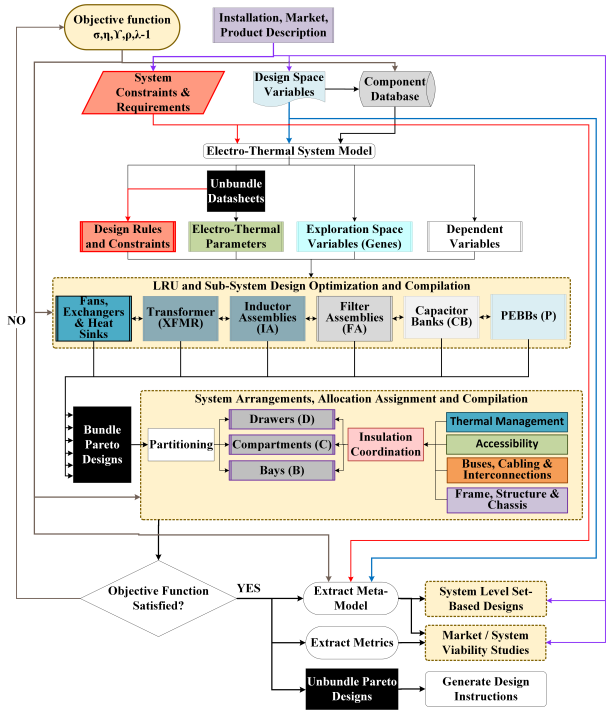


Fig. 1. Virtual Prototyping Process

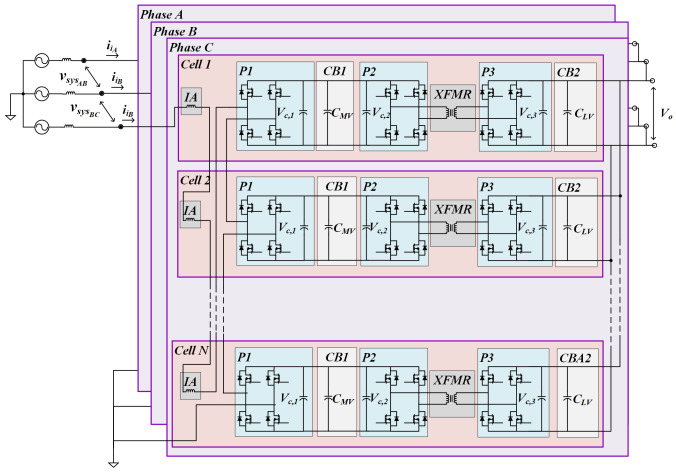


Fig. 2. System Implementation

the impact of the insulation system approach on the realizable power density of the final system. The proposed VPP allocates the physics of insulation, interconnection, frame support and thermal management into meaningful rectangular geometries.

This work looks at the use case of the MVac interface of a multi-eV fast charging system based on the ISOP SST, as shown in Fig. 2. It builds upon prior studies on the virtual prototyping of building block-based systems [9]–[11]. The VPP flow shown in Fig. 1, enables design space exploration and cause and effect of upfront design decisions, such as PEBB power semiconductor choice. Such decisions can be assessed against MVac voltage level of the installation, which will be covered in future work. In this work, a single building block cell of the ISOP SST is optimized for power density and efficiency for each power semiconductor choice using a multi-objective non dominated genetic sorting algorithm (NGSA II) [12]. Since a common-use PEBB is utilized, the heat sink is optimized for the Active Front End (AFE) PEBB (P_1 in Fig. 2) by constraining operation of the power semiconductors to a maximum junction temperature (T_{jmax}) (dictated by the device selection). The optimal Dual Active Bridge (DAB) mdeidum frequency (MF) transformer design is constrained by the AFE heat sink design and thermal viability of the transformer (given the installation environment). Such an approach tends towards maximization of power density ($/rho$), but the NSGA II also pushes the design in other directions by considering competing objectives, such as efficiency ($/eta$). The NSGA II is a fast sorting and elite mult-objective genetic algorithm (GA) that is well-suited to the optimization of highly nonlinear, multi-disciplinary systems where a Pareto-optimal front of multiple feasible designs and multiple local minima exist. The degree of competition between maximization of other objectives, such as specific cost σ, reliability and specific power (ratio of power to overall system weight, γ), may also be considered. The intent is to understand the impact of SiC MOSFET switching frequency and other device characteristics on power density and switching frequency. It is important to ensure that devices on the AFE PEBB heat sink operate as close as possible to T_{jmax} while maximizing the power throughput of the DAB power stage. The nominal (or rated) power of the system is dependent on considerations of DAB switching frequency and transformer leakage inductance against thermal constraints.

II. System Implementation and Virtual Prototype

The circuit topology of Fig. 2 uses common LRUs to build up the cells that comprise the ISOP SST. This modular approach is pursued in order to allow for a common, multi-use PEBB and, potentially, other common-use LRUs in order to explore the possibility of reducing cost through production economies of scale. While the stated application is for MVac interfacing, multi-eV fast charging stations, the same ISOP SST can apply to a range of applications, including microgrids and shipboard systems. The authors' VPP is aimed at helping equipment manufacturers, system integrators and installation decision makers make informed decisions up front to inform everything from the dedication of engineering resources to other product/market decisions. A PEBB design that can apply not only to a range of applications of the same topology but other topologies as well, such as Modular Multi-Level Converters (MMCs) has significant benefits, even beyond production economy of scale, such as highly maintainable systems, interchangeability of parts and reduction of spare inventory (the last of which is extremely important to shipboard applications).

With this system implementation, identical cells are connected in series on the MVac side and in parallel on the

LVdc side. The system is organized so that each cell is a maintainable *drawer* comprised of the following LRUs: MVac-side filter inductor assembly (IA), three identical PEBBs that are controlled differently according to function, MF transformer (XFMR), MVdc-side dc link capacitor bank (CB1) and LVdc-side dc link/stabilizing capacitor bank (CB2). The intention is to use the same LRUs over a range of nominal RMS MVac voltage levels, from 690V to 13.8kV and to maximize the possibility for LRU multi-use. PEBBs are forced-air cooled through finned heat sinks in order to enable isolating (or floating) the PEBBs, and transformer core from the system chassis. Additional air clearance space is added around the floating PEBBs and magnetic components as installation voltage rating is increased. This approach will allow for cells made up of optimally designed low voltage LRUs, having a *functional insulation* capability that is much lower than the system-level insulation voltage requirement, in series to achieve higher MVac rated voltage installations. Clearly, packaging of the system in this manner will not achieve the high power density of monolithic, highly integrated cell designs that have been reported in the literature [13]. However, the approach allows for simplicity in the insulation system and thermal management system designs and other benefits associated with cost, maintainability and availability that have been mentioned. Exploration of the impact of this approach on cost and, generally, life cycle cost, will be addressed in future work.

The VPP enables optimal scaling within the constraints of the type of building-block based PEC described above. The VPP is unique in that it relies upon an ontology consisting of LRUs organized into (Drawers), which are then arranged into *Compartments*. A vertical *Bay* is used to define the final equipment outside dimensions and represents some functional sub-system (such a phase leg), so multiple, identical bays can be used scale up the final system outside dimensions, mass, cost, losses, and reliability. The *Bay* may have vertically and horizontally arranged *Compartments* containing *Drawers*, buses and interconnects, cabling, fans, heat exchangers, air flow paths, etc. Each level of the ontology (LRU, Drawer, Compartment, Bay) contains dimensional *Allocations* for insulation or *Dielectric Stand-off* distances around LRU surfaces or between components and sub-assemblies having disparate Decisive Voltage Classifications (DVCs), *Thermal Management* (fans, air flow, heat exchangers, pipes, etc.), empty space or drawer rail space representing *Accessibility* and practical spacing for manufacturing, *Buses, Cabling and Interconnection* and *Frame, Structure and Chassis*. A candidate layout for a cell drawer is shown in Fig. 3, including color codes for the *Allocations*. This approach to the virtual prototype is illustrated to provide context for the optimization of PEBB and XFMR in this paper. Future work will demonstrate the optimization of the arrangements of the LRUs within the drawers.

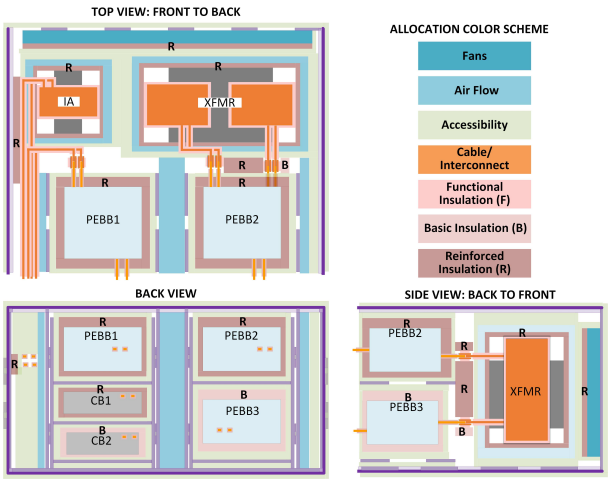


Fig. 3. Cell Drawer layout showing arrangement and allocations

III. Methodology

The promise of WBG power semiconductors is increasing the working frequency of power converters to increase power density. In this paper we examine the hypothetical limits of minimizing the volume of a forced-air convective cooling framework composed of fans and heat sinks for a desired heat resistance ($R_{th,sa}$). The methodology involves various aspects of a power electronics design paradigm presented in [6], [14].

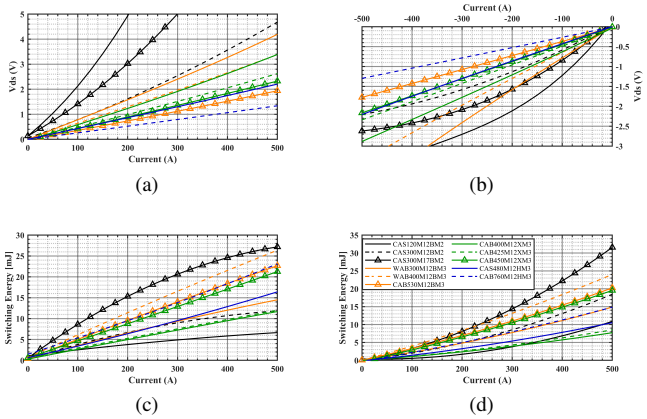
AFE and DAB switching frequency, $f_{sw,AFE}$ and $f_{sw,DAB}$, represent two of the *exploration space variables* (see Fig. 1) that are exercised by the NSGA II. At the ISOP SST cell level, the algorithm cycles through all the available power devices listed in Table II. The range of considered devices is treated as a gene around which the LRU optimizations are formulated, and are derived from a device component database from which design rules and constraints and electro-thermal parameters are extracted (through an *unbundling* process. In a similar manner, a fan component database [15] is utilized for heat sink optimization. Table I considered [12].

Design and exploration space variables are governed by the objective function listed in the Fig. 1 so that the NSGA-II ensures that VPP to populates a non-dominated front of competing objectives listed above using the the constraints and the space variable as shown in Fig. 10d. The VPP automates the process of bundling and unbundling parameter choices within correlating Pareto-optimized designs to the design space variables. This enables meta model generation similar to [16]. As a result, the VPP enables traceability to desired design, its meta-model and the Design space variables and constraints considered in Tables III & I.

For the devices listed in Table II, switching energies and drain-source voltages, including 3rd-quadrant operation. This is an important distinction between the loss calculations for third generation SiC MOSFET modules compared to second generation devices, which have a separate SiC diode in parallel with the MOSFET [17]. In order to extract relationships between operational current and the datasheet quantities from

TABLE I
SST GA DESIGN SPACE

Min.	*Max.*	*Enc.*	*Gene*	*Sym.*	*Description*
6	18	1	1	mc	*Core material*
1e-04	5	3	2	lcc	*Length of core center (m)*
1e-04	5	3	3	rc	*Rounding radius of core end leg (m)*
1e-04	5	3	4	wcec	*Width of core end leg center (m)*
1e-04	5	3	5	wcb	*Width of core base top leg (m)*
1	1	1	6	mp	*Primary material*
1e-06	1e-03	3	7	aptstr	*Desired total area of all primary coil parallel conductors*
1	5	1	8	Npprstr	*Number of primary conductors in parallel*
1	1000	3	9	Npclstr	*Desired number of primary turns per coil*
0.2	1e+05	3	10	rpdw	*Desired primary coil depth to width ratio*
1	1	1	11	ms	*Secondary material*
1e-06	1e-01	3	12	aststr-	*Desired total area for all secondary coil parallel conductors (m2)*
1	10	1	13	Nsprstr	*Number or secondary conductors in parallel*
Rpsmn	Rpsmx	2	14	Rpsstr	*Desired primary to secondary turns ratio*
0.2	1e+05	3	15	rsdw	*Desired secondary depth to width ratio*
2e+04	1e+05	3	16	fswAFE	*Desired Switching Frequency AFE (Hz)*
5e+04	1e+05	3	17	fswDAB	*Desired Switching Frequency DAB (Hz)*
1	11	1	18	Device ID	*Device ID*
1	35	1	19	Fan ID	*Fan ID*



(a) (b) (c) (d)

Fig. 4. Comparison of Cree-Wolfspeed SiC MOSFET modules: (a) conduction, (b) conduction in 3rd quadrant, (c) turn-on energy, and (d) turn-off energy.

TABLE II
SIC POWER DEVICES BEING CONSIDERED

Device Name	*VB(V)*	*USD*	*Rcs (Ω)*	*Tjmax(C)*
CAS120M12BM2	1200	336.64	0.037981	150
CAS300M12BM2	1200	576.63	0.037981	150
CAS300M17BM2	1700	868.68	0.037981	150
WAB300M12BM3	1200	592.11	0.038655	175
WAB400M12BM3	1200	730.25	0.037981	175
CAB530M12BM3	1200	701.04	0.037981	150
CAB400M12XM3	1200	679.45	0.058871	175
CAB425M12XM3	1200	764.97	0.058871	175
CAB450M12XM3	1200	835.52	0.058871	175
CAS480M12HM3	1200	2,157.73	0.034911	175
CAB760M12HM3	1200	2,792.73	0.034911	175

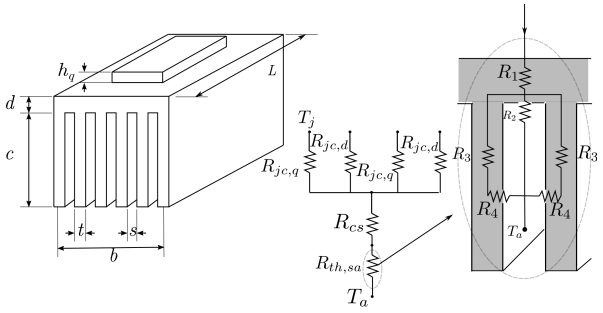


Fig. 5. Heat sink dimensions and equivalent thermal resistances.

which device losses are calculated, data points were extracted from XML files provided by the device manufacture at Tjmax. Then, 3rd-order curve-fits were applied on drain-source voltages (V_{ds}) for conduction losses to capture both the 1st and 3rd-quadrant operation, and 2nd-order curve-fits were applied to turn-on and turn-off energies. Comparisons are plotted in Fig. 4. Simplified loss expressions for a single device were derived using the methods described in [6], [18], [19]. Curve-fit functions for the device characteristics shown Fig. 4 were integrated into these expression in order to calculate AFE and DAB devices losses.

IV. HEAT SINK DESIGN

A heat sink (or heat sink section) is associated with each module. For simplicity, this study considers air-cooled, parallel plates heat sinks under forced convection like those of Fig. 5. Nevertheless, the methodology is extensible to different configurations.

In Fig. 5, b, L, d, c, t, and n are width, length, base plate thickness, fin height, fin thickness, and channel width, respectively. For a given fan and heat sink dimensions, the operating volumetric flow rate $\dot{V}$ results from the intersection of the fan curve, available from the manufacturer, and the system (heat sink) curve, representing the ΔP vs $\dot{V}$ relationship. The pressure drop in the cooling system includes the pressure drop in the air duct connecting the fan to the heat sink, the pressure drop along the heat sink, as well that one associated with entry and exit effects.

A thermal equivalent network approach, [20], is used to represent the different heat transfer mechanisms (Fig. 5).

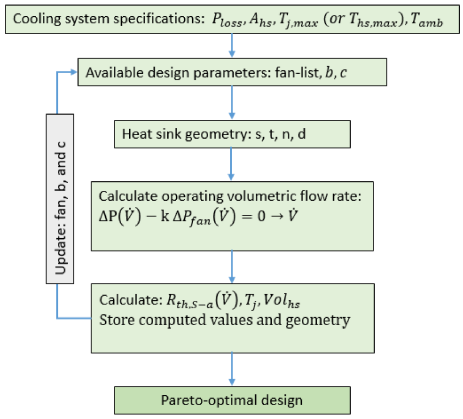


Fig. 6. Cooling system optimization algorithm.

The junction to case resistances, R_{jc}, and the case to sink resistance, R_{cs}, are taken as inputs from manufacturer data. The sink to air resistance, $R_{th,sa}$ is computed from the equivalent circuit shown on Fig. 5 (right). R_1 corresponds to a conduction resistance across the base, R_2 is a convection resistance between the air and the horizontal portion of the channel formed by the fins, and R_3 and R_4 are used to represent the heat transfer through the fins (a combination of conduction and convection). The conduction resistances are evaluated from $R_{cond} = d/(kA)$, where d represent the thickness of the layer where conduction is taking place, k the thermal conductivity of the solid material, and A the cross-sectional area perpendicular to the heat flux. The convective resistances, $R_{cnv} = 1/(hA)$ are evaluated with the convective heat transfer coefficient, h, which itself is obtained from Nusselt number correlations.

Given that the flow is externally driven, it is convenient to express the flow speed u in terms of the total volumetric flow rate, $u = \dot{V}/(nA)$, where, n, is to account for the n flow passages (formed by the fins). The correlations for friction factor and Nusselt number for forced and mixed convection and different flow regimes, are expressed in terms of the Reynolds number, $Re_{D_h} = (uD_h)/\nu$, where u represents the flow speed, ν the kinematic viscosity, and D_h the hydraulic diameter, given by, $D_h = (4A)/p$. A represents the channel cross sectional area and p its perimeter.

A. Laminar regime

When the flow is laminar, $Re_{D_h} < 2300$, we use, $f = C/Re_{D_h}$. C depends on the aspect ratio. For example, C=96, for $(c/s > 8)$. For the combined entry problem, in which velocity and thermal boundary layers develop simultaneously, we use,

$$Nu_{D_h} = \frac{3.657(\tanh(2.264Gz_{D_h}^{-1/3} + 1.7Gz_{D_h}^{-2/3}))^{-1}}{\tanh(2.432Pr^{1/6}Gz_{D_h}^{-1/6})} + \frac{(0.0499Gz_{D_h}^{-1})\tanh Gz_{D_h}^{-1}}{\tanh(2.432Pr^{1/6}Gz_{D_h}^{-1/6})} \quad (1)$$

Equation 1 is recommended by Baehr and Stephan for constant surface temperature, combined entry length, and fluids with $Pr \gtrsim 0.1$ with properties evaluated at mean film temperature. Gz_{D_h} represents the Grashof number.

B. Turbulent regime

In the turbulent regime, we employ Petukhov's correlation, $f = (0.790 \ln Re_{D_h} - 1.64)^{-2}$, which is recommended for $3000 \lesssim Re_{D_h} \lesssim 5 \times 10^6$.

For the Nusselt number, we rely on Gnielinski's correlation,

$$Nu_{D_h} = \frac{(f/8)(Re_{D_h} - 1000)Pr}{1 + 12.7(f/8)^{1/2}(Pr^{2/3} - 1)}, \quad (2)$$

which is recommended for $0.5 \lesssim Pr \lesssim 2000$ and $3000 \lesssim Re_{D_h} \lesssim 5 \times 10^6$.

C. Pressure drop

Once, the Darcy friction factor is obtained, according to the flow regime, the pressure drop experienced by the coolant as it flows through the passages can be obtained from,

$$\Delta p = \frac{1}{2}\rho u^2 \left[K_c + K_e + f\frac{L}{D_h}\right] \quad (3)$$

where, K_c and K_e are loss coefficients associated with contraction and expansion at the entrance and exit of the channels.

D. Heat sink thermal resistance

The thermal resistance of the finned heat sink illustrated in Fig. 5 can now be obtained, as the convective heat transfer coefficients can be obtained from the Nusselt number according to the flow regime (Eqs.1 or 2), as $h = (Nu_{D_h}\kappa_f)/D_h$, where κ_f represents the coolant thermal conductivity. Refer to [20], for a very similar and detailed approach.

The VPP framework cooling system optimization algorithm (Fig. 6) starts from knowledge of the device geometry, heat dissipation, and limiting temperatures. A design exploration covering different heat sink geometries (b, c, s, t, n, d) matched to multiple fans from a fan database is conducted to determine, for each case, the operating flow rate, pressure drops, heat transfer coefficients, thermal resistances, heat sink volume, and junction temperatures. Once these metrics are available to the GA algorithm, the fan selection takes place around an optimal power density of the cell. CFD models can be used to refine the resistance of a specific design and explore local features of the identified solution (Fig. 7).

V. Transformer Design

A genetic (evolution based) algorithm, NSGA-II, is used to explore the transformer design space. Details of the transformer genetic parameters are given in Table III & I. The parameter distribution of the final population is depicted in Fig. 8. The criteria will be to minimize Mass(M), Loss(P_t) and Volume(Vol_t) as shown in the fitness function Eq.(4) where C is the averaged sum of the genes.

$$\Theta = \begin{cases} \varepsilon(\tilde{c} - 1)[1\ 1\ 1]^T & , \tilde{c} < 1 \\ \left[\frac{1}{M}\ \frac{1}{P_t}\ \frac{1}{Vol_t}\right] & , \tilde{c} < 1 \end{cases} \quad (4)$$

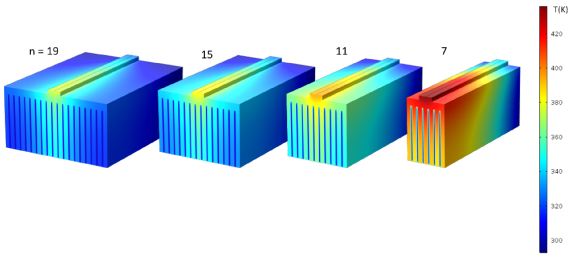


Fig. 7. CFD comparison of heat sinks with equal inlet flow velocity and module heat dissipation to explore the effect of heat diffusion into lateral fins.

TABLE III
DESIGN CONSTRAINTS FOR GA

Design Constraints	
Cell Para	***Value***
DC Voltage Primary	800V
DC Voltage Primary	800V
Cell Power level	75KVA
AC Voltage AFE	690 V
Tmax(SST)	180°C
Num of generation	70
Num of Population	3000
Modulation index	0.86
No. of primary coils in series	1
No. of secondary coils in series	1
No. of primary coils in parallel	2
No. of secondary coils in parallel	2
Max. SST power loss(KW)	4
Max. Device power loss(KW)	1
Min. primary to secondary turns ratio(Rpsmn)	0.95
Max. primary to secondary turns ratio(Rpsmx)	1.05
Max. Regulation	0.05

The approach relies upon a Magnetic Equivalent Circuit (MEC) Model, including high-frequency leakage and Thermal Equivalent Circuit (TEC) design. Core loss and winding losses must be considered in an Transformer design for a medium voltage and high current will account for the major loss contribution. High-frequency effects also need to be considered [21]. The distribution of losses are listed as and explained in detail for an inductor in [11].

The high frequency transformer losses that are being considered are listed as follows:

1) Core Loss [22]–[24]

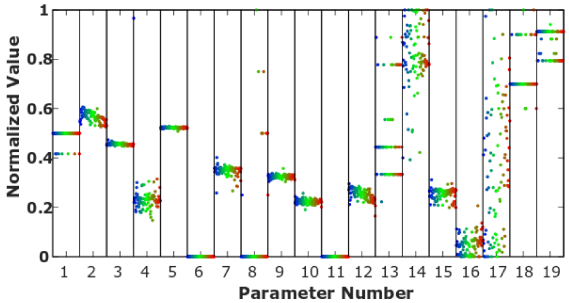


Fig. 8. Gene Parameter

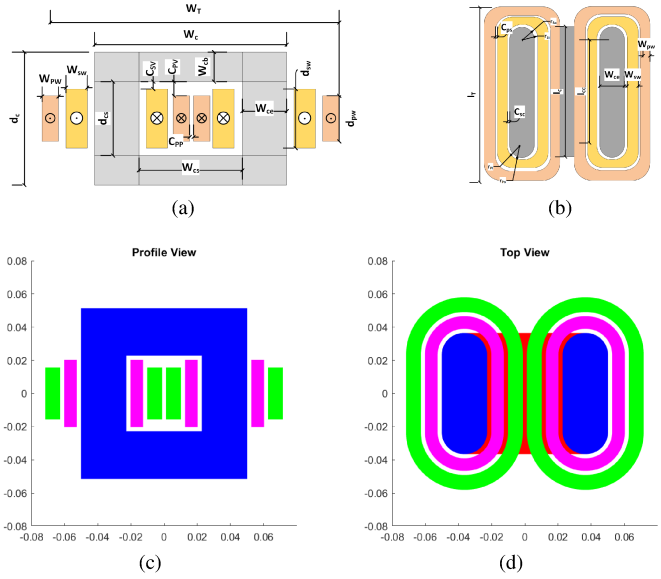


Fig. 9. (a) & (c) Profile view of the transformer.(b) & (d) are Top view of the Transformer. (c) & (d) are the result of running the VPP of the transformer [After [22]].

   a) Eddy Current losses
   b) Hysteresis Current losses
2) DC Conductor loss
3) Thermal loss
4) AC conductor Loss
   a) Skin effect in strip conductors [25]
   b) Proximity effect loss [26]

VI. Optimization Results

In this paper, the technique is set forward for a high-frequency core-type transformer within the setting of an separating DC-DC converter. The chosen core-type transformer geometry at the side the the outline of coil cross-section are shown in Fig. 9. The Fig. 9a & Fig. 9b show the construction and breakdown of the transformer for the MEC and TEC analysis, respectively. The Figs. 9c & 9d are the results of VPP, and show the profile and top views, respectively. The detailed analysis of the SST using GA is also explained in [14], but design variables such as switching frequency, devices, and heat sink design were out of the scope.

The optimization is conducted basing the contemplation set forward by the past segments, one the most consideration thats center within the optimization is power density, for this to be feasible, the power devices within the converter should operate at Tjmax. For this to happen, This heat sink should be design sufficiently to expel the generated heat. This successfully points of interest or limits the switching frequency, which impacts the transformer leakage, thus affecting the over all power converter volume, losses, etc. The Fig. 10a illustrates the combined losses of the transformer and the device losses as defined the previous sections. The Pareto optimal front of losses with respect to design numbers are shown here. The

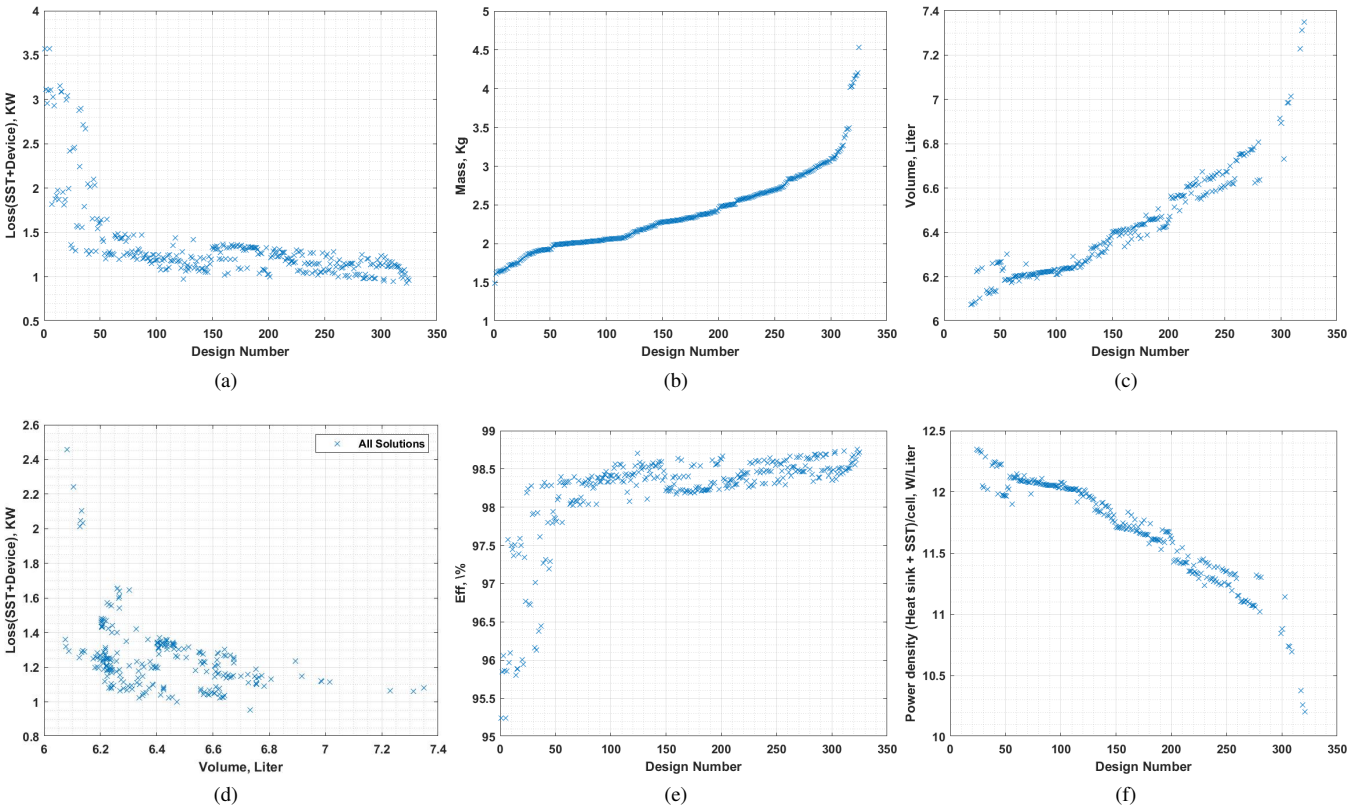


Fig. 10. (a) Pareto front of Device + SST losses, (b) Pareto Front of SST mass, (c) Pareto Front of Volume of SST+ Volume of heat sink x 6(1 heat sink/2 switches),(d) Pareto Optimal Front Loss VS Volume shown in (a) & (c), (e) Efficiency of the cell & (f) Power Density (Heat sink*6 + SST)

losses ranges from 3.6 kW to 900 W. The losses reduce as we move up in volume and mass of the transformer. Fig. 10b and the Fig. 10c shows that the mass of the SST falls between 1.5 kg to 4.6 kg and the volume starts from 6 liters to 7.4 liters. In the optimization scheme, the volume is give key importance. Here, volume of the heat sink * 6 + volume of the SST are considered, this enables the design to ensure global optima for multi-object optimization and consider various trade-offs between device losses and the transformer loss, which effect the power density the most in this topology. Figs. 10a & 10c plots together gives the Pareto optimal front as shown in Fig. 10d that clearly illustrates the trade-off between volume of the dependent variables and the over loss of the converter being considered. In the interest of further analysis, a random design can be chosen from the given 330 designs and detailed meta-model can be obtained as shown in [5] for a MMC design. The efficiency is very important aspect of DAB-based power converters [27], Fig. 10e shows the efficiency ranges between 95% to 98.8% is achievable. To calculate the overall power density of the converter analysis the mechanical cabinets, insulation, dielectric standoff, etc., should be considered which is beyond the scope of this paper. Therefore, a preliminary power density analysis can be done on the SST and heat sink designs for this power converter as how in Fig. 10f. 10 W/Liter to 12.5 W/Liter can be achieved for the heat sink and the SST.

VII. Conclusion

The optimization results presented in this paper shows demonstrates a detailed primary study conducted to maybe say, to explore the trade-offs between power density and efficiency in the design space for DABs. The details like losses of the power devices, heat sink design, and the transformer design and its effects on power density are also shown in this paper. This study allows designer to understand trends, and understand the root-cause of the trends, and trace back impact of additional design variables or constraints on the system. Furthermore, the design can align the trade-space with market objects to help determine which design to bring to market. As we are moving closer every day to fully functioning EV chargers, to attain a feasible, reliable, cost-effective, and power density product using the latest technology will be a key aspect to watch. This process can be used to attain a feasible, reliable, cost-efficient, and power density design to aid in bring the next generation power conversion products to market, such as multi-eV fast charging stations or electrified shipboard application. The expansion of the all the other components and the allocations around the power devices for the converter will certainly reduce the power density of the converter. This study gives the hypothetical semi-physics based approach to scaling and building MV and HV power converters leveraging the most recent accessible power power modules innovation.

Within the future studies, thorough investigation and test validations of these converters must be carried forward. Due to the page restrain of this paper, clarification and points of interest of the total optimization isn't explained, instead this paper focus on outlining the prerequisites and the preliminary analysis to understand the by and large impacts of the device choices, transformer and the heat sink design.

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