Application of An Active Gate Driver for Paralleling Operation of Si IGBT and SiC MOSFET

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***Abstract*—Wide band gap (WBG) devices feature high switching frequency operation and low switching loss. They have been widely adopted in tremendous applications. Nevertheless, the manufacture cost for SiC MOSFET greater than that of the Si IGBT. To achieve a trade off between cost and efficiency, the hybrid switch, which includes the paralleling operation of Si IGBT and SiC MOSFET, is proposed. In this article, an active gate driver is used for the hybrid switch to optimize both the switching and thermal performances. The turn-on and turn-off delays between two individual switches are controlled to minimize the switching loss of traditional Si IGBT. In this way, a higher switching frequency operation can be achieved for the hybrid switch to improve the converter power density. On the other hand, the gate source voltages are adjusted to achieve an optimized thermal performance between two individual switches, which can improve the reliability of the hybrid switch. The proposed active gate driver for hybrid switch is validated with a 2 kW Boost converter.**

Keywords—Wide band gap, SiC MOSFET, Si IGBT, thermal performance optimization

I. Introduction

Wide band gap (WBG) devices have gained much popularity due to their high temperature operation and low switching loss characteristics [1]-[4]. The downside for the WBG devices based power converters is that a high system cost is required. Due to the manufacture difference, the price for conventional Si IGBT per ampere is five times cheaper than the SiC MOSFET [5]. Moreover, the conduction loss for high current rating Si IGBT is small. The main disadvantage for Si IGBT is the slow switching speed and high switching loss. Innovatively, by combining a conventional Si IGBT with a SiC MOSFET, a trade off between the cost and efficiency is achieved.

The optimized current ratio between Si IGBT and SiC MOSFTE is discussed in [6] to optimize the die size and relax the thermal management system. The zero-voltage switching (ZVS) control strategy is proposed for the hybrid switch to reduce the switching loss and increase the switching frequency [7]. Different gate control patterns for hybrid switch are investigated in [8], a thermal balance control mode is proposed to improve the reliability of the hybrid switch, where the turn-on and turn-off delays are manipulated. The applications of hybrid switch in inverters are also reported in [9]-[12]. The power loss model for the hybrid switch is discussed in [13]. In the previous literature, the power loss model is only developed based on the same and constant gate voltage for hybrid switch. In this article, the variable gate volatge solution is developed and the corresponding power loss model is modified by taking the gate volatge into consideration.

However, in the existing literature, only the turn-on and turn-off delays can be controlled to optimize the performance of the hybrid switch. Although the best efficiency operation condition can be found, the thermal performance of the hybrid switch is not optimized, which is important for the reliability operation. Therefore, in this article, an active gate driving solution is proposed and adopted for the hybrid switch to optimize both the efficiency and thermal performance. From the experimental results, it can be found out that the thermal balance between two individual devices can be achieved by using the proposed active gate driver.

II. Introduction of Hybrid Switch and Active Gate Driver

Hybrid switch, which composes of a Si IGBT (IGW40T120 1200 V/40A) and a SiC MOSFET (C2M0160120D 1200V/12.5A) in paralleling operation. The circuit diagram for the hybrid switch is shown in Fig. 1. Cost comparisons among different solutions, all Si IGBT, all SiC MOSFET, and hybrid switch are demonstrated in Fig. 2. The large switching loss (turn-on and turn-off losses) of Si IGBT can be reduced by designing appropriate gating signals for two devices. Based on the turn-on delay and turn-off delay between Si IGBT and SiC MOSFET, there exist four different control schemes for hybrid switch. Among these different control schemes, to minimize the switching loss and improve the switching frequency capability, the SiC MOSFET should be turns-on first to provide zero-voltage turn-on for Si IGBT to reduce the turn-on switching loss. Due to the fast switching speed of SiC MOSFET, the turn-on delay time is close to zero. In addition, the SiC MOSFET should be turned off later than the Si IGBT so that the zero-voltage turn-off can be achieved for Si IGBT. Compared with the almost zero turn-on delay time, a large turn-off delay time is required to reduce the turn-off switching

loss of Si IGBT due to its long tail current. Furthermore, a thermal balance operation between two individual devices is also of great importance to improve the system reliability.

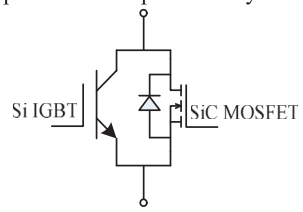


Fig. 1. Circuit symbol of hybrid switch

Traditionally, only the turn-on delay and turn-off delay of the hybrid switch can be adjusted. However, for the hybrid switch, the switching loss, which can determine the maximum switching frequency, should be kept as small as possible. The turn-on delay and turn-off delay should be determined to minimize the switching loss and improve the maximum switching frequency capability for hybrid switch. Therefore, more control freedoms should be introduced to achieve the thermal balance operation between Si IGBT and SiC MOSFET. In this article, another two control freedoms, Si IGBT gate voltage and SiC MOSFET gate volatge, are introduced. Fig. 2 shows the variable gate volatge control circuit. Based on the control signals, the gate voltage can be adjusted from 15 V to 25 V. The relationship between the gate voltage and control signals are shown in Equation (1).

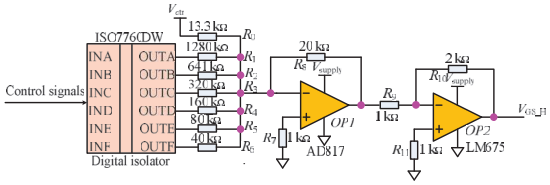


Fig. 2. Circuit implementation of variable gate volatge control.

$$V_{\mathrm{GS\_H}} = V_{\mathrm{ctr}}\left(\frac{1}{R_0} + \frac{\mathrm{INA}}{R_1} + \frac{\mathrm{INB}}{R_2} \cdots \frac{\mathrm{INF}}{R_6}\right) R_8 \frac{R_{10}}{R_9} \tag{1}$$

The system control diagram is shown in Fig. 3. Based on the circuit operating conditions and the power loss model discussed in next Section, the required gate voltages or control signals can be calculated based on the developed power loss model in next Section. A look-up table can be generated to provide the control signals based on the circuit operating conditions.

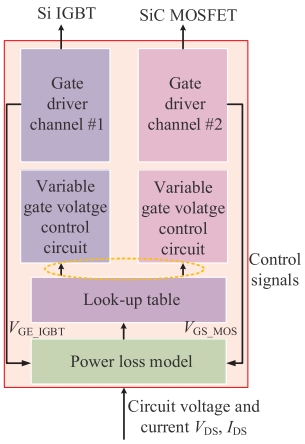


Fig. 3. System control block diagram.

III. Power Loss ModelFor Hybrid Switch

To achieve the thermal balance operation of the hybrid switch, the power loss and thermal models for the hybrid switch should be derived. Fig. 4 shows the typical experiment waveform for the hybrid switch with turn-on and turn-off delays. $V_{\mathrm{GS\_MOS}}$ and $V_{\mathrm{GE\_IGBT}}$ are the gate voltage for the SiC MOSFET and Si IGBT, respectively; V_{DS} is the voltage across the hybrid switch, i_{IGBT} and i_{MOSFET} are the device current for Si IGBT and SiC MOSFET, respectively. Clearly, there are five stages during one switching cycle for the hybrid switch, and the power loss calculation for each stage is discussed below.

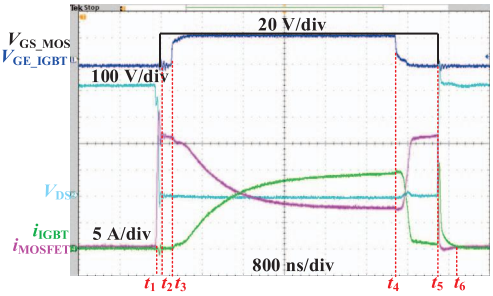


Fig. 4. Typical experiment waveform for the hybrid switch with turn-on and turn-off delays.

Fig. 5 shows the simplified steady state operation circuit model of the hybrid switch. Compared with Si IGBT, there is no knee voltage (0.5 V-1.0 V) for the SiC MOSFET. Thus, the IGBT is conducting when the voltage across the hybrid switch is greater than the IGBT knee voltage, which can be expressed as follows

$$I = I_{\mathrm{MOS}} = \frac{V_{\mathrm{knee}}}{R_{\mathrm{ds}}} \tag{2}$$

where V_{knee} is the kneed voltage of IGBT, and R_{ds} is the on-state resistance of the SiC MOSFET.

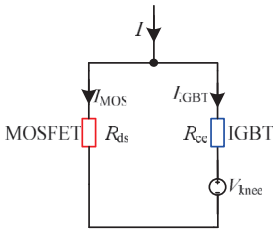


Fig. 5. Equivalent circuit for the hybrid switch in steady state.

Stage [t_1, t_2]: in this stage, the SiC MOSFET is undergoing hard switching, and the hard turn-on loss can be approximated either by using double pulse test results or data provided by the manufacture datasheet. An example is demonstrated here to derive the turn-on loss model of the SiC MOSFET C2M0160120D. The SPICE model provided by the manufacture is used to obtain the turn-on loss model under different conditions. For high accuracy modelling results, the double pulse test results are preferred.

The switch turn-on loss can be modelled as functions of device drain to source current I_{DS}, drain to source voltage V_{DS}, gate source voltage V_{GS}, and junction temperature T_J. The general modelling idea is to derive the relationship between the switching loss and device drain to source current I_{DS}. Then, other factors are normalized and added to modify the basic modelling between the switching loss and drain to source current I_{DS}. The turn-on loss is selected as an example to demonstrate here.

***Step 1*:** Turn-on loss and the device drain to source current.

Fig. 6 shows the curve fitting result for the turn-on loss with different device current. Please note that the simulation data are obtained when V_{DS}=600 V, V_{GS}=20 V, R_G=10 Ω, T_J=25 ºC. Equation (3) is the curve fitting results.

$$E_{on\_MOS}=0.3392\times I_{DS}^2+2.7928I_{DS}+11.92 \quad (3)$$

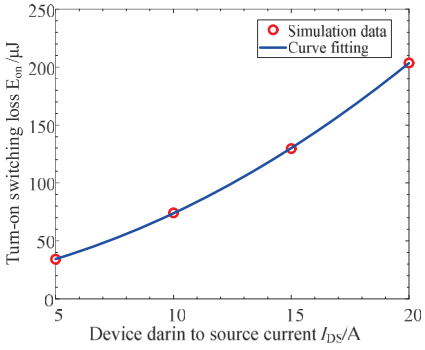


Fig. 6. Modelling of device turn-on switching loss and device drain to source current.

***Step 2*:** Turn-on loss and the device drain to source voltage

With the variation of drain to source voltage, the turn-on switching loss is also varied. The simulation data are obtained when I_{DS}=10 A, V_{GS}=20 V, R_G=10 Ω, T_J=25 ºC and the results are shown in Fig. 7. To introduce the drain to source voltage into the turn-on loss model, the simulation data is normalized by setting the base value when V_{DS}=600 V, I_{DS}=10 A, V_{GS}=20 V, R_G=10 Ω, T_J=25 ºC. The modeling result for the normalized turn-on switching loss is shown in Fig. 8 and Equation (4).

$$E_{on\_MOS}=5.9131\times10^{-7}\times V_{DS}^2+0.0013371V_{DS}-0.017457 \quad (4)$$

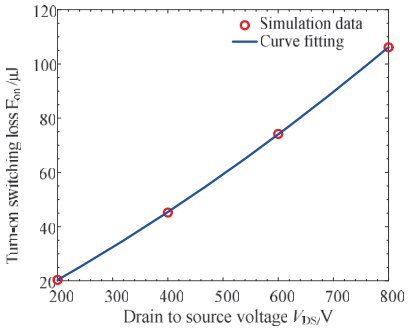


Fig. 7. Modelling of device turn-on switching loss and device drain to source voltage.

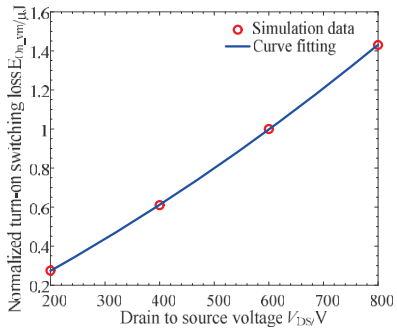


Fig. 8. Modelling of device normalized turn-on switching loss and device drain to source voltage.

By taking the drain to source voltage into consideration, the device turn-on switching loss can be modelled as

$$E_{on}(I_{DS},V_{DS})=E_{on\_vm}\times E_{on}(I_{DS}) \quad (5)$$

***Step 3*:** Turn-on loss and the device junction temperature

The device junction temperature will also affect the switching loss. According to the datasheet, it can be seen that with different junction temperatures, there is almost no variations on the device turn-on switching loss. Therefore, the influence of the junction temperature can be ignored for the SiC MOSFET used in this paper.

***Step 4*:** Turn-on loss and the device gate source voltage

In the proposed approach, the gate voltage can be adjusted in the range of 15 V to 25 V. Therefore, the device turn-on loss under different gate voltages are investigated to introduce the gate source voltage into the loss model. Fig. 9 and Equation (6) show the modelling result of the device gate source voltage and turn-on switching loss. Please note that the simulation data is normalized by setting the base value when V_{DS}=600 V, I_{DS}=10 A, V_{GS}=20 V, R_G=10 Ω, T_J=25 ºC.

$$E_{on\_MOS}=0.0058556\times V_{GS}^2-0.29822V_{GS}+4.6218 \quad (6)$$

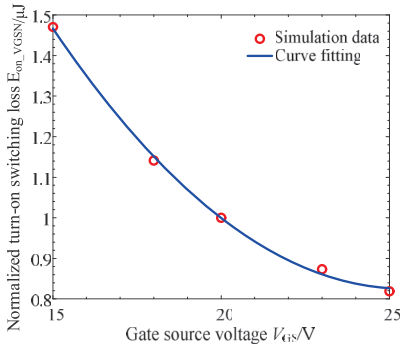


Fig. 9. Modelling of device turn-on switching loss and gate source voltage.

Finally, by combining all the factors into considerations, the turn-on switching loss for SiC MOSFET is modelled as follows.

$$E_{on}(I_{DS},V_{DS},T_J,V_{GS}) = E_{on\_VDSN} \times E_{on}(I_{DS}) \times E_{on\_VGSN} \quad (7)$$

Stage [t_2, t_3]: in this stage, due to the turn-on delay, the Si IGBT is still not conducting, all the current will flow through the SiC MOSFET and conduction loss will be generated. The corresponding conduction loss can be expressed as below.

$$E_{con\_MOS1} = I^2 R_{ds}(t_3 - t_2) \quad (8)$$

Due to the fast switching speed of SiC MOSFET, the duration of this stage can be approximated as the turn-on delay. For higher accuracy, the turn-on time of the SiC MOSFET under different circuit conditions can be obtained and modeled by using SPICE model. Please note that the device on-state resistance will vary with its junction temperature and gate source volatge. Then, the device on-state resistance is modelled by taking device current, gate source volatge and junction temperature into considerations.

***Step 1*:** On-state resistance and the device drain to source current

Similarly, Fig. 10 shows the device on-state resistance with different device current and their relationship can be modelled by using curve fitting result.

$$R_{ds(on)}=0.00015517 \times I_{DS}^2 + 0.00083918 I_{DS}+0.16067 \quad (9)$$

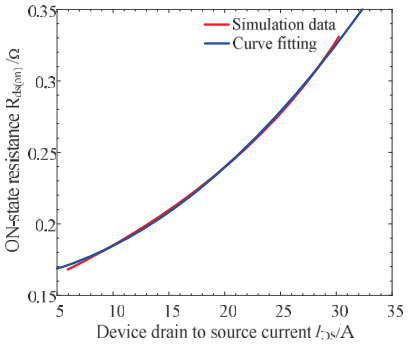


Fig. 10. Modelling of device on-state resistance and device drain-to-source current.

***Step 2*:** On-state resistance and the junction temperature

The normalized on-state resistance is used to introduce the junction temperature influence in the model between on-state resistance and device current. Fig. 11 and Equation (10) show the modelling results.

$$R_{ds(on)}=2.2462 \times 10^{-5} \times T_J^2 + 0.00097996 T_J + 0.16067 \quad (10)$$

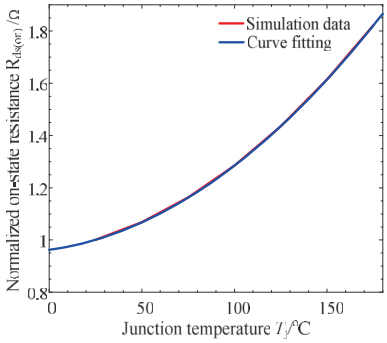


Fig. 11. Modelling of device on-state resistance and device drain-to-source current.

***Step 3*:** On-state resistance and the gate source voltage

Fig. 12 shows the normalized on-state resistance with different gate voltages. It can be seen that with the increase of gate voltage, the on-state resistance for the SiC MOSFET is decreased.

$$R_{ds(on)}= -9.3292 \times 10^{-5} \times V_{GS}^3 + 0.0065979 \times V_{GS}^2 \quad (11)$$
$$-0.15972 \times V_{GS} + 2.2251$$

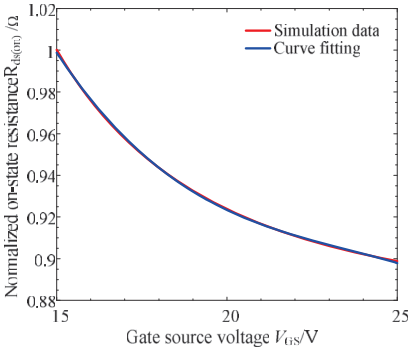


Fig. 12. Modelling of device on-state resistance and device gate source voltage.

Stage [t_3, t_4]: in this stage, the current flows through both the SiC MOSFET and Si IGBT, and the equivalent circuit is shown in Fig. 4. According to Fig. 4, the current flows through each device can be derived as

$$I_{MOS} = \frac{R_{ce}}{R_{ce}+R_{ds}} I + \frac{V_{knee}}{R_{ce}+R_{ds}} \quad (12)$$

$$I_{IGBT} = \frac{R_{ds}}{R_{ce}+R_{ds}} I - \frac{V_{knee}}{R_{ce}+R_{ds}} \quad (13)$$

Then, the conduction loss of two devices in this stage can be derived as

$$E_{\text{con\_MOS2}} = \begin{cases} I^2 R_{\text{ds}}(t_4\text{-}t_3), I \le I_{\text{knee}} \\ (\dfrac{R_{\text{ce}}}{R_{\text{ce}}+R_{\text{ds}}} I + \dfrac{V_{\text{knee}}}{R_{\text{ce}}+R_{\text{ds}}})^2 \\ \times R_{\text{ds}}(t_4\text{-}t_3), I > I_{\text{knee}} \end{cases} \quad (14)$$

$$E_{\text{con\_IGBT}} = \begin{cases} 0, I \le I_{\text{knee}} \\ ((\dfrac{R_{\text{ds}}}{R_{\text{ce}}+R_{\text{ds}}} I - \dfrac{V_{\text{knee}}}{R_{\text{ce}}+R_{\text{ds}}}) R_{\text{ds}} + V_{\text{knee}}) \\ \times (\dfrac{R_{\text{ds}}}{R_{\text{ce}}+R_{\text{ds}}} I - \dfrac{V_{\text{knee}}}{R_{\text{ce}}+R_{\text{ds}}}) \\ \times (t_4\text{-}t_3), I > I_{\text{knee}} \end{cases} \quad (15)$$

Stage [t_4, t_5]: in this stage, all the load current will flow through the SiC MOSFET due to the turn-on delay time that adopted to ensure zero-voltage switching operation of Si IGBT. The additional conduction loss for SiC MOSFET in this stage can be expressed as

$$E_{\text{con\_MOS3}} = I^2 R_{\text{ds}}(t_5 - t_4) \quad (16)$$

The duration of this stage is also the turn-off delay time $T_{\text{off\_delay}}$ of the hybrid switch.

Stage [t_5, t_6]: in this stage, the SiC MOSFET will undergoing a hard switching turn-off. Similarly, the turn-off loss model can be either derived by using a double pulse test results or data provided by manufacturer datasheet.

In addition, the Si IGBT still has turn-off loss due to the minority carrier recombination during the gate turn-off delay time [11]. The same procedures for the SiC MOSFET turn-on loss modelling are performed.

The total power loss for the SiC MOSFET and Si IGBT can be expressed as

$$P_{\text{loss\_MOS}} = E_{\text{on\_MOS}} + E_{\text{con\_MOS1}} + E_{\text{con\_MOS2}} + E_{\text{con\_MOS3}} + E_{\text{off\_MOS}} \quad (17)$$

$$P_{\text{loss\_IGBT}} = E_{\text{con\_IGBT}} + E_{\text{off\_IGBT}} \quad (18)$$

The junction temperature for the device can be expressed as

$$T_j = T_c + R_{\theta jc} \times P_{\text{loss}} \quad (19)$$

where T_j is the junction temperature, T_c is the case temperature, $R_{\theta jc}$ is the thermal resistance, and P_{loss} is the power loss consumed by the device.

Based on the power loss model and the power device thermal model as shown in Equation (19), the junction temperature for Si IGBT and SiC MOSFET in a hybrid switch can be derived as

$$T_{\text{j\_IGBT}} = T_{\text{c\_IGBT}} + R_{\theta\text{jc\_IGBT}} \times P_{\text{loss\_IGBT}} \quad (20)$$

$$T_{\text{j\_MOS}} = T_{\text{c\_MOS}} + R_{\theta\text{jc\_MOS}} \times P_{\text{loss\_MOS}} \quad (21)$$

where $T_{\text{c\_IGBT}}$ and $T_{\text{c\_MOS}}$ are the case temperature for the Si IGBT and SiC MOSFET, $R_{\theta\text{jc\_IGBT}}$ and $R_{\theta\text{jc\_MOS}}$ are the thermal resistance for Si IGBT and SiC MOSFET, $P_{\text{loss\_IGBT}}$ and $P_{\text{loss\_MOS}}$ are the power loss consumption for the Si IGBT and SiC MOSFET. By assuming an ideal cooling condition, the case temperatures for two devices are identic. In addition, if two dies are placed on the same substrate, same case temperature can be expected.

Therefore, in order to achieve a thermal balance operation, the following equation should be satisfied.

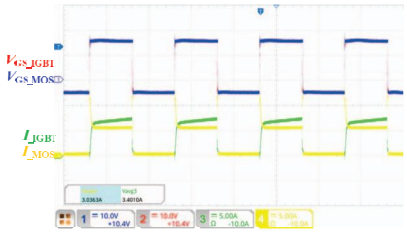
$$R_{\theta\text{jc\_IGBT}} \times P_{\text{loss\_IGBT}} = R_{\theta\text{jc\_MOS}} \times P_{\text{loss\_MOS}} \quad (22)$$

Thus, to achieve thermal balance operation for the hybrid switch, an optimal power loss ratio for the SiC MOSFET and Si IGBT should be achieved. For the proposed solution, the required gate voltages to achieve thermal balance operation under certain operating conditions can be calculated based on the power loss and thermal models. The look-up table method is used to generate the required signals.

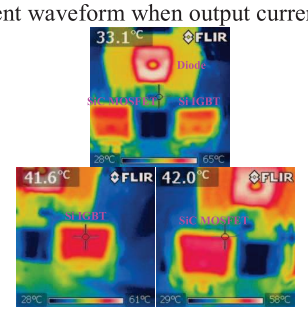
IV. Experiment Results

To investigate the thermal performance of hybrid switch, a 2 kW continuous boost converter is constructed to perform the test. The testing conditions are: input voltage: 100 V; switching frequency: 20 kHz; output voltage: 200 V. The turn-on delay of 0.3 μs and turn-off delay of 2.5 μs are adopted to achieve high efficiency operation of the hybrid switch. In this work, we assumed that the junction to case thermal resistances for two devices are same, so the case temperature is used to estimate the junction temperature. In the future, the thermal resistance difference between Si IGBT and SiC MOSFET should also be taken into consideration.

When the output current equals 5 A, the thermal balance operation can be achieved for the hybrid switch as shown in Fig. 13. As can be seen from Fig. 13, the conduction loss for IGBT is higher than SiC MOSFET, while there is almost no switching loss for IGBT. Thus, the total power dissipations for Si IGBT and SiC MOSFET are same.



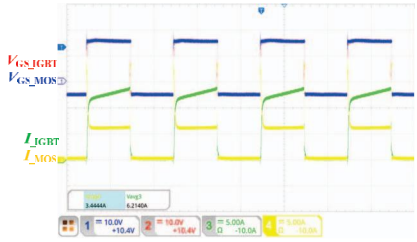
(a) Experiment waveform when output current equals 5 A



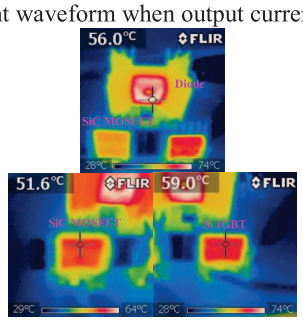
(b) Thermal performance when output current equals 5 A

Fig. 13. Experiment waveform when output current equals 5 A.

With the increase of output current, the conduction loss for IGBT is dominating the power loss dissipation, so the temperature for IGBT is greater than MOSFET as shown in Fig. 14, the temperature difference is around 7 °C.



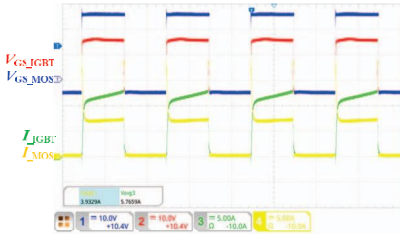
(a) Experiment waveform when output current equals 10 A



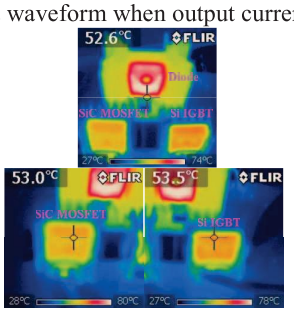
(b) Thermal performance when output current equals 10 A

Fig. 14. Experiment waveform when output current equals 10 A.

To achieve thermal balance operation of the hybrid switch, the gate voltage for SiC MOSFET is increased to dynamically adjust the current distribution. With the increase of gate voltage, more current will flow through the SiC MOSFET to reduce the conduction loss of Si IGBT. Finally, the thermal balance operation as shown in Fig. 15 is achieved. The average current for SiC MOSFET increases from 3.44 A to 3.93 A.



(a) Experiment waveform when output current equals 10 A



(b) Thermal performance when output current equals 10 A

Fig. 15. Experiment waveform when output current equals 10 A with the developed AGD.

V. Conclusions and Future Work

In this article, the hybrid switch performance is investigated with the proposed active gate driver. The optimized turn-on and turn-off delays for the hybrid switch is experimentally found. The ZVS operation for the Si IGBT is desired to maximize the converter efficiency. In addition, to achieve thermal balance operation of the hybrid switch, the gate source voltage is dynamically adjusted to modify the current ratio, which can be used in the hybrid switch application to improve the system reliability.

Acknowledgment

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