Four Control Freedoms AGD for Hybrid SiC MOSFET and Si IGBT Application

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***Abstract*—Silicon carbide (SiC) MOSFET features low switching loss and it is advantageous in high switching frequency application, but the manufacture per Ampere cost is approximately five times higher than the silicon (Si) IGBT. Therefore, by paralleling Si IGBT and SiC MOSFET together, a trade-off between cost and loss is achieved. In this paper, a four control freedoms active gate driver (AGD) including turn-on delay, turn-off delay, and two independent gate voltages, is proposed to optimize the performance of the paralleled device. By adjusting these four control freedoms, optimal operation for paralleled device can be obtained. Moreover, the proposed AGD can dynamically adjust the current ratio between two paralleled devices, which can help achieve thermal balance between two devices and improve system reliability. Double pulse test (DPT) experimental results are presented and analyzed to validate the effectiveness of the proposed AGD for paralleled Si IGBT and SiC MOSFET application.**

Keywords—SiC MOSFET, Si IGBT, hybrid switch, active gate driver.

I. Introduction

Wide band gap devices are widely adopted in tremendous industrial applications due to their outstanding characteristics of high frequency and high efficiency operation [1]–[3]. Silicon carbide (SiC) metal oxide semiconductor field effect transistor (MOSFET) is considered as an excellent substitution for conventional silicon (Si) insulated gate bipolar transistor (IGBT) in high voltage and high power applications, like traction inverters [4], solid state transformers [5], renewable energy systems [6], and future data center power supplies [7]. Compared with Si IGBT, SiC MOSFET has faster switching speed and lower switching losses, which can increase the converter power density and efficiency. The high performance of SiC MOSFET can reduce the size of both heatsink and passive elements. It was experimentally found out that for a 3 kW prototype, the system efficiency improvement is more than 3% for the SiC MOSFET when compared with the Si IGBT [8]. Nevertheless, the manufacture cost per ampere for SiC MOSFET is five times higher than the Si IGBT [9].

In order to reduce the system cost and achieve a trade-off between the efficiency and cost, the hybrid switch concept is proposed in [10]. The maximum operating switching frequency is increased when compared with traditional Si IGBT. To reduce the large switching loss of Si IGBT, different gate control patterns for hybrid switch were investigated in [11]. It was found out that the Si IGBT should turn-off firstly to reduce its large switching loss caused by long tail turn-off current. In this way, the zero voltage turn-off for Si IGBT can be achieved. A thermal balance control mode was also proposed for the hybrid switch to improve the system reliability, where the turn-on and turn-off delays are manipulated to adjust the thermal performance of hybrid switch. The optimized current ratio between Si IGBT and SiC MOSFET was investigated in [12] to optimize the die size and relax the thermal management system. Experimental characterizations on a hybrid switch were obtained in [13], which demonstrated improvements in terms of loss reduction, short circuit capability, and cost reduction. Comparative studies of two hybrid switch concepts were presented in [14] from the switching characteristics, operational principles, and applications perspectives. The practical design considerations for the hybrid switch were discussed from the interconnect parasitic, cost, and current ratio optimization perspectives [15]. The power loss model and size reduction algorithm were developed for hybrid switch [16]. The hybrid switches were implemented in different circuit topologies, including boost converter, active neutral point clamping inverter and three-level rectifier.

To further optimize the performance of paralleled device, in this paper, active gate driver (AGD) with four control freedoms: turn-on and turn-off delays, two independent gate voltages, is proposed to optimize the performance of the hybrid switch. In particular, the proposed method can dynamically adjust the current ratio between two devices. The benefits of the proposed method are: 1) switching loss optimization; 2) capability of adjusting current ratio dynamically; 3) achieve thermal balance and improve reliability.

The rest of this paper is organized as follows. Section II presents a brief introduction of hybrid switch. The operational principles and key design considerations for the active gate driver with four control freedoms are discussed in Section III. In Section IV, experiment results from double pulse test (DPT) are presented and analyzed to verify the functionality of the proposed idea.

II. Introduction of Hybrid Switch

Paralleled operation of SiC MOSFET and Si IGBT is also known as hybrid switch. The main purpose of hybrid switch is to achieve trade-off between loss and cost. A 1200–V 40–A Si IGBT (IGW40T120) and a 1200–V 12.5–A SiC MOSFET (C2M0160120D) are parallel connected to construct the hybrid switch [11]. To have the same current capability, a 40-A SiC MOSFET (C2M0040120D) can be selected. Fig. 1 shows the circuit symbol of hybrid switch, which composed of a SiC MOSFET and Si IGBT.

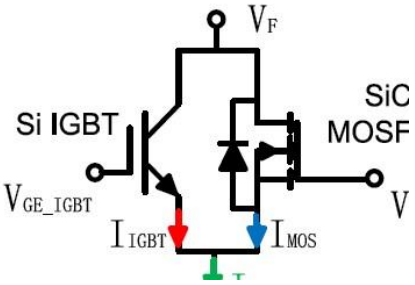


Fig. 1. Circuit symbol of hybrid switch.

Cost comparisons among different solutions are shown in Fig. 2 based on the unit price from Digikey. It can be seen that compared with SiC solution, the hybrid switch can achieve almost half of the cost reduction. The large switching loss (turn-on and turn-off losses) of Si IGBT can be reduced by designing appropriate gating signals for two devices. Generally, there exist four gate control pattens as shown in Fig. 3 for hybrid switch. Clearly, for gate patten 1, the zero-voltage turn-on switching and zero-voltage turn-off switching for IGBT can be achieved, which is preferred for the switching loss reduction of hybrid switch. Therefore, for hybrid switch, the turn-on delay and turn-off delay should be carefully designed to reduce switching loss. In addition, the current distribution and thermal balance between two devices also of great importance to improve the reliability of hybrid switch.

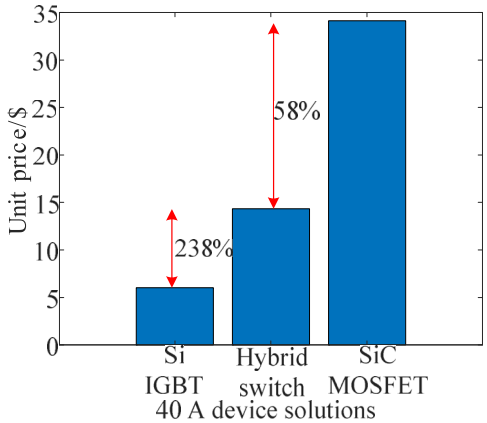


Fig. 2. Cost comparisons among different solutions.

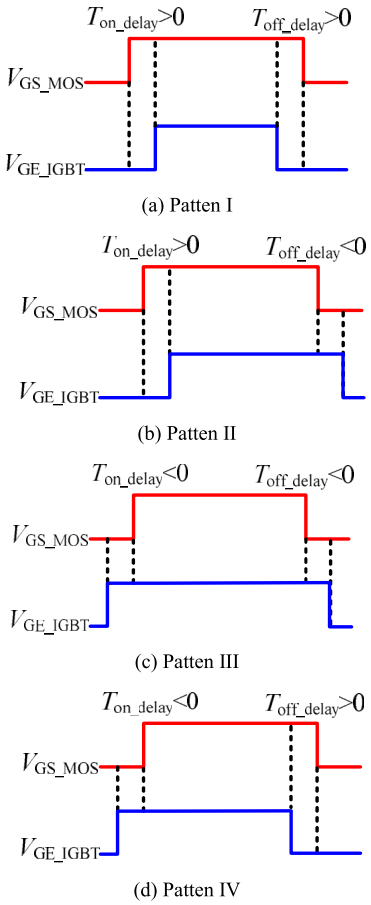


Fig. 3. Gate control pattens for hybrid switch.

To achieve the thermal balance operation of the hybrid switch, the power loss and thermal models for the hybrid switch should be derived. In addition, more control freedoms are preferred to achieve trade-off between switching loss, conduction loss, and circuit EMI performance. In the existing literature, only the hybrid switch turn-on delay and turn-off delay can be controlled, which limits the optimization of hybrid switch. Thus, in this article, a gate driver with four control freedoms is introduced to have more control freedoms to optimize the system. Fig. 4 shows the typical experiment waveform for the hybrid switch with turn-on and turn-off delays. V_{GS_MOS} and V_{GE_IGBT} are the gate voltage for the SiC MOSFET and Si IGBT, respectively; V_{DS} is the voltage across the hybrid switch, i_{IGBT} and i_{MOSFET} are the device current for Si IGBT and SiC MOSFET, respectively. Clearly, since the SiC MOSFET turns on earlier than the Si IGBT, the voltage across the hybrid switch already decreases to zero before the Si IGBT is turning on and the zero-voltage turn-on operation is achieved. During the turn-off process, the Si IGBT turns off first, while the SiC MOSFET is still in ON state, the voltage across the hybrid switch is zero and the zero-volatge turn-off is achieved for the Si IGBT.

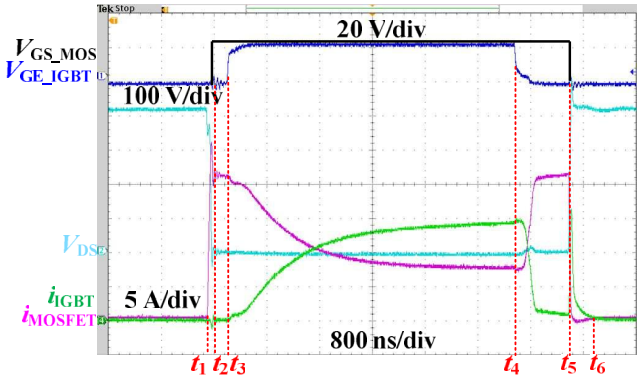


Fig. 4. Typical experiment waveform for the hybrid switch with turn-on and turn-off delays.

III. Four Control Freedoms Active Gate Driver

Fig. 5 shows the function blocks of the proposed active gate driver, which mainly includes the flowing three parts: 1) field programmable gate array (FPGA) controller: due to the high resolution and control flexibility of FPGA controller, it is adopted to achieve the system control; 2) variable gate voltage control circuit: the variable gate voltage circuit can adjust the positive gate voltage based on the control signals generated from FPGA controller; 3) two independent gate driver channels: two gate drivers are adopted to achieve independent control of two paralleled devices.

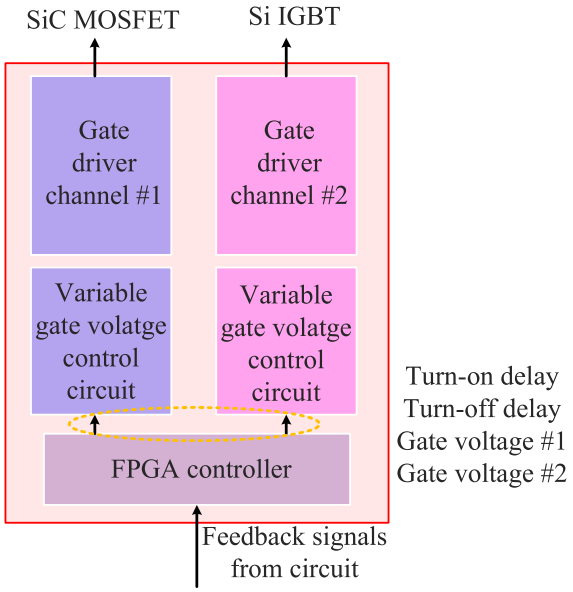


Fig. 5. Function blocks of the proposed active gate driver.

The variable gate voltage control circuit is shown in Fig. 6. It includes an analog adder circuit to adjust the voltage level and a voltage amplifier to boost the maximum output current and amplify the voltage level. By controlling the input signals generated from FPGA controller, the analog adder circuit can adjust the output voltage level accordingly. 2^n voltage adjustment steps can be obtained by using n channel digital isolator. In this design, a 6-channel digital isolator with six different resistor values are selected to provide 64 volatge adjustment steps. The voltage amplifier's output voltage V_{GS_H} can be calculated with Eq. (1).

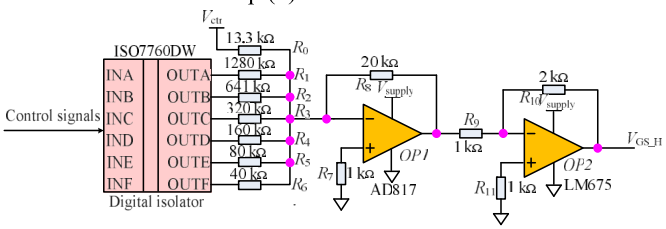


Fig. 6. Variable gate voltage control circuit.

$$V_{GS\_H} = V_{ctr}\left(\frac{1}{R_0}+\frac{INA}{R_1}+\frac{INB}{R_2}...\frac{INF}{R_6}\right)R_8\frac{R_{10}}{R_9} \quad (1)$$

Normally, the maximum gate voltage rating for power devices is around 25 V. Therefore, in this paper, the adjustable gate voltage is designed in the range of [15 V, 25 V]. In this design, the control voltage V_{ctr} equals 5 V, for the gate voltage lower boundary value 15 V, the following equation should be satisfied.

$$5\times\left(\frac{R_8}{R_0}\right)\times 2 = 15 \quad (2)$$

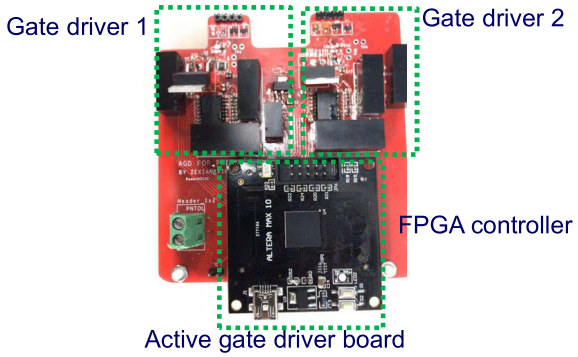
For the gate voltage upper boundary value 25 V, the following equation should be satisfied.

$$5\times\left(\frac{R_8}{R_0}+\frac{R_8}{R_1}+\frac{R_8}{R_2}+\frac{R_8}{R_3}+\frac{R_8}{R_4}+\frac{R_8}{R_5}+\frac{R_8}{R_6}\right)\times 2 = 25 \quad (3)$$

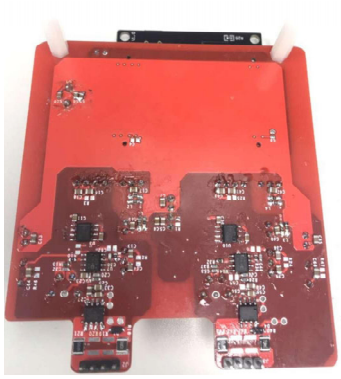
By adopting the proposed variable gate voltage control circuit for each gate driver channel, two control freedoms of independent gate voltages can be introduced. For the other two control freedoms: turn-on delay and turn-off delay, the FPGA controller can easily generate the required delays for two gating signals.

IV. Experiment Results

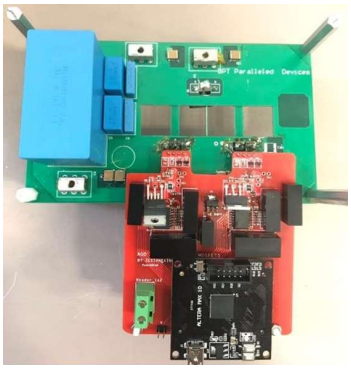
Fig. 7 shows the picture of the designed AGD, there are two independent gate drive channels and field-programmable gate array (FPGA) is used to control the gate pattens. Fig. 7(c) shows the double pulse test (DPT) board to examine the characteristics of hybrid switch.



(a) Top view



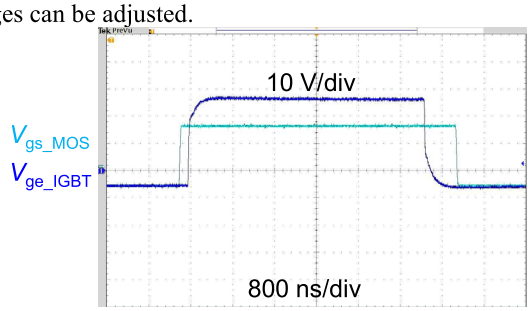
(b) Bottom view



(c) DPT board

Fig. 7. Top view and bottom view of the designed AGD and DPT board.

Fig. 8 shows the possible gate pattens for paralleled device, the turn-on and turn-off delays and two independent gate voltages can be adjusted.



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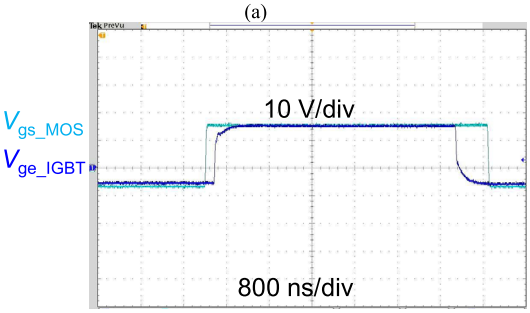

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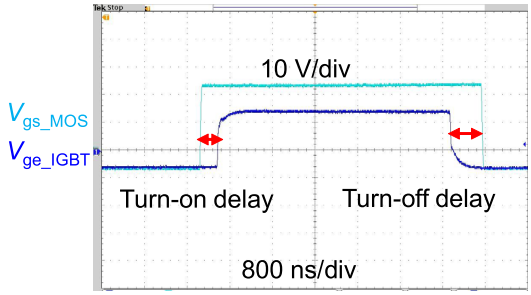

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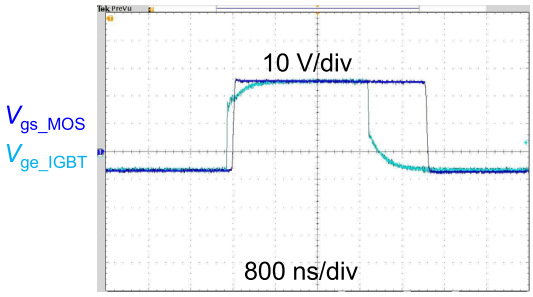


(d)

Fig. 8. Different gate control pattens for paralleled device.

In the experiment, Si IGBT with part number of IGW40T120 from Infineon and SiC MOSFET with part number of C2M0160120D from CREE are selected. Fig. 9 shows the experiment waveform when same gate voltage and no turn-on and turn-off delays are applied for both devices. Clearly, there are severe oscillation during the turn-on process due to different switching speed of Si IGBT and SiC MOSFET. SiC MOSFET turns on first and has most of the current. During the turn-off process, SiC MOSFET turns-off first, and the load current flows through Si IGBT. Then, IGBT undergoing a long time period turn-off process with long tail current, which generates considerable switching loss.

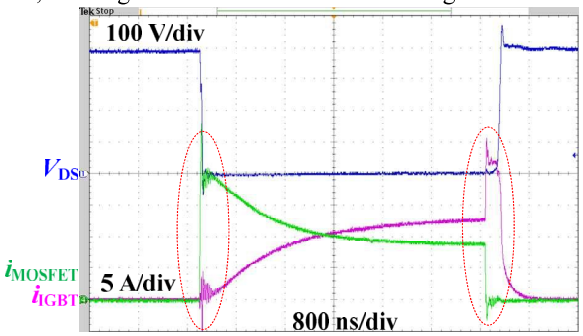


Fig. 9. Double test waveform with same gate voltages and no turn-on and turn-off delays.

To reduce the switching loss, turn-on delay and turn-off delay are inserted to help IGBT achieve soft switching. Specifically, the zero-voltage turn-on and zero-voltage turn-off for IGBT are achieved as shown in Fig. 10.

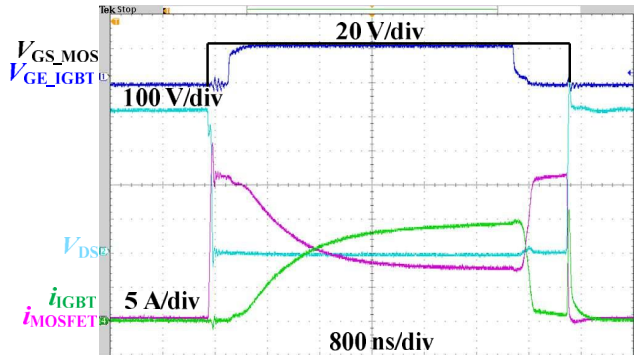


Fig. 10. Double test waveform with turn-on and turn-off delays to achieve soft switching of IGBT.

To optimize the hybrid switch performance, experiment results with different turn-on and turn-off delays are summarized in Table 1 and drawn in Fig. 11. From the results, it can be seen that the turn-on loss is minimized when the turn-on delay is slightly higher than zero, which ensures the zero-voltage turn-on of IGBT.

TABLE. I. TURN-ON LOSS WITH DIFFERENT TURN-ON DELAYS

Turn-on	-0.5 μs	0 μs	0.3 μs	0.8 μs	1.5 μs	2 μs
E_{on_MOS}	10. 4 μJ	528 μJ	616 μJ	731.2 μJ	783.2 μJ	814.8 μJ
E_{on_IGBT}	887.5 μJ	251.4 μJ	32 μJ	20.16 μJ	20 μJ	21.456 μJ
E_{on_tot}	897.9 μJ	779.4 μJ	648 μJ	751.36 μJ	803.2 μJ	836.23 μJ

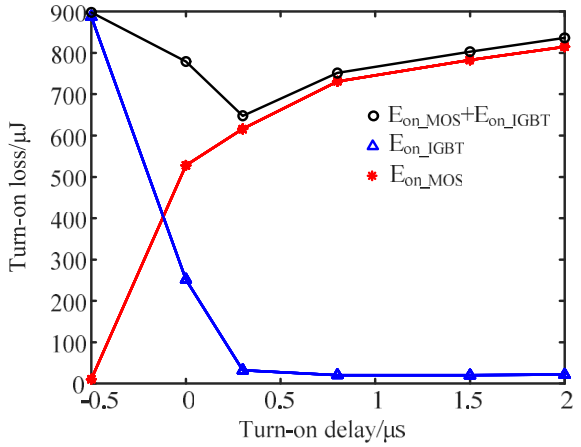


Fig. 11. Turn-on loss of hybrid switch with different turn-on delays.

Similarly, the experiment results with different turn-off delays are summarized in Table 2 and drawn in Fig. 12. When there is no turn-off delay, the turn-off loss is large due to the long tail current of the IGBT. The total turn-off loss is reduced with the increase of turn-off delay to guarantee the zero-voltage turn-off of IGBT. Further increase turn-off delay will increase the total turn-off loss since the turn-off loss of MOSFET is increasing. The optimal point is around the minimum delay time that ensures zero-voltage turn-off of IGBT.

TABLE. II. TURN-OFF LOSS WITH DIFFERENT TURN-OFF DELAY

Turn-off delay	0 μs	1 μs	1.5 μs	1.8 μs	2.5 μs	4 μs
E_{off_MOS}	137. 8 μJ	423.6 μJ	505 μJ	573 μJ	693.36 μJ	928.8 μJ
E_{off_IGBT}	2768 μJ	610.4 μJ	454 μJ	360.4 μJ	237.36 μJ	175.8 μJ
E_{off_tot}	2905.9μJ	1034 μJ	959 μJ	933.4 μJ	930.7 μJ	1104.6 μJ

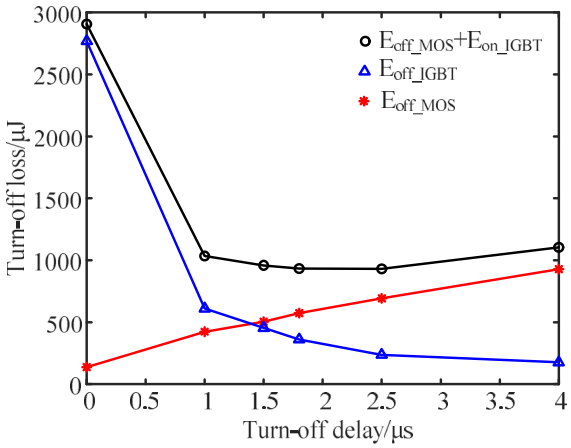
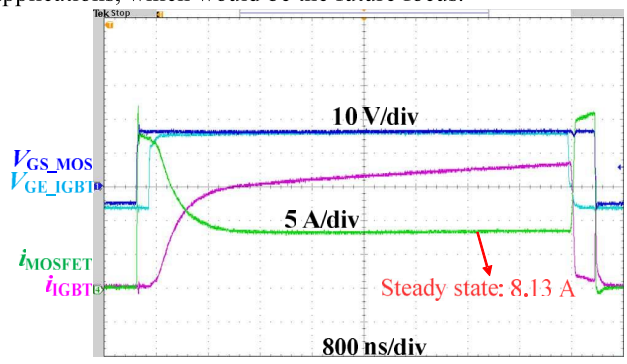
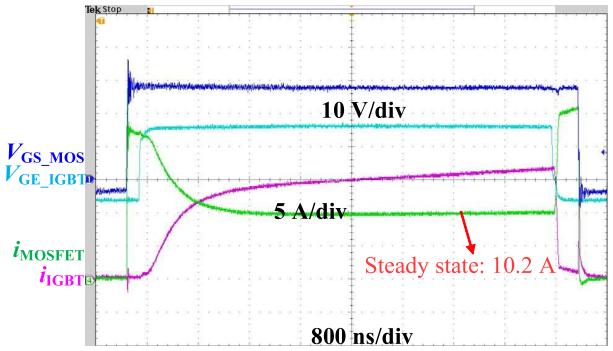


Fig. 12. Turn-off loss of hybrid switch with different turn-off delays.

Furthermore, current distribution between two devices is also of great interest for hybrid switch. Traditionally, the current distribution is only depended on the load current. However, with the proposed AGD, the gate voltages for two devices are adjustable, which can dynamically modify the device on-state resistance or forward voltage. Thus, the current distribution can be dynamically adjusted by regulating the gate voltages. Fig. 13 shows experiment results of the current distribution between two devices. If same gate voltages are applied, the steady state current for MOSFET is around 8.13 A. If the gate voltage for MOSFET is increased from 15 V to 25 V, the steady current for MOSFET is increased from 8.13 A to 10.2 A. The MOSFET on-state resistance is decreasing with the increase of gate voltage, so the current consumed by MOSFET is increased. The current distribution capability is beneficial for thermal balance and reliability improvement for hybrid switch in power converter applications, which would be the future focus.



(a) with same gate voltages



(b) with different gate voltages

Fig. 13. Current distribution capability with the proposed AGD.

V. Conclusion and Future Work

In this paper, an active gate driver with four control freedoms, including two independent gate voltages, turn-on and turn-off delays, is proposed for hybrid SiC MOSFET and Si IGBT application. Compared with traditional gate controls for hybrid switch, two additional control freedoms are provided. Based on the experiment results, the current distribution inside the hybrid switch can be dynamically adjusted so that the conduction losses for two individual switches can be controlled. Thus, the further optimization of hybrid switch can be achieved. In the future, the efficiency optimization and thermal balance with the proposed AGD will be investigated. To achieve this goal, the following work and challenges have to be tackled:

1) Power loss model development: an accurate power loss models for the Si IGBT and SiC MOSFET inside the hybrid switch should be derived. However, the difficulty of deriving the accurate power loss models is the coupling between the junction temperature and power loss.

2) Thermal model development: to achieve optimal control or balance of junction temperatures for Si IGBT and SiC MOSFET, the thermal model should be developed to estimate the device junction temperature.

3) Feedback circuit design: the device power loss and junction temperature are related with the circuit voltage and current. Thus, the operating voltage and current for the device should be detected and send to the controller as inputs. Based on these input signals, the device power loss and junction temperature can be derived.

4) Control strategy: for the proposed gate driver, it has four control freedoms. To optimize the hybrid switch performance, the specific control strategies should be investigated based on the applications and optimization targets.

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