Modeling and Characterization of 10-kV SiC MOSFET Modules for Medium-Voltage Distribution Systems

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Abstract—This work presents the modeling and characterization of 10-kV SiC MOSFET modules used for medium-voltage distribution system applications. In addition to the nonlinear junction capacitances of the devices, the model includes the nonlinearities present at steady-state like transfer characteristics and the behavior in the Ohmic region, which allows to increase the accuracy of the SiC MOSFET model. Furthermore, the parasitic inductances in the circuit (such as the source inductance shared by the power stage and driver loop and the drain inductance) are considered in the model since it has been demonstrated previously that it influences the total losses. By using the proposed model, the calculated voltage and current transients show a good match with the experimental results.

Index Terms—SiC MOSFET switching analysis, switching losses, parasitic effect, analytical model, characterization.

I. INTRODUCTION

Today's society is increasingly dependent on a safe and reliable supply of electricity. The growing concerns about the availability of primary energy and the aging infrastructure of current electricity transmission and distribution systems are increasingly challenging security, reliability, and power quality [1]. In this scenario, new proposals are emerging, such as the implementation of microgrids and smart grids, aimed at managing and optimizing generation and demand more flexibly, maintaining the stability and reliability of the system. The integration of renewable energies in microgrids and their interconnection with conventional medium-voltage distribution systems can be done through power electronic converters using low-loss medium-voltage devices like SiC MOSFET modules [1]– [3].

The design of a power converter for medium voltage applications requires proper understanding of tbe the static and dynamic behavior of power transistors. Several modeling approaches have been proposed for SiC MOSFETs, including semiconductor physics models [4] and behavioral models [5]–[8] as summarized below.

Y. Ren, et. al. [6] proposed an accurate analytical model, which allows calculating the power loss of MOSFET transistors. The nonlinearity of the capacitors of the devices and the

parasitic inductance in the circuit, such as the source inductor shared by the power stage and driver loop, the drain inductor, etc., are considered. In addition, it considered the ringing always observed in the switching power supply and ignored in most traditional loss model. In this paper, the ringing loss is analyzed in a simpler way with a clear physical meaning. Based on this model, the circuit power loss can be accurately predicted. As it is explained in this work, the conventional analytical loss model (see for example [9] and [10]) treats the switch turn-ON and turn-OFF waveforms as piecewise linear. It does not consider the source inductance and the nonlinear characteristics of the capacitors of the device. Therefore, the result normally does not match the experimental results very well, especially for high-frequency applications.

The proposal given in [4] includes the high-frequency parasitic components in the circuit and enables fast, accurate simulation of the switching behavior using only datasheet parameters. Nonlinearities in the junction capacitances of the devices are incorporated to increase the accuracy of model by fitting their nonlinear curves to a given expression.

Reference [5] presented an analytical loss model for the commutation pair of silicon carbide (SiC) MOSFETs and SiC Schottky barrier diodes. Compared to the conventional loss calculation method, the proposed model is derived based on the conservation of energy, which considers the impact of the displacement currents on estimating the turn-ON and turn-OFF losses.

The work addressed here, in addition to the nonlinear junction capacitances of the devices, includes the nonlinearities encountered during steady-state conditions like transfer characteristics and the behavior in the Ohmic region, which allows the accuracy of the SiC MOSFET model to be increased. The parasitic inductance in the circuit (such as the source inductor shared by the power stage and driver loop and the drain inductor) are considered in the model, as it was demonstrated it influences the total device losses. The modeling and extraction methodology of the model parameters are given, and the impact of operational conditions on the model parameters is

studied.

The presented analytical model is developed using the characterization of a 10-kV SiC MOSFET Half-Bridge Module. Static characterizations, including current-voltage characteristics (output and transfer characteristics), on-resistance, and capacitance-voltage characteristics, are acquired using an Agilent curve tracer at different case temperatures to get device performance. A double-pulse test setup was built to perform dynamic characterization of the SiC MOSFET during turn-ON and turn-OFF transients at 5-kV drain bias and different load currents.

By using the proposed model, the total losses of the devices can be calculated with high accuracy, and the maximum switching frequency under different operating conditions can be predicted for a given application.

II. MODELING OF THE SiC MOSFET SWITCHING CHARACTERISTICS

A mathematical modeling of each period is necessary to represent the SiC MOSFET turn-ON and turn-OFF transients. The final values from one period form the initial conditions for the next period.

For this analysis, Figs. 1(a)-(d) illustrate simplified circuits for different periods valid for the turn-ON and turn-OFF in order to represent the dynamic behavior corresponding to the hard-switching operation mode [1]. The switching characteristics of the SiC MOSFETs given in [3]– [5] address the nonlinearity of the capacitors of the devices and the parasitic inductances in the circuit.

In these equivalent circuits, L_{sd} and R_s represent the sum of all parasitic inductances and resistance in series with the SiC MOSFET, L_s represents the MOSFET common source inductance. Parasitic capacitances of the SiC MOSFET C_{GS}, C_{GD}, and C_{DS}, diode and load inductor lumped parasitic capacitance C_{dk}. The two inputs are the supply voltage V_{dd} and load current I_{dd}.

Here, the modeling of the SiC MOSFET transients proposed in [4] is adopted to describe the turn-ON and turn-OFF transients.

A. MOSFET Turn-ON Transient

The drain terminal of the MOSFET is positively biased, turning the device ON. From the user's point of view it is important to determine the energy loss during turn-ON. Consequently, from descriptions of the turn-ON action and the dynamic model of the MOSFET, turn-ON losses can be estimated.

1) Turn-ON delay period: This period is defined by $v_{GS} < V_{th}$ and $v_{DS} = V_{dd}$. There is no drain current I_d other than leakage because of the two pn junctions, which means that one is blocking. This gives rise to a MOSFET equivalent circuit model of two opposing diodes as shown in Fig. 1(a).

This period begins when the gate pulse is applied, and the input capacitors of the SiC MOSFET C_{GS} and C_{GD} are charged. The MOSFET is off until v_{GS} reaches V_{th}. The load current, I_{dd}, circulates through the top Schottky diode. In

this period, the drain current is zero, and the drain-to-source voltage is equal to the dc-link voltage V_{dd}. The expressions that describe the dynamics of this period can be summarized as follows [4].

$$V_g = R_g i_g + v_{GS} + L_S \frac{di_g}{dt} \tag{1}$$

$$i_g = C_{GS} \frac{dv_{GS}}{dt} + C_{GD} \frac{dv_{GD}}{dt} \tag{2}$$

$$v_{GS} = v_{GD} + v_{DS} \quad (v_{DS} = V_{dd}) \tag{3}$$

$$i_g = C_{iss} \frac{dv_{GS}}{dt} \quad (C_{iss} = C_{GS} + C_{GD}) \tag{4}$$

2) Current rise period: During this period the channel current will be directly proportional to $(v_{GS} - V_{th})$. The current rise time ends when v_{GS} reaches V_{mil} from V_{th}, where $V_{mil} = I_{dd}/G + V_{th}$, and G is the transconductance of the MOSFET. In this period, the drain current will reach the load current. The equivalent circuit for this period corresponds to Fig. 1(b). The expressions for this period correspond to (2) in addition to the following

$$V_{dd} = v_{DS} + (L_s + L_{sd}) \frac{di_d}{dt} + R_s i_d \tag{5}$$

$$i_d = G(v_{GS} - V_{th}) + C_{oss} \frac{dv_{DS}}{dt} \tag{6}$$

where $(C_{oss} = C_{DS} + C_{GD})$.

$$V_g = R_g i_g + v_{GS} + L_s \frac{di_d}{dt} \tag{7}$$

3) Voltage fall period: The voltage fall period corresponds to the time required for V_{ds} to reach $V_{ds}(on)$. The equivalent circuit for this period corresponds to Fig. 1(c). In addition to the equations indicated above, the ones shown below must be solved for this period

$$C_{dk} \frac{dv_{dk}}{dt} = (i_d - I_{dd}) \tag{8}$$

$$V_{dd} = v_{DS} + (L_s + L_{sd}) \frac{di_d}{dt} + R_s i_d + v_{dk} \tag{9}$$

4) Ringing period: As indicated in [4], this period can be approximated by the time required for v_{gs} to reach V_{gg} from the value at the end of previous period.

The equivalent circuit for this period corresponds to Fig. 1(d). The expression of current i_d is given below.

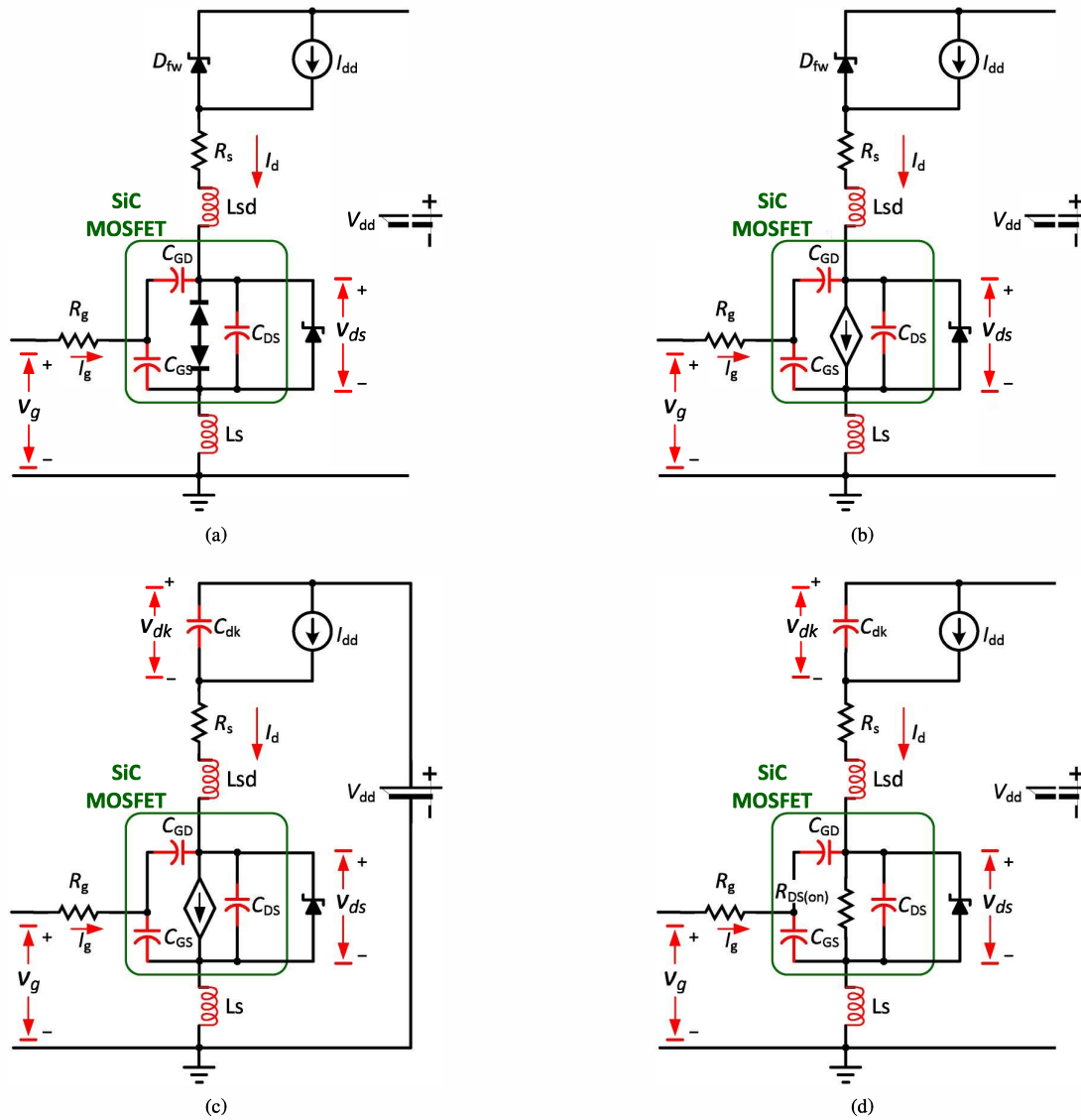$$i_d = \frac{v_{DS}}{R_{DS(on)}} + C_{oss} \frac{dv_{DS}}{dt} \tag{10}$$

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Fig. 1. Equivalent circuits and state equations used to represent turn-ON and turn-OFF behaviors corresponding to hard-switching operation mode [4]: (a) turn-ON delay period, (b) current rise time period, (c) voltage fall time period and (d) ringing period.
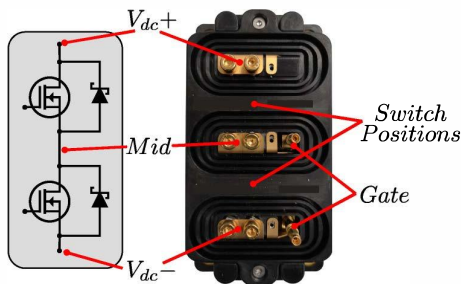

Fig. 2. 10-kV SiC MOSFET XHV-9 module.

B. MOSFET Turn-OFF Transient

The turn-OFF action of the SiC MOSFET is the reverse of the turn-ON action. The input capacitance C_{iss} is charged to a level that the gate voltage $v_{GS} \leq V_{th}$, the threshold level.

The four turn-OFF periods (see Fig. 1) are identical to the turn-ON periods but occur in reverse order and the state equations can be derived in a similar manner [4].

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III. CHARACTERIZATION OF THE SiC MOSFET

A. Static Characterization

The static characterization of the 10-kV SiC MOSFET from CREE seen in Fig. 2 includes DC and AC characterizations [11]. The DC characterization includes on-state resistance, output and transfer characterizations were performed using an Agilent B1505A Power Analyzer/Curve Tracer with a Keysight N1265A Ultra High Current Expander Fixture for high power characterization. These DC characterizations are made at different case temperatures to show the temperature dependency of the SiC MOSFET. The module transfer characteristics illustrated in Fig. 3 is obtained at 20 V Drain-Source voltage bias while the Gate-Source voltage is swept from 0 V to 15 V for different case temperatures. The derivative of the transfer characteristics or the module transconductance expressed in (13) is illustrated in Fig. 4 for different case temperatures.

Similarly, the output characteristics of the MOSFET is measured by sweeping the Drain-Source voltage at different Gate-Source voltages and different case temperatures. Fig. 5 and Fig. 6 display the output characteristics for five different Gate-Source voltages and five different case temperatures, respectively. The on-state resistance is measured at $V_{GS} = 15$ V at different case temperatures. Fig. 7 shows the on-state resistance characterization. At room temperature $(T_c = 25°C)$ and $I_{DS} = 40\,A$, the on-resistance is $R_{DON} = 69.7\,m\Omega$ while at $(T_c = 150°C)$ and $I_{DS} = 40\,A$ the on-resistance is $R_{DON} = 162.6\,m\Omega$ which is more than twice the initial on-resistance. The output and transfer characteristics, as well as the on-state resistance, can be model by (11), (12), and (14) where their fitting coefficients are stated in Tables I, II, , III and IV, respectively.

Furthermore, the AC characterization was made with the Agilent B1505A and the Keysight N1273 Capacitance Test Feature to measure the nonlinear junction capacitances (C_{iss}, C_{oss} and C_{rss}) of the 10-kV MOSFET up to 3-kV as given in. 8. The capacitance can be modeled using expression (15), and the coefficients are listed in Table V.

TABLE II
OUTPUT CHARACTERISTICS FOR VARIOUS GATE-SOURCE VOLTAGES FUNCTION COEFFICIENTS

V_{GS}	I_{ss}	τ
5 [V]	0.031	0.5
10 [V]	8.1	-1.15
12 [V]	24	0.65
13 [V]	38.5	0.43
15 [V]	90	0.195

$$I_{DS} = I_{ss}\left(1 - e^{-\tau V_{DS}}\right) \qquad (11)$$

$$I_{DS} = \frac{\alpha}{1 + e^{-\beta(V_{GS}-\gamma)}} \qquad (12)$$

$$G = \frac{\alpha\beta\,e^{-\beta(V_{GS}-\gamma)}}{\left(1 + e^{-\beta(V_{GS}-\gamma)}\right)^2} \qquad (13)$$

TABLE III
OUTPUT CHARACTERISTICS FOR VARIOUS CASE TEMPERATURE AND $V_{GS} = 15$ [V] FUNCTION COEFFICIENTS

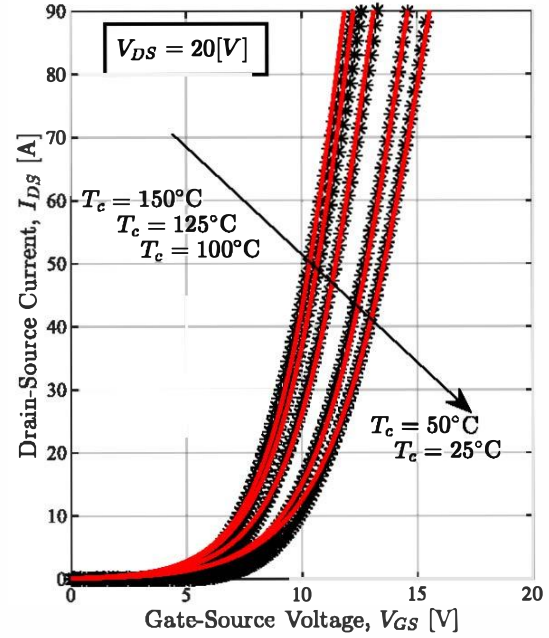| Temperature	I_{ss}	τ
25°C	140	0.125
125°C	140	0.07
100°C	140	0.0585
150°C	140	0.0485

Fig. 3. Transfer characteristics for various case temperatures.

$$R_{DS(on)} = \kappa e^{\rho \cdot I_{DS}} \qquad (14)$$

$$C = \frac{1}{\dfrac{1}{C_{ov}} + \dfrac{V_{DS}^x}{C_j}} + C_{hv} \qquad (15)$$

TABLE IV
ON-RESISTANCE FUNCTION COEFFICIENTS

Temperature	κ	ρ
25°C	0.0611	0.0035
50°C	0.0745	0.0018
125°C	0.1115	0.0007
100°C	0.1348	0.0004
150°C	0.16	0.0004

B. Dynamic Characterization

For the dynamic characterization of the SiC module, a double-pulse test (DPT) was conducted on the XHV-9 10-kV SiC MOSFET to measure the energy loss under ON and
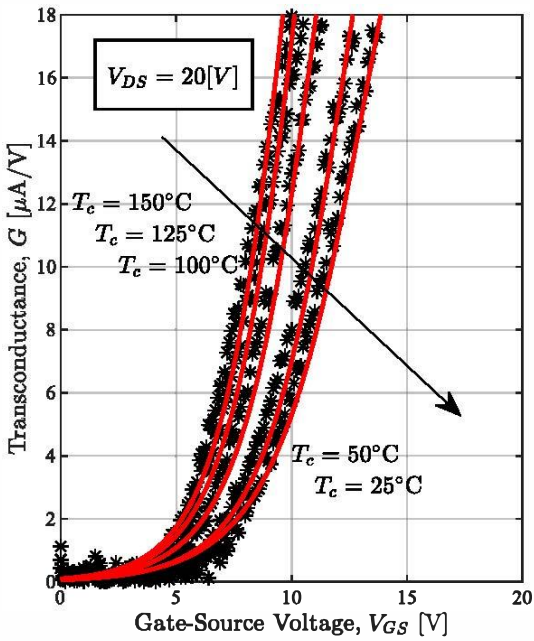
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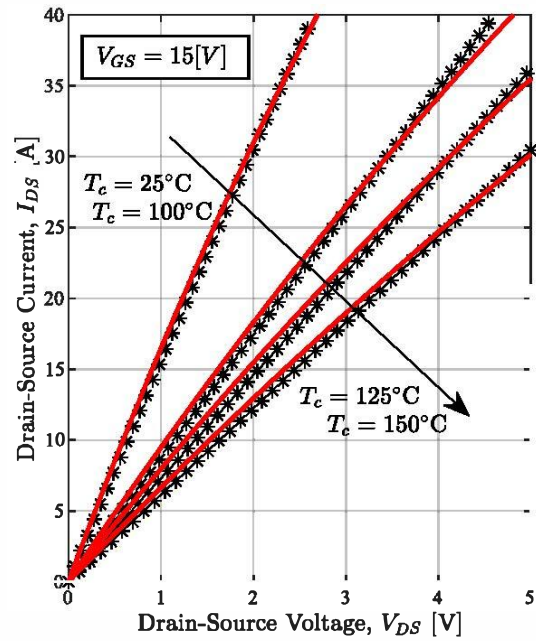Fig. 4. Module transconductance for various case temperatures.

Fig. 6. Output characteristics with temperature as a parameter.
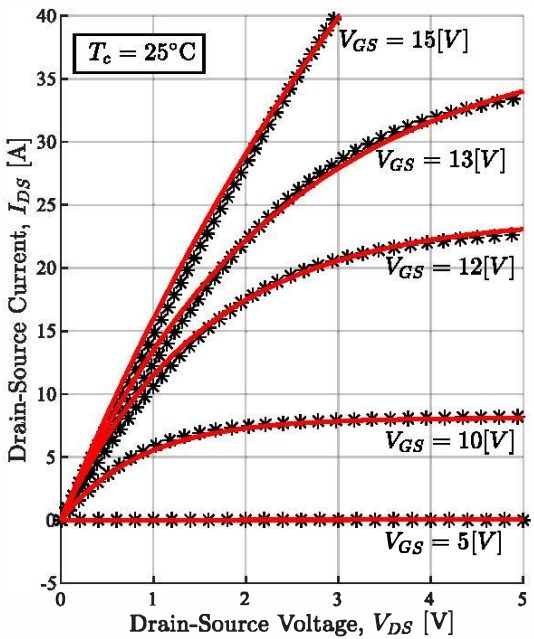

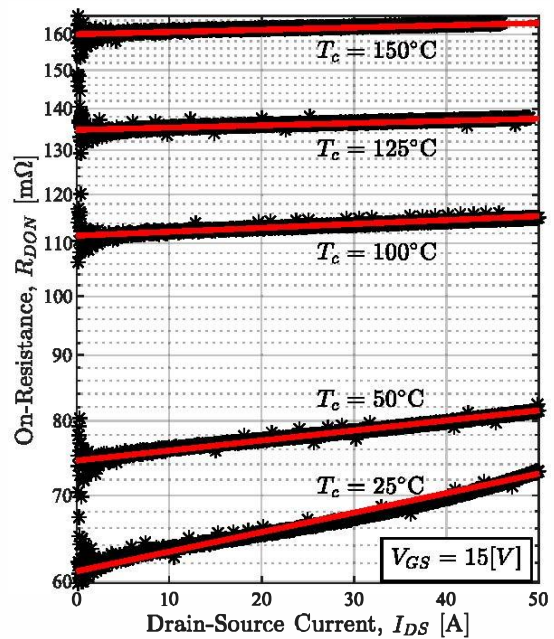Fig. 5. Output characteristics with the gate-source voltage as a parameter.

Fig. 7. On-resistance vs drain-Source current with temperature as a parameter.

OFF conditions. The DPT setup is illustrated in Fig. 9. The PCB board with decoupling capacitors in Fig. 10 is used to reduce parasitic inductance between the module and the capacitor bank, consisting of two 30 μF 4.5-kV capacitors in series. A parasitic inductance of $50\,nH$ was measured using a Vector Network Analyzer Bode 100. A $\pm$ 20 kV Glassman
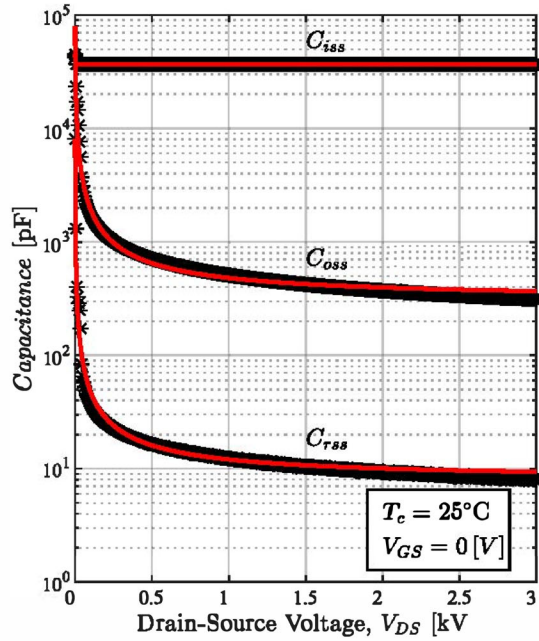
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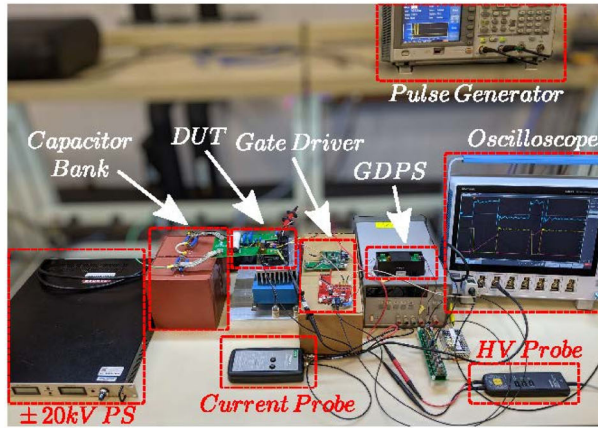Fig. 8. Capacitance vs drain-source voltage (0 - 3 [kV]).

Fig. 9. Double pulse test setup.

power supply is used to charge the capacitor bank to supply the current to a 315 μH air inductor load. The gate driver signal is generated using a function generator controlled by LabVIEW and sent to the gate driver through an optical signal adapter. The switching losses were measured at different current levels as shown in Table VI. To measure the voltage and current on the XHV-9 module, a high differential voltage probe (THDP0100) and a Rogowski current probe (PEM CWT Ultra Mini) were used with a MSO58 oscilloscope. Fig. 11 shows a screenshot of the MSO58 oscilloscope for a DPT at 60 A load current.
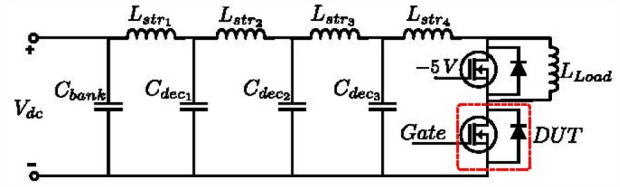

Fig. 10. Double pulse test equivalent schematic circuit.

TABLE V
10-KV SiC MOSFET CAPACITANCES

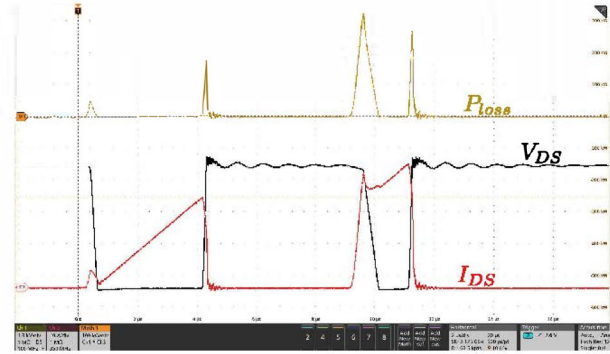| Capacitance	C_{ov}	C_{hv}	C_j	x
C_{iss}	42.4 [nF]	36.5 [nF]	500	1
C_{oss}	45 [nF]	312 [pF]	170000	1
C_{rss}	8.06 [nF]	8.05 [pF]	4000	1

Fig. 11. DPT waveforms at $V_{DS} = 5\,kV$ and $I_{DS} = 60\,A$.

IV. EXPERIMENTAL AND SIMULATION RESULTS

The different functions indicated in Section II are solved by programming a numerical algorithm to solve the set nonlinear differential equations for each period.

The nonlinear capacitance as a function of drain-source voltage was included using the expression (15) with the parameters shown in Table V, the transconductance according to the expression given in (13), with the parameters of Table I, and the on-state resistance as a function of current is shown in (14), and its parameters correspond to the ones given the Table IV.

Fig. 12- Fig. 14 show experimental and modelled dynamic waveforms corresponding to the turn-ON and turn-OFF of the 10-kV Half-Bridge SiC Power Module for 5kV of dc-bus

TABLE VI
DOUBLE PULSE TEST PULSE SPECIFICATIONS

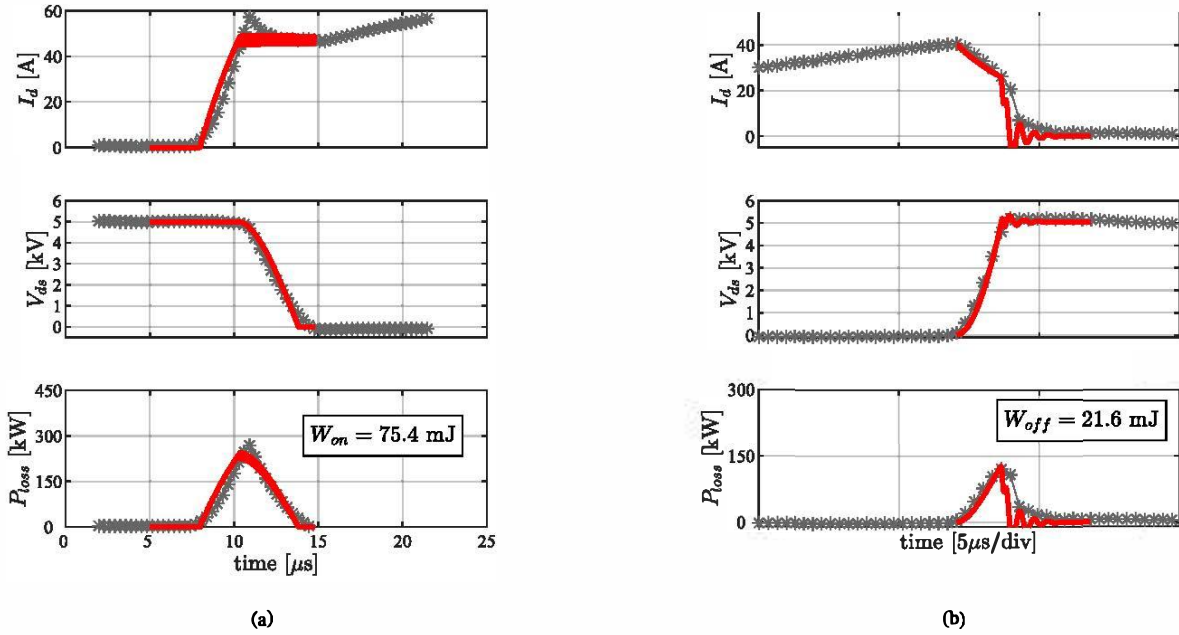| Voltage	Current	1st Pulse	OFF	2nd Pulse
5 [kV]	20 [A]	1.3 [μs]	2 [μs]	1.3 [μs]
5 [kV]	30 [A]	1.9 [μs]	4 [μs]	1.5 [μs]
5 [kV]	40 [A]	2.53 [μs]	4 [μs]	2 [μs]
5 [kV]	50 [A]	3.16 [μs]	5 [μs]	2 [μs]
5 [kV]	60 [A]	3.95 [μs]	6 [μs]	2 [μs]

Fig. 12. Experimental (x mark) and modelled (solid red line) dynamic waveforms corresponding to the turn-ON and Turn-OFF of the 10-kV XH9-9 Half-Bridge SiC Power Modules for 5kV of dc-bus voltage and a drain current of 45 A. Bottom subfigures show the dissipation of the module.
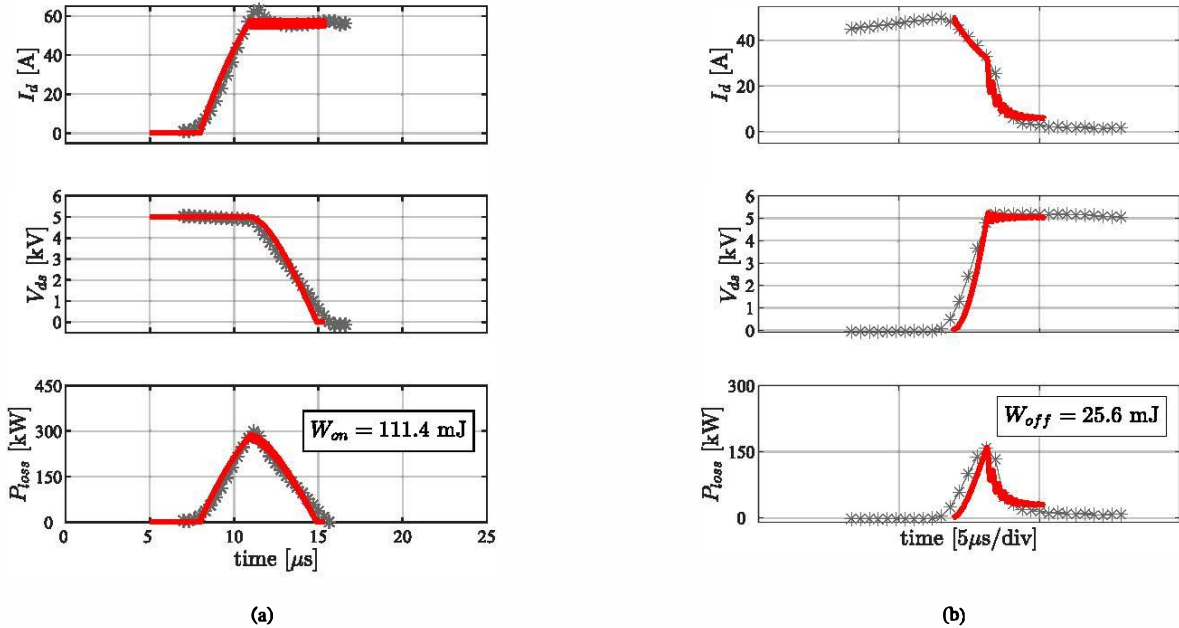

Fig. 13. Experimental (x mark) and modelled (solid red line) dynamic waveforms corresponding to the turn-ON and Turn-OFF of the 10-kV XH9-9 Half-Bridge SiC Power Modules for 5 kV of dc-bus voltage and a drain current of 56 A. Bottom subfigures show the dissipation of the module.

voltage and a drain current of 45 A, 56 A y 60 A, respectively. These results correspond for a $T_j = 25°C$.

The gate resistance is equal to 8Ω, which corresponds to the resistance included in the gate driver plus the internal one

of the module. The gate supply voltage is +20V for turn-on process and -5V for turn-off the MOSFET.

These figures also provide the dissipation of the module for each case.

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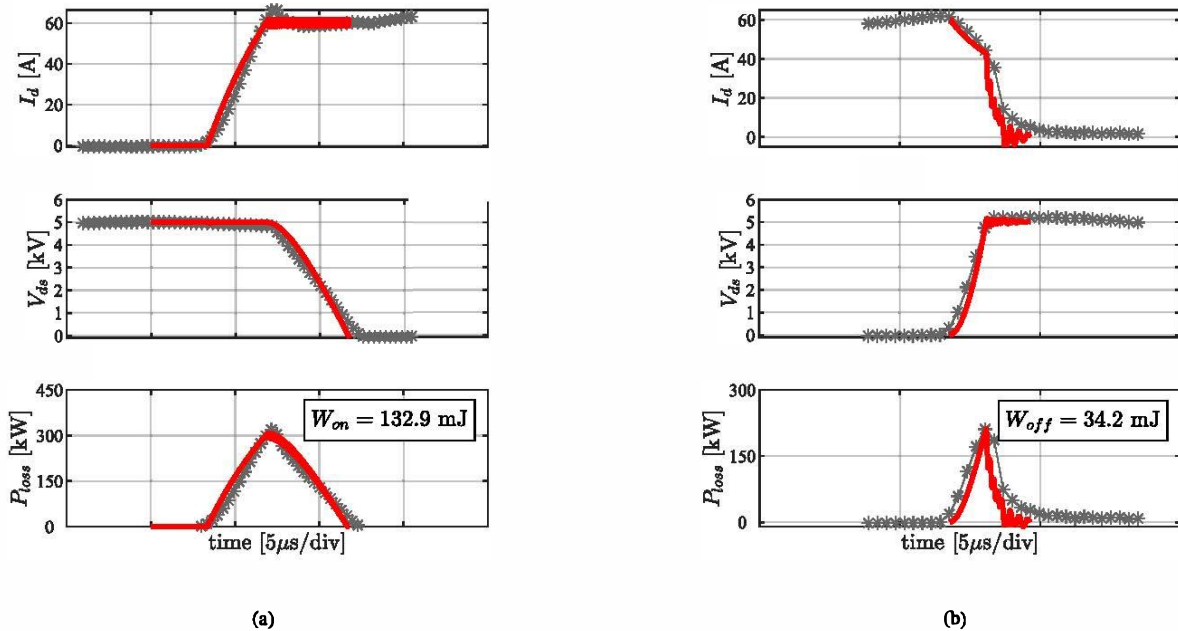(a)   (b)

Fig. 14. Experimental (x mark) and modelled (solid red line) dynamic waveforms corresponding to the turn-ON and Turn- OFF of the 10-kV XH9-9 Half-Bridge SiC Power Modules for 5 kV of dc-bus voltage and a drain current of 60 A. Bottom subfigures show the dissipation of the module.

In these figures, the calculated voltage and current transients show a good match with the experimental results. In this manner, it can concluded that the model can predict with very high accuracy the dynamic behavior of the SiC MOSFET.

ACKNOWLEDGMENT

V. CONCLUSION

This work model and characterized a 10-kV SiC MOS-FETs modules used for medium-voltage distribution system applications. The model included the nonlinearities in the junction capacitances of the devices, steady-state characteristics like transfer characteristics, and the feature in the Ohmic region were incorporated to increase the accuracy of the SiC MOSFETs models by fitting their nonlinear curves to the dynamic model. The characterization of the module included static at different case temperatures to show the temperature dependency of the SiC MOSFET. Furthermore, the dynamic characterization of the SiC module was conducted by a double pulse test on the XHV-9 10-kV SiC MOSFET to measure the energy loss during the ON and OFF transients. The results of the model obtained confirmed the capability to predict the switching losses accurately. In future work, the behavior of the reverse recovery of the Schottky diode will be modeled to incorporate these losses, and also including different scenarios such as soft-switching operating mode.

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