A Wireless Power Transfer based Gate Driver Design for Medium Voltage SiC MOSFETs

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***Abstract*—Wide band gap (WBG) devices have been widely adopted in numerous industrial applications. In medium voltage applications, multi-level converters are necessary to reduce the voltage stress on power devices, which increases the system control complexity and reduces power density and reliability. High voltage silicon carbide (SiC) MOSFET enables the medium voltage applications with less voltage level, simple control strategy and high power density. Nevertheless, great challenges have been posed on the gate driver design for high voltage SiC MOSFET. Wireless power transfer (WPT) can achieve power conversion with large airgap, which can satisfy the system isolation requirement. Thus, in this article, a WPT based gate driver is designed for the medium voltage SiC MOSFET. The coil is optimized by considering voltage isolation, coupling capacitance, size, and efficiency. Experimental prototype was built and tested to validate the effectiveness of the proposed WPT based gate driver.**

Keywords—Silicon carbide (SiC) MOSFET, medium voltage, gate driver, wireless power transfer (WPT)

I. Introduction

High power and medium voltage (MV) applications are increasingly important. To achieve the required voltage blocking capability, multiple power devices in series connection is necessary. However, the voltage sharing among these power devices cannot be ensured [1, 2]. High voltage silicon carbide (SiC) metal–oxide–semiconductor field-effect transistor (MOSFET) can effectively avoid the series connection and enable the application of the simple converter topology in these MV applications. In particular, 10 kV SiC MOSFET has been characterized and adopted in MV applications by several research groups [3]-[5].

The *dv/dt* of the 10 kV SiC MOSFET can reach up to 110 kV/μs [6]. Such high *dv/dt* may flow through the coupling capacitance of the gate driver isolation transformer and generate noise current to cause malfunction of the control circuit as demonstrated in Fig. 1 [6]. Therefore, a careful design of the gate driver isolation transformer with extreme low coupling capacitance between primary side and secondary side is desired.

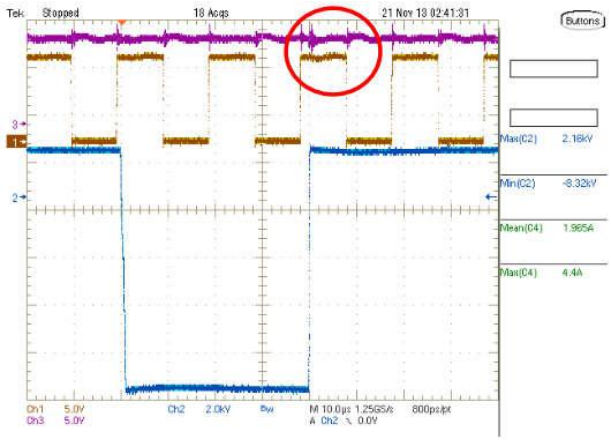


Fig. 1. Waveforms of the common-mode voltage and its influence on the signals on the primary side of the isolation stage. (Ch1: A PWM input of the H-bridge IC on primary side of the isolation stage; Ch2: Common-mode voltage; Ch3: Vcc of the H-bridge IC) [6].

High voltage isolation (>20 kV) is also required for the 10 kV SiC MOSFET gate driver design. To achieve high voltage isolation, the existing methods have been categorized into the following four groups: 1) voltage transformer [6]-[11]; 2) current transformer [12]-[15]; 3) power over fiber [16]; 4) wireless power transfer [17]-[21].

For the voltage transformer, large size transformer core is required to satisfy the creepage and clearance requirements, which increases the volume and weight of gate driver. On the other hand, due to the high coupling between primary side and secondary side, high efficiency operation can be achieved.

The current transformer solution can satisfy the system requirement with less number of turns and lower coupling capacitance when compared with voltage transformer based solution. Another main advantage of current transformer based solution is that it can be simply used to drive multiple power modules. The primary winding is shared among all different channels. However, a large transformer core is still required. The coupling between primary side and secondary side is reduced when compared with the voltage transformer.

Although the optical fiber can achieve extreme low (theoretical zero) coupling capacitance, this solution is expensive and the reported power is only 0.5 W, which may not provide sufficient driving capability for 10 kV SiC MOSFET with multiple dies in parallel [16].

Wireless power transfer (WPT) is also a promising technology for 10 kV SiC MOSFET application. The high voltage isolation requirement can be easily achieved by adjusting the airgap of primary coil and secondary coil, and the coupling capacitance between two coils can be reduced by optimal deign. Moreover, multiple-output can be easily achieved by using WPT technology as demonstrated in [19] and [21]. Although the system efficiency is not very good when compared with other solutions due to the low coupling between primary and secondary, the power loss is acceptable for 10 kV SiC MOSFET applications, where the system power is in the range MW. In [17], an asymmetric primary coil and secondary coil structure is designed to reduce the coupling capacitance. The system coupling capacitance is selected as optimization objective and the parametric sweep method with the aid of ANSYS simulation model is adopted to achieve the coil design. Additional non-isolated regulators are required to obtain the desired gate voltages for turn-on and turn-off.

In this article, a WPT based gate driver is designed for medium voltage applications with low coupling capacitance and high voltage isolation capability. Symmetric coil structure design is adopted to reduce the system complexity and cost. The selected compensation topology can achieve fixed voltage output with constant switching frequency operation, which helps reduce the adoption of the non-isolated regulator for the turn-on gate voltage. The turn-off gate voltage can be generated from a non-isolated regulator. The finite element analysis (FEA) based simulations are performed to achieve the optimal design of the coil by considering various factors into consideration, like voltage gain, efficiency, and coupling capacitance. The overall gate driver structure and implementations are discussed. Finally, experimental results for the developed gate driver are presented under different scenarios.

II. System Design and Optimization

In this section the system structure and optimal design procedures are discussed.

In this work, the inductive power transfer with primary series compensated and secondary series compensated structure as shown in Fig. 2 is selected. For medium voltage gate driver application, the major design objective is to minimize the coupling capacitance between primary side and secondary side. Thus, closed-loop control is not preferred due to the high voltage isolation requirement and introduced extra coupling capacitance. As discussed in [22], the selected circuit topology in Fig. 2 has one operating point, where the converter voltage gain is independent of the load. This operating point can be used to achieve open-loop operation of the converter. Another feature of the selected topology is simplicity, where only two capacitors are used to compensate the voltage drop on the leakage inductors.

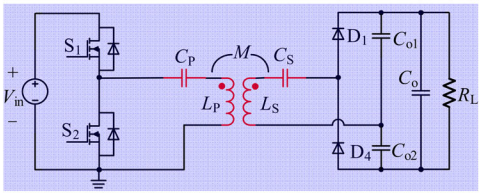


Fig. 2. Circuit diagram of the primary side series compensated and secondary side series compensated inductor power transfer.

The circuit equivalent diagram for the system can be derived as shown in Fig. 3 [22].

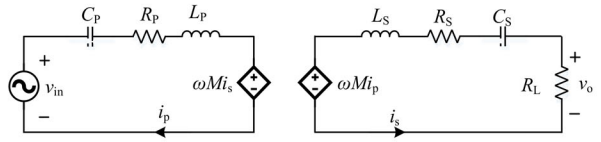


Fig. 3. Equivalent circuit diagram.

According to Fig. 3, the voltage transfer ratio or voltage gain can be derived as follows

$$G = \frac{v_{\text{out}}}{v_{\text{in}}} = \frac{\omega M}{Z_P Z_S + \omega^2 M^2} R_L \tag{1}$$

where Z_P and Z_S are the primary and secondary impedance, respectively. ω is the angular switching frequency. M is the mutual inductance of the primary side and secondary side coils. There exists an operating switching that ensures that the voltage transfer ratio is independent of the load [22], which is desired for the 10 kV gate driver application with simple circuit and high reliability. Meanwhile, feedback control would increase coupling capacitance between the primary side and secondary side. Therefore, in this research, the converter switching frequency is designed at this switching frequency point as shown in Eq. (2) to achieve constant voltage transfer ratio.

$$\omega = \sqrt{\frac{\omega_p^2 + \omega_s^2 + \Delta}{2(1-k^2)}} \tag{2}$$

where ω_p and ω_s are the primary side and secondary side angular resonant frequency. Due to the symmetric structure of primary side and secondary side, $\omega_p=\omega_s$ cn be obtained. k is the coupling coefficient between primary and secondary. The expression for Δ is shown in Eq. (3).

$$\Delta = \sqrt{(\omega_p^2 + \omega_s^2)^2 - 4(1-k^2)\omega_p^2\omega_s^2} \tag{3}$$

The system loss is mainly caused the parasitic resistors. Then, the primary side and secondary side efficiencies can be expressed as:

$$\eta_P = \frac{\dfrac{\omega^2 k^2 L_P L_S (R_S + R_L)}{(R_S + R_L)^2 + X_S}}{R_P + \dfrac{\omega^2 k^2 L_P L_S (R_S + R_L)}{(R_S + R_L)^2 + X_S}} \tag{4}$$

$$X_S = \omega L_S - \frac{1}{\omega C_S} \tag{5}$$

$$\eta_S = \frac{R_L}{R_S + R_L} \tag{6}$$

$$\eta = \eta_P \times \eta_S \tag{7}$$

where R_P and R_S re the primary and secondary resistances.

The main trade-offs for the coil design are voltage isolation, size, and system efficiency. With the aid of the ANSYS software, the coil parameters can be optimized.

The coupling capacitance of the coils can be modelled by using the paralleling copper plate.

$$C_{\text{couple}} = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{8}$$

where ε_r is the relative permittivity of the insulation material. In this case, air is used as the insulation material and ε_r=1 can be obtained. A is the overlapping area between the primary side and secondary side coils. d is the distance between two coils.

The estimated isolation capability of the system can be obtained by using Eq. (9) [23].

$$V_{\text{breakdown}} = \kappa t \tag{9}$$

where κ is the dielectric strength of the insulation material and t is the thickness. In this case, the thickness equal to the distance between two coils.

From the theoretical analysis, we can conclude that: 1) Large distance is preferred to achieve high voltage isolation and low coupling capacitance; 2) small distance is preferred to achieve high coupling and high efficiency operation; 3) small overlapping area is preferred for low coupling capacitance; 4) large overlapping area is preferred for high coupling. Design flow chart as shown in Fig. 4 is adopted to achieve the optimal design of the coils. In the design, the coil inner radius a, the number of turns N, and the coil distance d are selected as design variables. The copper width, pitch, and system operating frequency are predefined.

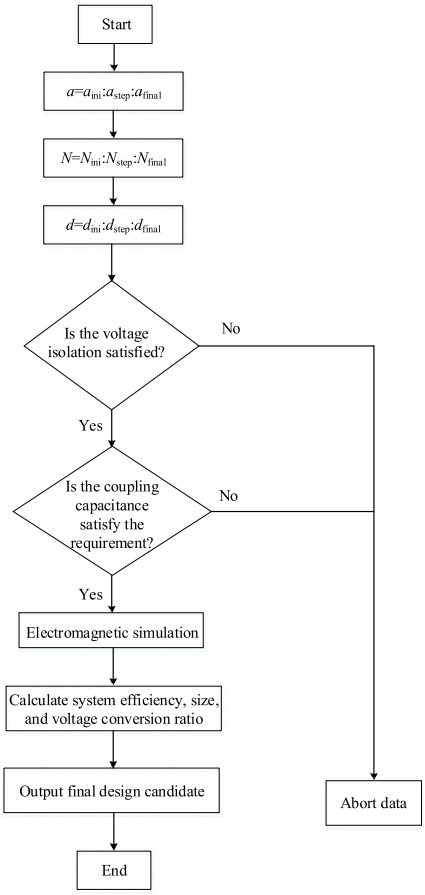


Fig. 4. Design flow chart for the coil.

Fig. 5 shows the electric filed simulation result. It can be seen that the maximum electric filed occurs inside the PCB coils, the FR4 epoxy material has large electric strength (20 MV/m). To reduce the coupling capacitance and common mode (CM) noise current, an EMI shielding layer is added to provide conduction path for CM current.

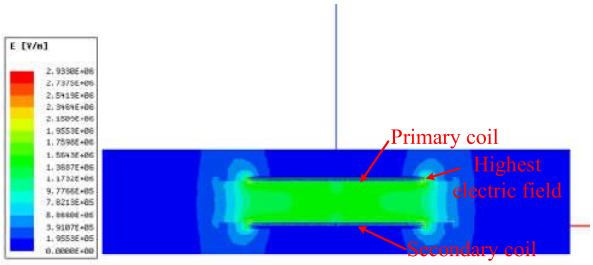


Fig. 5. Electric field simulation result.

The measurement results for the coil are summarized in Table I. The system switching frequency is designed at 2.5 MHz to achieve high efficiency conversion. Fig. 6 shows the measurement result of the coupling capacitance, a low coupling capacitance around 2 pF is achieved with an airgap of 15 mm.

TABLE I. MEASUREMENT RESULTS FOR THE DESIGNED COIL

a=1 mm, N=24, t=15 mm	
L_P/μH	11.98
C_P/pF	450
R_P/Ω	3.3887
L_S/μH	11.98
C_S/pF	3.388
Mutual inductance/μH	2.05
Coupling coefficient k	0.1767
Coupling capacitance/pF	2.0327

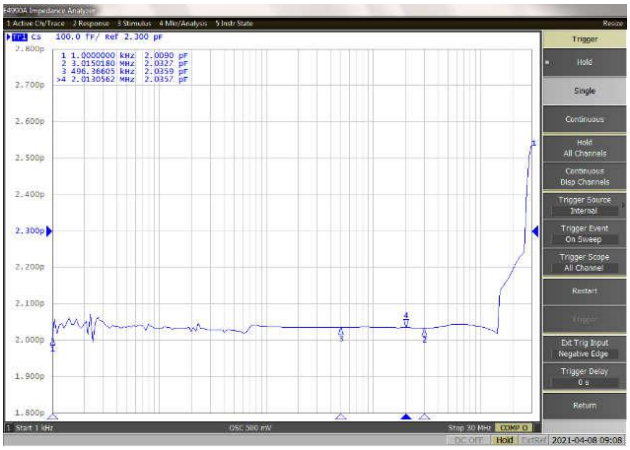


Fig. 6. Coupling capacitance measurement result with impedance analyzer.

III. Experiment Results and Discussions

Fig. 7 shows the overall gate driver power supply structure. The positive gate voltage is provided by the wireless power transfer and the negative voltage is generated through a non-isolated regulator. The secondary side PWM side is transmitted through optical fiber to achieve high voltage isolation and good EMI performance. The linear regulator VX7805-1000 from CUI Inc is selected, which has the following characteristics: 1) wide input voltage range: 8 V-26 V; 2) the maximum power is around 2.5 W. The gallium nitride (GaN) half-bridge driver (LMG5200) is used as the primary half-bridge inverter, which is capable of up to 10 MHz operation.

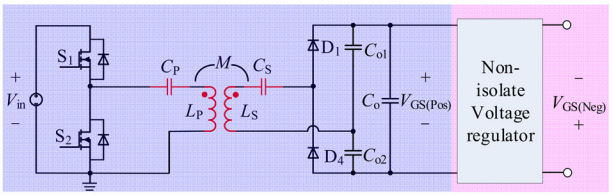
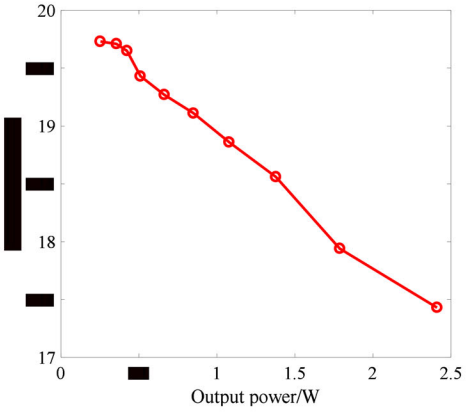
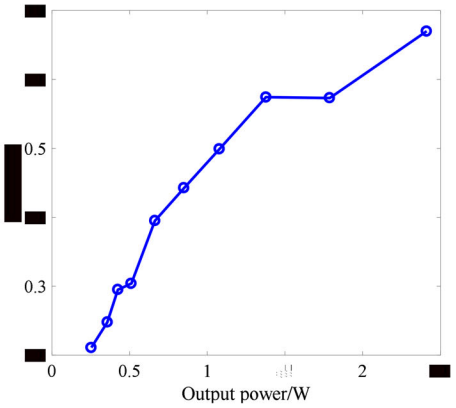


Fig. 7. The proposed medium voltage gate driver power supply structure.

Fig. 8 shows the wireless power transfer system output voltage and efficiency with different output power. The output voltage variation with output power is small (the largest variation is around 2.34 V), which makes open-loop operation of the power supply feasible and the maximum efficiency around 70% can be achieved for the system.



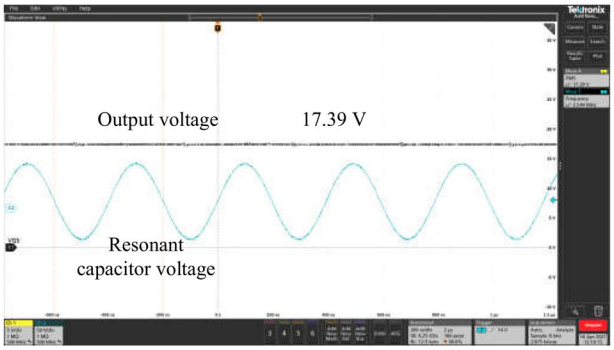
(a) Output voltage with different output power



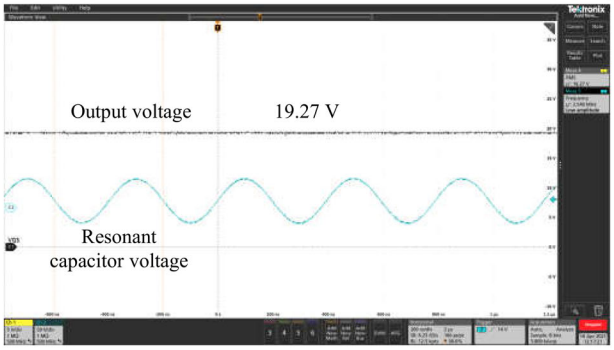
(b) Converter efficiency with different output power

Fig. 8. WPT system efficiency and output voltage with different output power.

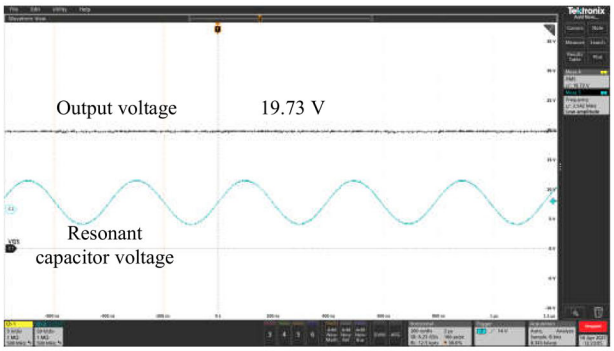
Fig. 9 shows the system output voltage experiment waveforms, where the system operating frequency is 2.5 MHz. The output voltage varies from 17.39 V to 19.73 V even with a large variation of load resistance. Therefore, open loop operation of the designed circuit is feasible.



(a) R_L=126 Ω



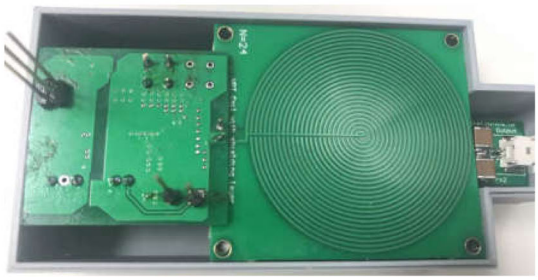
(b) R_L=460 Ω



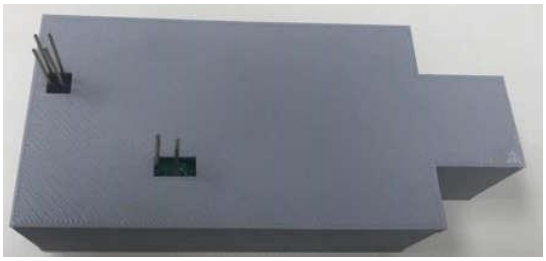
(c) R_L=1540 Ω

Fig. 9. Output voltage experiment waveforms under different load conditions.

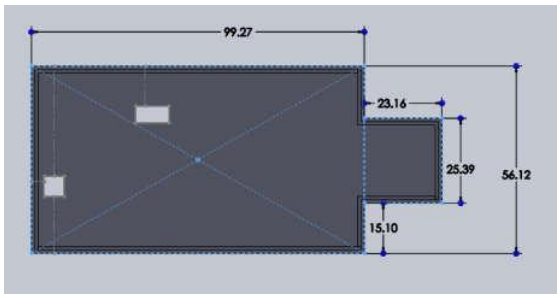
A 3D printed box as shown in Fig. 10 is designed to encapsulate the inductive power transfer based high voltage isolated power supply. The dimensions of the designed high voltage isolated power supply is shown in Fig. 10(c).



(a) 3D printed box for power supply with top side open



(b) 3D printed box for power supply with top side closed



(c) Dimensions in mm for the designed 3D printed box

Fig. 10. 3D printed box for the designed inductive power transfer based power supply for medium voltage gate driver.

To further validate the effectiveness of the WPT based medium voltage gate driver, a double pulse test (DPT) platform as shown in Fig. 11 is built. 1200 V/40 A SiC MOSFET SCT2080KE from ROHM is selected as device under test (DPT) to validate the operation of the designed gate driver.

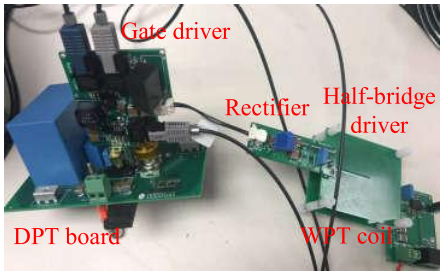


Fig. 11. Picture of the DPT test setup and designed WPT based gate driver.

Fig. 12 shows the gate driver output experiment waveform. The turn-on gate voltage is around 18 V, while the turn-off gate voltage is around -5 V, which can be used to drive medium voltage SiC MOSFET.

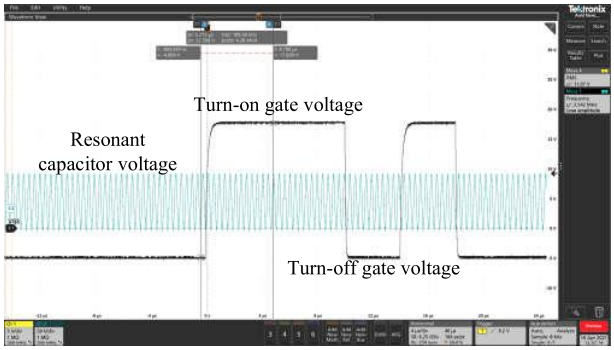
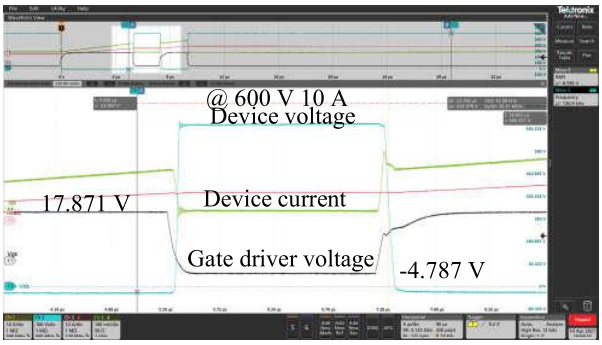
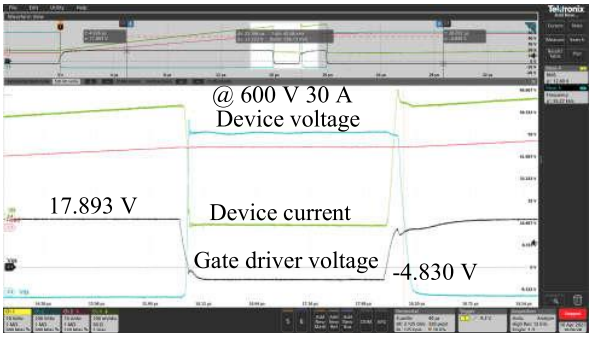


Fig. 12. Gate driver experiment waveform.

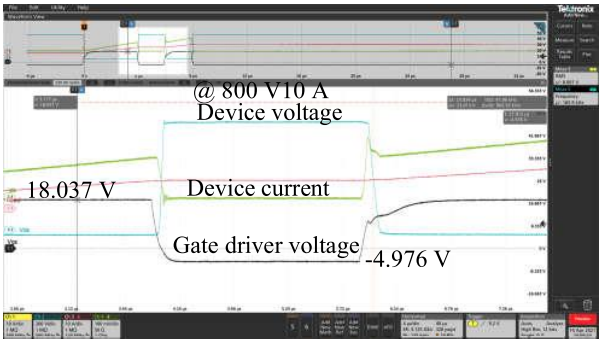
Fig. 13 shows the experiment waveforms under different conditions. It can be seen even with open loop operation, the gate voltage is almost constant at 18 V with small variations, which proves that the proposed gate driver can be designed with open loop to simplify the circuit and reduce the coupling capacitance caused by the feedback control.



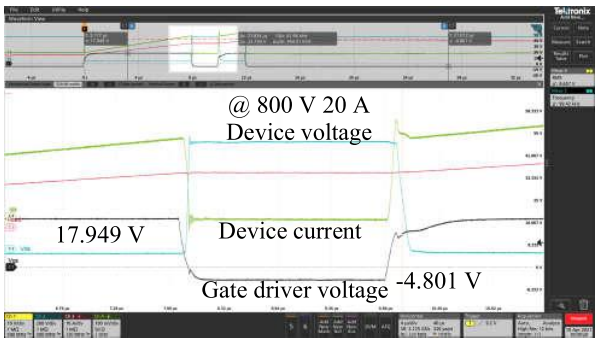
(a) DPT experiment waveform at 600 V and 10 A



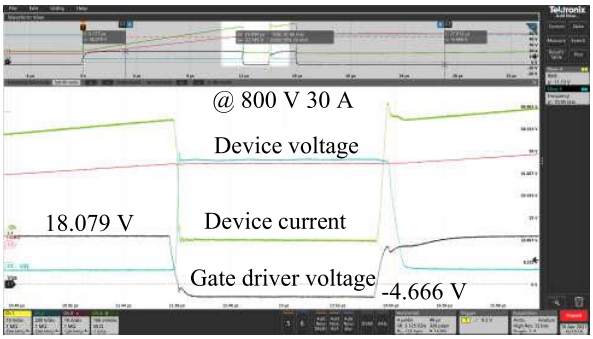
(b) DPT experiment waveform at 600 V and 30 A



(c) DPT experiment waveform at 800 V and 10 A



(d) DPT experiment waveform at 800 V and 20 A



(e) DPT experiment waveform at 800 V and 30 A

Fig. 13. Experiment waveforms under different operating conditions.

Isolation test for the designed power supply is performed by applying constant dc voltage on the primary side and secondary side. The system setup is shown in Fig. 14. The high voltage dc power supply FC30P4 with 30 kV maximum output from glassman is used to apply 20 kV voltage difference on the primary side and secondary side. As can be seen from Fig. 14, no leakage current can be observed during the test, which lasts for 10 minutes.

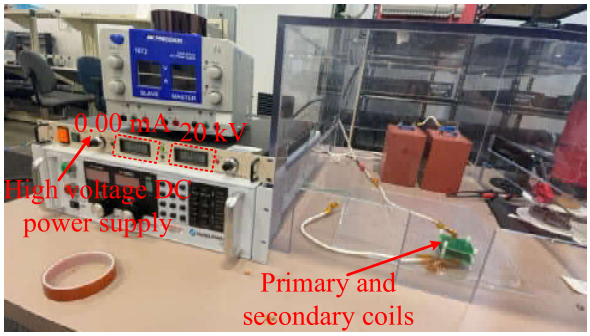


Fig. 14. Isolation test by applying constant dc voltage.

Fig. 15 shows the thermal performance of the designed gate driver at rated output power (2.5 W). The hottest part is the gallium nitride (GaN) half-bridge driver (LMG5200of the primary inverter, which is around 44 °C, which is far below than the maximum junction temperature 125 °C. Based on the characteristic of 10 kV power module (multiple dies in parallel operation), a higher power capability can be achieved with the proposed design.

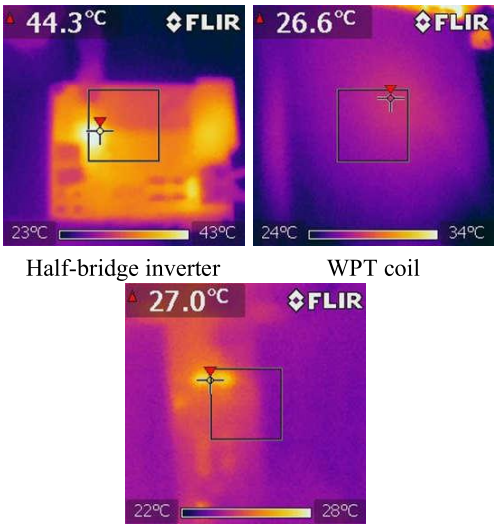


Fig. 15. Thermal performance of the WPT coil based power supply.

The designed power supply can also be modified to have two-output isolated voltages as shown in Fig. 16, which can be used to drive a half-bridge power module. The primary side inverter and coil are shared, which can reduce the number of components and power supply system size. Due to the large distance between two receivers, the coupling and corresponding influence between them is negligible.

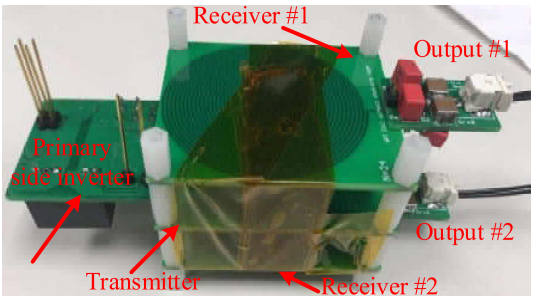


Fig. 16. Designed high voltage insulated power supply with two output channels.

IV. Conclusion

In this article, a WPT based gate driver for 10 kV SiC MOSFET application is presented. For 10 kV gate driver application, the isolation and coupling capacitance are the most important requirements. By operating the WPT system at a specific constant frequency, the system output voltage is independent of the load, which can be used for the gate driver power supply design with reduced complexity and coupling capacitance. Preliminary experiment results are presented to validate the effectiveness of the developed WPT based gate driver. The isolation test demonstrates the high voltage isolation characteristic of the designed power supply. Medium voltage test is the focus of future work.

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