Comprehensive Investigations on Paralleling Operation of SiC MOSFETs based on Subcircuit Model in MATLAB/SIMULINK

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2021 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia) | 978-1-6654-1851-5/21/$31.00 ©2021 IEEE | DOI: 10.1109/WIPDAASIA51810.2021.9656101

***Abstract*— Wide band gap (WBG) devices have been widely applied in industrial applications owning to their advantages of low switching loss, low on-stage voltage drop, and high operating temperature. Paralleling operation of power devices/modules is attractive due to its cost-effective and high power characteristics. In applications require very high current capability, paralleling operation of off-the-shelf power devices/modules becomes the only choice. However, current balancing operation of individual power device/module becomes difficult due to the differences of circuit parasitics. To investigate the device/module and circuit parasitics influences on the current sharing performance, in this article, a subcircuit model was built in MATLAB. Comprehensive comparisons and analysis are performed, which can provide guidance for engineers when designing the system with paralleling devices/modules. Moreover, the solutions to achieve current balancing operating are proposed with the aid of active gate driver. Experiment results are presented and analyzed to validate the effectiveness of current sharing solutions.**

Keywords—Wide band gap, current sharing, circuit parasitics, active gate driving

I. Introduction

Silicon carbide (SiC) metal–oxide–semiconductor field-effect transistor (MOSFET) enables the improvement of power converter efficiency and power density [1, 2]. It is also advantageous in paralleling operation owning to its positive temperature characteristic of on-state resistance. Nevertheless, paralleling operation is still challenging since the dynamic current sharing will become worse due to its negative temperature characteristic of threshold voltage [3]. In most of the papers, only the influences of on-state resistance and threshold voltage on current sharing performance are investigated. In practice, all circuit and device parasitics would have certain effect on the current sharing operation between paralleled power devices.

To mitigate the current unbalance operation, different solutions have been proposed in the literature. The passive components can be added into the circuits to alleviate the current unbalance issue. Although the static current unbalance can be mitigated with addition series resistor in the parallel branches, no improvement on the dynamic current balancing performance can be achieved with this method. Investigations can also be made on the symmetric parasitics design of the power module with multiple paralleling dies [4, 5]. The development cycle is long and the cost is high. The differential mode choke is inserted to achieve current balance operation [3]. However, the size and power loss of the inserted choke would be the major concerns especially at high power applications. Active gate driver is another promising technology to achieve current balancing operation among paralleled power devices [6]-[10]. As categorized in [1], the active gate driver for paralleling switches mainly include variable gate resistance, variable gate current, variable delay, and variable gate voltage. A multi-level active gate driving strategy is proposed for the paralleling operation of SiC power modules, where the individual module current information are obtained by detecting the voltage across the Kelvin source parasitic inductance [9, 10]. A complicate circuitry is required to achieve the functions. Moreover, this technique is limited for power devices/modules with Kelvin source terminal. In most of the literature, the static current unbalance is usually neglected due to positive characteristic of on-state resistance. Nevertheless, as analyzed in [3], the on-state resistance is less sensitive to the temperature. Therefore, it is also important to tackle the static current unbalance to improve the system reliability.

The device and circuit parasitics, including on-state resistance, threshold voltage, common source stray inductance, and switching loop stray inductance, effects on the current balancing operation are investigated in [12, 13]. However, there are other circuit parasitics can also affect the current balancing performance of paralleling operation of devices/modules. To fully understand the circuit and device parasitics influences on current sharing performance, all possible circuit and device parasitics are investigated and compared with the aid of the subcircuit model in MATLAB/SIMULINK. To make comparisons among different circuit parasitics influence on the current sharing operation, 20% mismatches for all parasitcis are assumed and simulated. The current error is plotted to demonstrate the effect of each parasitic. The theoretical analysis results can provide insights on the current sharing between paralleling devices. Moreover, to mitigate the current unbalance between paralleling devices/modules, a simple two-level active gate driving solution with adjustable turn-on voltage is proposed. The experiment results demonstrate the effectiveness of using adjustable turn-on voltage for current balancing operation. To further achieve both static and dynamic current sharing operation, a hybrid turn-on gate volatge and gate delay control strategy is discussed and the feasibility is approved by using simulation and subcircuit model.

The rest of the paper is organized as follows. The MATLAB based subcircuit model is briefly discussed in Section II. With the aid of the subcircuit model, the possible device and circuit parasitics influences on current sharing operation are investigated in Section III. The two-level active gate driving solutions are discussed in Section IV, and the experimental results are presented to validate the effectiveness. The simulation studies for a hybrid turn-on gate volatge and

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gate delay for SiC MOSFETs with paralleling operation are presented. Finally, conclusions are drawn.

II. Subcircuit Model for SIC MOSFET

In this work, the SiC MOSFET is modelled by using the conventional method, and its operation can be divided into off region, linear region and saturated region. Fig. 1 shows the subcircuit model of a SiC MOSFET [14].

$$I_{DS} = 0, V_{GS} < V_{th}, \text{ off region}$$

$$I_{DS} = \beta((V_{GS} - V_{th})V_{DS} - V_{DS}^2 / 2)(1 + \lambda |V_{DS}|),$$
$$0 < V_{DS} < V_{GS} - V_{th}, \text{linear region}$$

$$I_{DS} = \frac{\beta}{2}(V_{GS} - V_{th})^2 (1 + \lambda |V_{DS}|), 0 < V_{GS} - V_{th} < V_{DS},$$
$$\text{saturated region} \quad (1)$$

where β is the transistor gain, V_{th} is the threshold voltage, and λ is the channel modulation. These parameters can be extracted based on the transfer characteristic curve (I_{DS}-V_{GS}) provided by the manufacture datasheet.

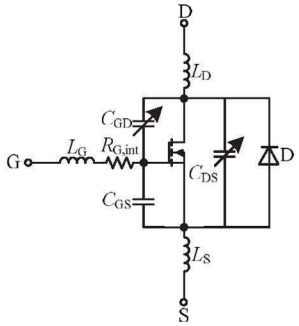


Fig. 1. Model of SiC MOSFET.

Fig. 2 shows the subcircuit model based double pulse test (DPT) circuit with two paralleling devices. Table 1 summarizes the circuit and device parasitics for two devices and assuming 20% difference for investigations, which can be caused by manufacture process or printed circuit board (PCB) layout. The device parasitics are obtained based on the manufacture datasheet. The device parasitic capacitances are modelled by using linearization method, and multiple capacitance values under different drain-to-source voltages are selected.

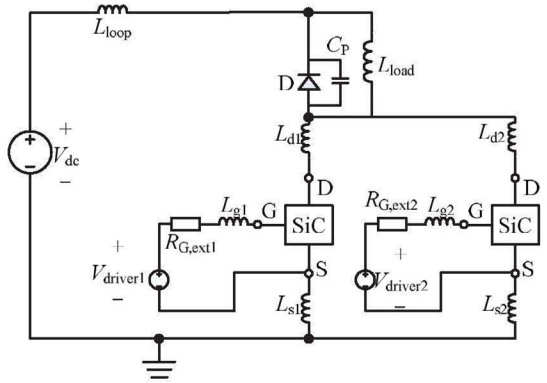


Fig. 2. DPT circuit model with two paralleling devices.

TABLE I. CIRCUIT PARASITICS AND THEIR VALUES

Variable	Definition	Values for device 1	Values for device 2
$R_{G,ext1}$, $R_{G,ext1}$	Gate driver resistor	24 Ω/6 Ω	20 Ω/5 Ω
$R_{G,int}$, $R_{G,int}$	Device internal gate resistor	1.2 Ω	1 Ω
L_{g1}, L_{g2}	Gate loop parasitic inductance introduced by gate driver	12 nH	10 nH
L_{G1}, L_{G2}	Gate terminal parasitic inductance due to package	11.04 nH	9.2 nH
L_{s1}, L_{s2}	Parasitic inductance from source terminal to ground	6 nH	5 nH
L_{S1}, L_{S2}	Source terminal parasitic inductance due to package	12 nH	10 nH
L_{d1}, L_{d2}	Parasitic inductance from drain terminal to freewheeling diode	6 nH	5 nH
L_{D1}, L_{D2}	Drain terminal parasitic inductance due to package	7.32 nH	6.1 nH
V_{th1}, V_{th2}	Threshold voltage	6.24 V	5.2 V
C_{iss1}, C_{iss2}	Input capacitance	[960 840 624 600 576] pF for [0 1 10 100 800] V	[800 700 520 500 480] pF for [0 1 10 100 800] V
C_{rss1}, C_{rss2}	Reverse transfer capacitance	[504 372 120 36 21.6] pF for [0 1 10 100 800] V	[420 310 100 30 18] pF for [0 1 10 100 800] V
C_{oss1}, C_{oss2}	Output capacitance	[1020 780 312 86.4 43.2] pF for [0 1 10 100 800] V	[850 650 260 72 36] pF for [0 1 10 100 800] V
β_1, β_2	Gain (Related with device on-state resistance)	0.28392	0.2366

III. Parasitics Influences on Current Sharing Performance

When investigating the individual parasitic influence on current sharing performance, the other parasitics are kept same for the two paralleled devices. The test condition is fixed at 400 V and 10 A for all the scenarios.

A. Device Parasitic-Interal Gate Resistor

Due to the manufacture process, the internal gate resistor may not consistent for the devices with the same part number. Fig. 3 shows the results with internal gate resistor mismatch. The maximum current difference is 0.6308 A, and the influence of internal gate resistor is not obvious. Meanwhile, the internal gate resistor will mainly affect the dynamic stages with negligible influence on the steady state. The current sharing performance is still good with the internal gate resistor mismatch.

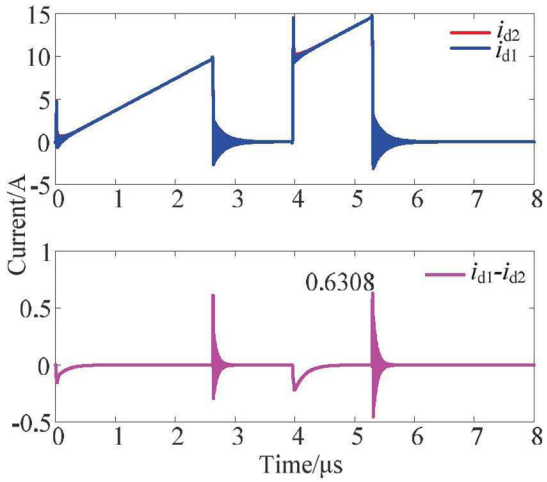


Fig. 3. Current sharing performance with internal gate resistor mismatch.

B. Device Parasitic-Threshold Voltage

The threshold voltage mismatch can also be caused by manufacture process or the degradation of device. Fig. 4 shows the results with threshold voltage mismatch. The maximum current difference is 2.954 A, the influence of threshold voltage is large. The device with a lower threshold voltage will turn-on fast and has higher current. In addition, the threshold voltage has a negative temperature characteristic so that the threshold voltage mismatch should be avoided in the real application. A large current unbalance is observed during the dynamic processes, especially during turn-on process.

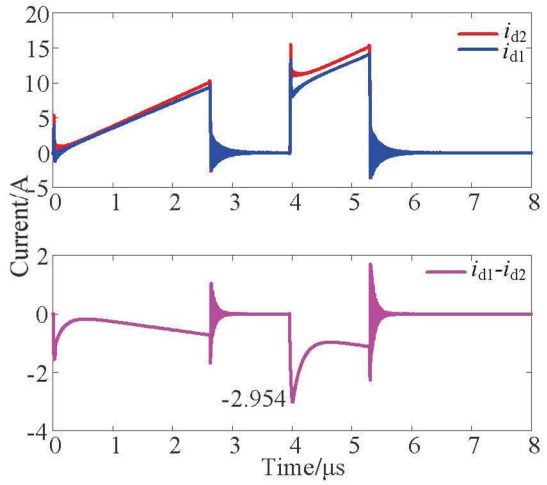
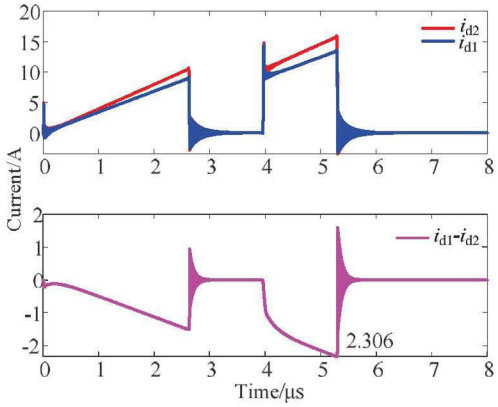


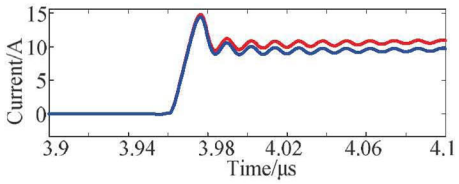
Fig. 4. Current sharing performance with threshold voltage mismatch.

C. Device Parasitic-Gain (Related with Device On-state Resistance)

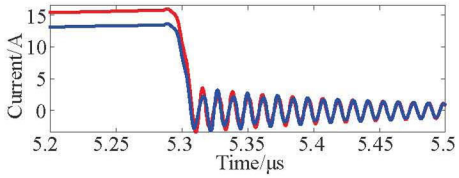
Fig. 5 shows the current sharing performance with on-state resistance mismatch. From the result one can observe that the on-state resistance will mainly affect the static current sharing performance, while its influence on dynamic current sharing performance is negligible. The maximum current difference is around 2.306 A.



(a) Overall current sharing waveform



(b) Zoomed-in current sharing waveform during turn-on process



(c) Zoomed-in current sharing waveform during turn-off process

Fig. 5. Current sharing performance with on-state resistance mismatch.

D. Device Parasitic-Gate Terminal Parasitic Inductance

Fig. 6 shows the current sharing performance with gate terminal parasitic inductance mismatch. The maximum current difference is around 0.3178 A. The gate terminal parasitic inductance has small influence on the current sharing performance.

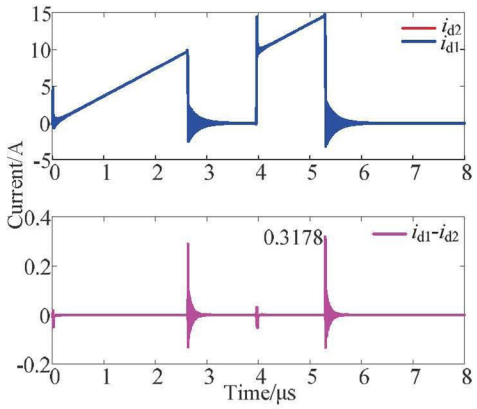


Fig. 6. Current sharing performance with gate terminal inductance mismatch.

E. Device Parasitic-Drain Terminal Parasitic Inductance

Fig. 7 shows the current sharing performance with drain terminal parasitic inductance mismatch. The maximum current difference is around 0.1792 A.

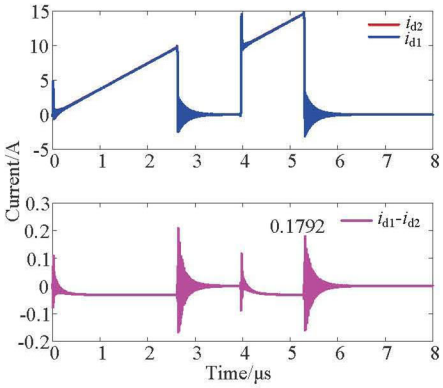
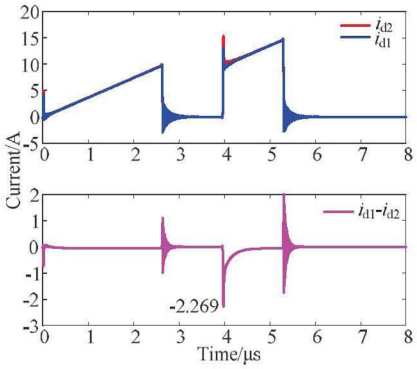


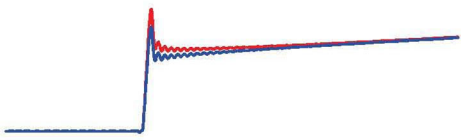
Fig. 7. Current sharing performance with drain terminal inductance mismatch.

F. Device Parasitic-Source Terminal Parasitic Inductance

Fig. 8 shows the current sharing performance with source terminal parasitic inductance mismatch. The maximum current difference is around 2.269 A. Compared with drain terminal parasitic inductance, the source terminal parasitic inductance has large influence on the current sharing performance. The major reason is that the source terminal inductance is also included in the gate loop, which will affect the gate voltages on each device and the dynamic current sharing performance.



(a) Overall current sharing waveform



(b) Zoomed-in current sharing waveform during turn-on process

Fig. 8. Current sharing performance with source terminal inductance mismatch.

G. Device Parasitic-Input Capacitance

Fig. 9 shows the current sharing performance with input capacitance mismatch. The dynamic switching speed is closely related with the input capacitance. A large input capacitance will lead to slow switching speed. Thus, the maximum current difference of 2.002 A is seen during the turn-on process.

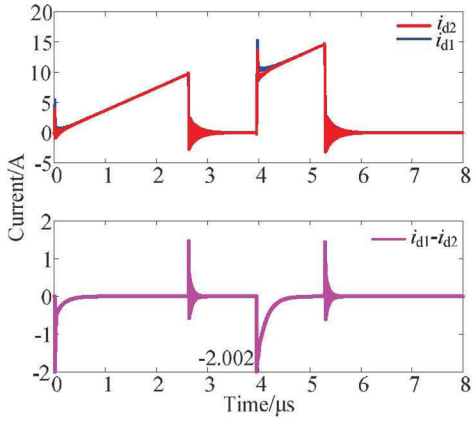


Fig. 9. Current sharing performance with input capacitance mismatch.

H. Device Parasitic-Reverse Transfer Capacitance

Fig. 10 shows the current sharing performance with revere transfer capacitance mismatch, which would also affect the dynamic switching process. The maximum current difference is around 3.783 A.

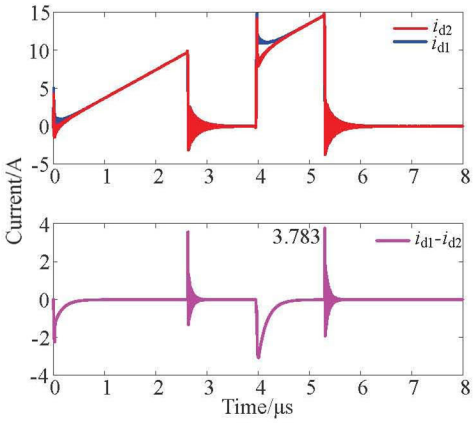


Fig. 10. Current sharing performance with reverse transfer capacitance mismatch.

I. Device Parasitic-Output Capacitance

Fig. 11 shows the current sharing performance with output capacitance mismatch. The device turn-off process is mainly affected by the output capacitance. The maximum current difference is during the turn-off process, which is around 1.476 A.

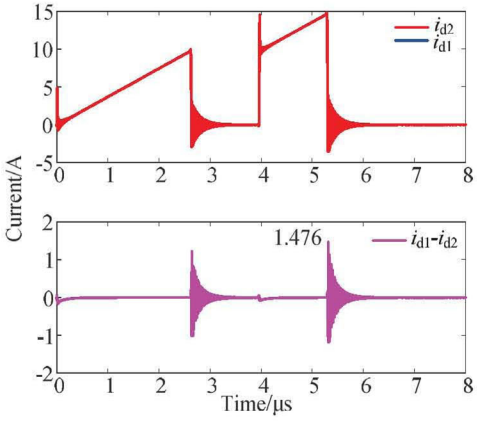


Fig. 11. Current sharing performance with output capacitance mismatch.

J. Circuit Parasitic-Turn-on Gate Resistor

Fig. 12 shows the current sharing performance with turn-on gate resistor mismatch. Clearly, the turn-on switching speed is greatly affected by the turn-on gate resistor. The maximum current difference is around 4.154 A, which occurs during the turn-on process.

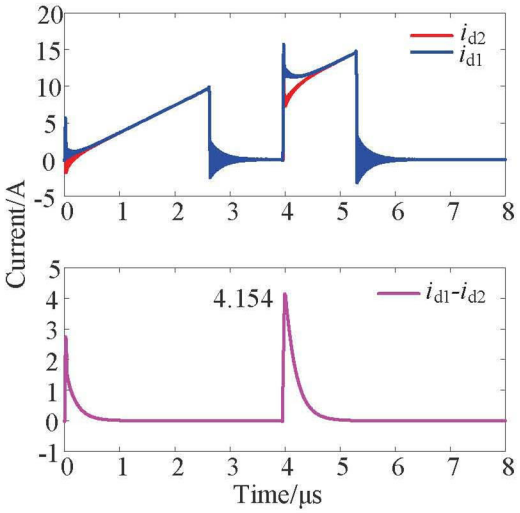
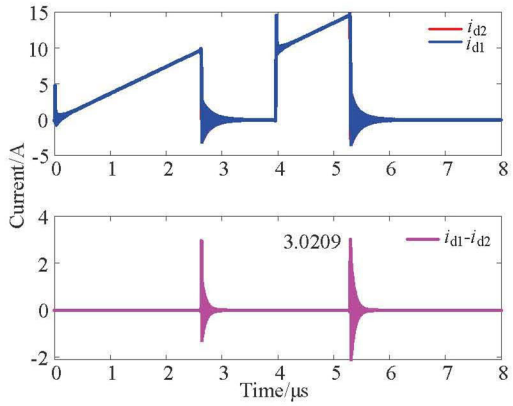


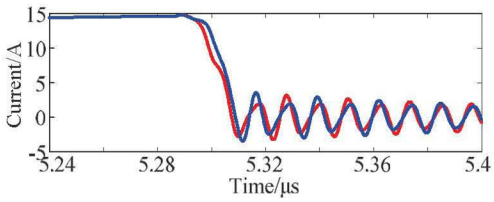
Fig. 12. Current sharing performance with turn-on gate resistor mismatch.

K. Circuit Parasitic-Turn-off Gate Resistor

Fig. 13 shows the current sharing performance with turn-off gate resistor mismatch. It can be seen that mainly the turn-off process is affected by the turn-off gate resistor mismatch. The maximum current difference is around 3.0209 A.



(a) Overall current sharing waveform



(b) Zoomed-in current sharing waveform during turn-off process

Fig. 13. Current sharing performance with turn-off gate resistor mismatch

L. Circuit Parasitic-Gate Loop Parasitic Inductance

Fig. 14 shows the current sharing performance with gate loop parasitic inductance mismatch. This mismatch can be caused by the asymmetric layout of gate drivers. For the gate loop parasitic inductance, only the dynamic current sharing performance is affected. The maximum current difference is around 0.6958 A.

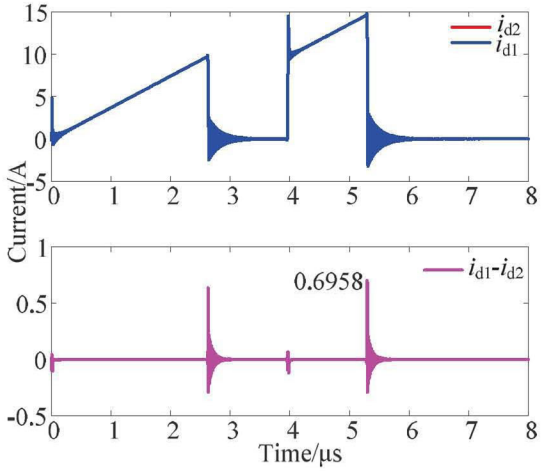


Fig. 14. Current sharing performance with gate loop parasitic inductance mismatch.

M. Circuit Parasitic- Parasitic Inductance from Drain Terminal to Freewheeling Diode

Fig. 15 shows the current sharing performance with circuit drain terminal parasitic inductance mismatch. This mismatch can be caused by the asymmetric layout of PCB. The maximum current difference is around 0.1649 A.

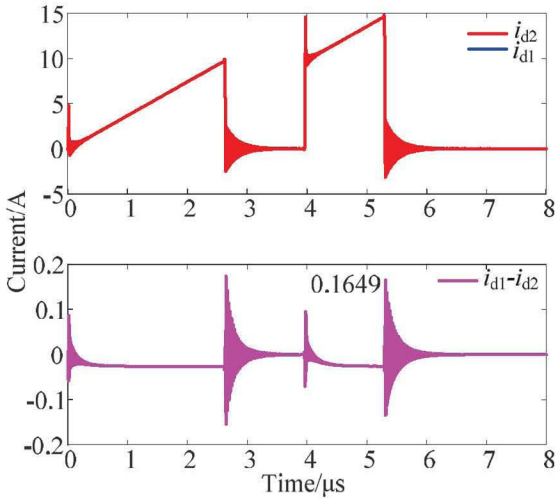


Fig. 15. Current sharing performance with circuit drain terminal parasitic inductance mismatch.

N. Circuit Parasitic- Parasitic inductance from source terminal to ground

Fig. 16 shows the current sharing performance with common circuit source parasitic inductance mismatch. This mismatch can be caused by the asymmetric layout of PCB. The maximum current difference is around 0.1482 A.

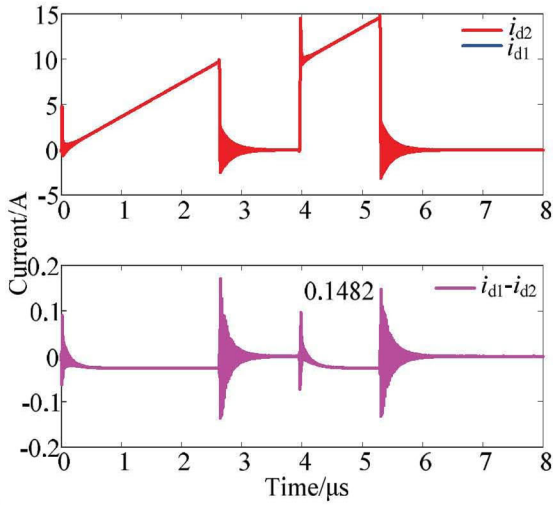


Fig. 16. Current sharing performance with circuit source terminal parasitic inductance mismatch.

Fig. 17 summarizes the parasitics influences on current sharing performance. From Fig. 17, we can observe that to achieve a good current sharing operation, several special considerations should be made: 1) when select the gate resistors, the resistance tolerance should be small so that the variations between each gate driver is minimized. In addition, the gate resistors should also have a stable temperature performance; 2) the common source parasitic inductance should be minimized since it is included in both gate loop and power loop, the device package with kelvin source can alleviate the current unbalance caused by the common source parasitic inductance ; 3) the on-state resistance mismatch and threshold voltage mismatch are the major reasons for the unbalanced device currents. Although efforts can be made to mitigate these parasitics mismatches, it is impossible to achieve identic parasitics for individual devices. In addition, the circuit parasitics are also difficult to be identic when more power devices are in parallel. Therefore, solutions are still required to mitigate the current unbalance.

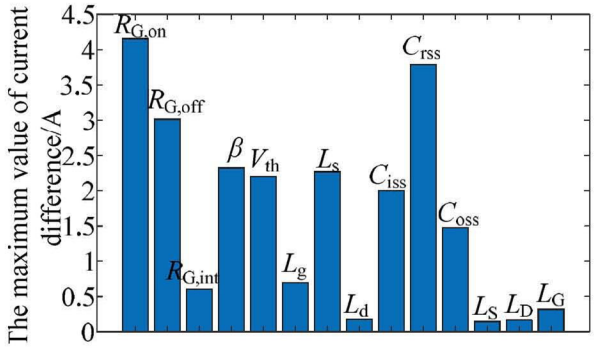


Fig. 17. Current sharing performance comparisons among different circuit parasitics.

IV. Active Gate Driving Method to Mitigate the Current Sharing Performance

According to [10], in the saturation region, the SiC MOSFET current can be modelled as Eq. (2). The mismatches of the dynamic current among different paralleled power devices are caused by the threshold voltage mismatches.

$$i_{dsj}=g_{fs}(v_{gsj}-v_{thj})^2, v_{gsj} > v_{thj} \quad (2)$$

Therefore, to compensate the difference of threshold voltage, different gate voltages can be applied for the individual devices/modules. In addition to the threshold voltage mismatch, the unbalanced transient current caused by other circuit mismatches can also be compensated by the gate volatge. The difficulties of active gate driver with adjustable turn-on voltage including: 1) adjustable turn-on gate voltage circuit design; and 2) current monitor circuit design. This work simply focus on the adjustable turn-on gate voltage circuit design. For medium voltage SiC MOSFET, like 3.3 kV and 10 kV SiC MOSFETs, gate driver with high insulated power supply is required. In this research, a wireless power transfer based high voltage insulated power supply is designed for medium voltage SiC MOSFETs. Fig. 18 shows the circuit topology of the gate driver power supply. The positive turn-on gate voltage is generated by wireless power transfer converter and the negative turn-off gate voltage is generated by a non-isolated dc/dc converter with a regulated -5 V output voltage in a wide input voltage range. Fig. 19 shows the picture of the experiment setup. By adjusting the switching frequency of primary inverter, the turn-on gate voltage can be adjusted accordingly.

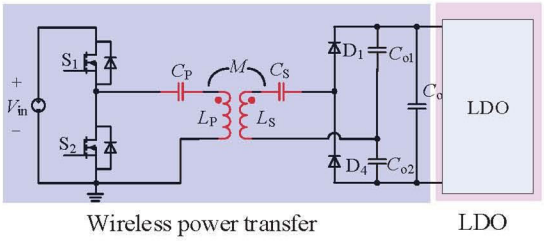
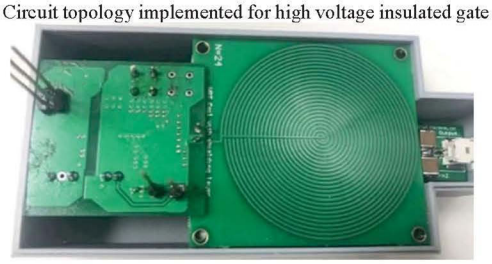
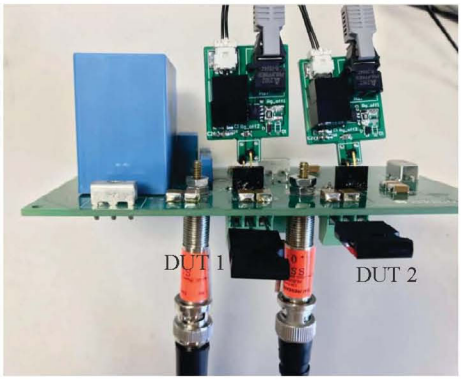


Fig. 18. Circuit topology implemented for high voltage insulated gate driver.

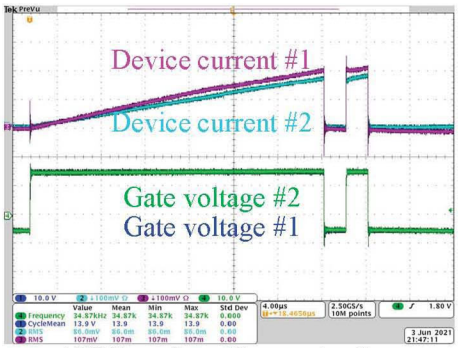


(a) Wireless power transfer converter

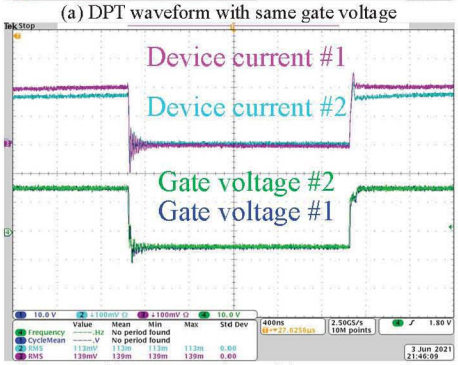


(b) DPT setup with paralleling SiC MOSFETs

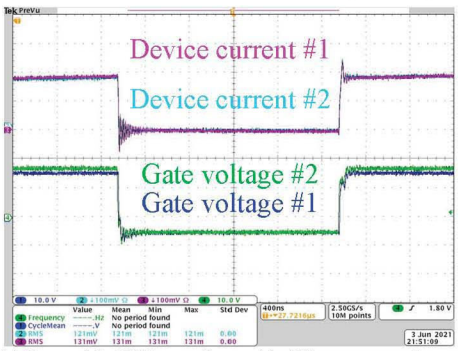
Fig. 19. Experiment setup.



(a) DPT waveform with same gate voltage



(b) Zoomed-in DPT waveform with same gate voltage



(c) Zoomed-in DPT waveform with different gate voltages

Fig. 20. DPT experiment waveforms with same and different gate voltages.

Fig. 20(a) and Fig. 20(b) show the DPT waveforms with same gate voltage for two paralleling devices. Current unbalance exists due to the asymmetric parasitics. Fig. 20(c) shows the DPT waveform with different gate voltages. As can be seen from Fig. 20(b), device 1 turns on faster than device 2. In order to achieve current sharing, the turn-on gate voltage for device 2 can be increased as show in Fig. 20 (c). A well current sharing can be achieved by using adjustable turn-on gate voltage.

V. Hybrid Turn-on Gate Voltage and Gate Delay Strategy for Paralleling Operation

Although the variable turn-on gate voltage can mitigate the threshold voltage mismatch or other parasitics mismatches, the static current sharing operation is affected at the same time. As discussed in [13], the on-state resistance is sensitive to the gate voltage. To decouple between the dynamic current sharing and static current sharing, a hybrid turn-on gate voltage and gate delay control strategy can be adopted. The basic idea is that during the dynamic process, the gate delays between paralleled devices are adjusted to achieve dynamic current sharing, while the turn-on gate voltages are adjusted for the purpose of static current sharing caused by the mismatch of on-state resistance. Please note that in the existing literature, the static current sharing is not discussed and only the positive temperature characteristic of on-state resistance is used to achieve current sharing operation. However, as analyzed in [13], when compared with its Si counterpart, the on-state resistance of SiC MOSFET is less sensitive to the temperature. Thus, static current balancing strategy is also required.

Based on the previous discussions, the threshold voltage and on-state resistance are set different between two paralleled power devices. Fig. 21 shows the simulation results with the same gate driver. Both the static and dynamic currents are unbalance. Fig. 22 shows the simulation waveforms with variable gate volatge. Although the dynamic current sharing operation is achieved, the static current unbalance still exists. Fig. 23 shows the hybrid gate voltage and gate delay control strategy, both the turn-on and turn-off delays, and the gate voltage are adjusted to achieve current sharing operation.

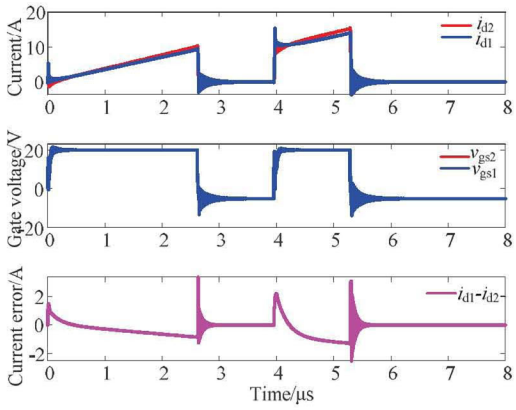
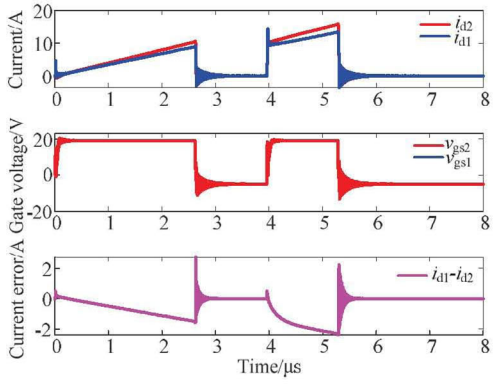
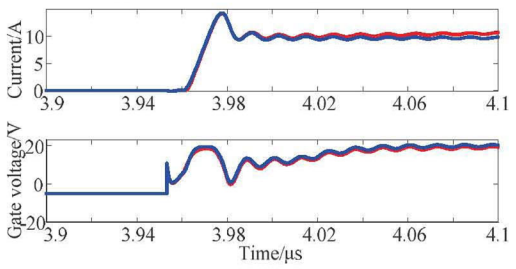


Fig. 21. Simulation t waveforms with the same gate driver.

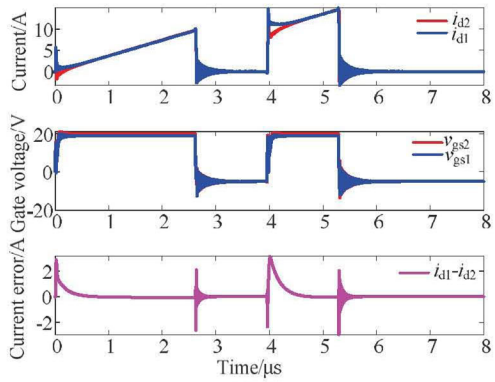


(a) Overall current sharing waveform

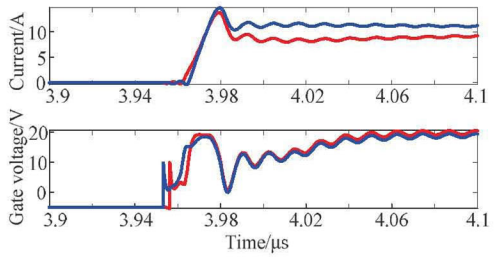


(b) Zoomed-in current sharing waveform during turn-on process

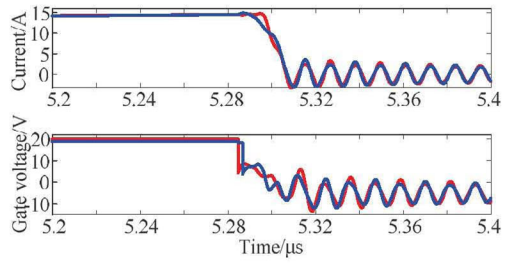
Fig. 22. Simulation t waveforms with the variable gate volatge gate delay control strategy.



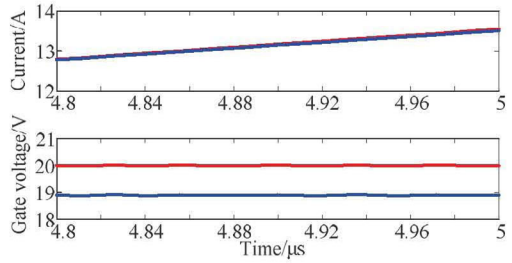
(a) Overall current sharing waveform



(b) Zoomed-in current sharing waveform during turn-on process



(c) Zoomed-in current sharing waveform during turn-off process



(d) Zoomed-in current sharing waveform during steady state condition

Fig. 23. Simulation t waveforms with the proposed hybrid gate volatge gate delay control strategy.

VI. Conclusions

In this work, the current sharing performance of paralleling devices/modules are investigated based on the subcircuit model in MATLAB. Each possible device and circuit parasitics are considered and comparisons are presented. To mitigate the current unbalance, an adjustable turn-on gate voltage solution is proposed. By adjusting the switching frequency of the primary inverter on the isolated gate driver power supply, the output volatge is regulated. The experiment results demonstrate the effectiveness of using adjustable turn-on gate voltage for the current sharing operation of paralleling devices. The hybrid gate voltage and gate delay control strategy is proposed and verified by simulation studies.

Acknowledgment

This material is based upon work supported by the National Science Foundation under Grant No. 1939144, GRID Connected Advanced Power Electronics Systems (GRAPES), Project GR-21-06.Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the National Science Foundation.

References

[1] S. Zhao, X. Zhao, Y. Wei, Y. Zhao and H. A. Mantooth, "A Review on Switching Slew Rate Control for Silicon Carbide Devices using Active Gate Drivers," IEEE Journal of Emerging and Selected Topics in Power Electronics, doi: 10.1109/JESTPE.2020.3008344.

[2] S. Zhao, X. Zhao, A. Dearien, Y. Wu, Y. Zhao and H. A. Mantooth, "An Intelligent Versatile Model-Based Trajectory-Optimized Active Gate Driver for Silicon Carbide Devices," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 429-441, Mar. 2020.

[3] Z. Zeng, X. Zhang and Z. Zhang, "Imbalance Current Analysis and Its Suppression Methodology for Parallel SiC MOSFETs with Aid of a Differential Mode Choke," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1508-1519, Feb. 2020.

[4] S. K. Singh, N. K. Pilli, F. Guedon, and R. Mcmahon, "PMSM drive using silicon carbide inverter: Design, development and testing at elevated temperature," in *Proc. IEEE Int. Conf. Ind. Technol.*, Mar. 2015, pp. 2612–2618.

[5] H. Li, S. Munk-Nielsen, S. Beczkowski, and X. Wang, "A novel DBC layout for current imbalance mitigation in SiC MOSFET multichip power modules," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8042–8045, Dec. 2016.

[6] Y. Xue *et al.*, "A compact planar Rogowski coil current sensor for active current balancing of parallel-connected silicon carbide MOS FETs," in *Proc. of IEEE Energy Convers. Congr. Expo.*, Sep. 2015, pp. 4685–4690.

[7] Z. Zhang, J. Dix, F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert,"Intelligent gate drive for fast switching and crosstalk suppression of SiC devices," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9319–9332, Dec. 2017.

[8] S. Kokosis, I. Andreadis, G. Kampitsis, P. Pachos, and S. Manias, "Forced current balancing of parallel connected SiC JFETs during forward and reverse conduction mode," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1400–1410, Feb. 2017.

[9] Y. Yang, Y. Wen and Y. Gao, "A Novel Active Gate Driver for Improving Switching Performance of High-Power SiC MOSFET Modules," IEEE Transactions on Power Electronics, vol. 34, no. 8, pp. 7775-7787, Aug. 2019.

[10] Y. Wen, Y. Yang and Y. Gao, "Active Gate Driver for Improving Current Sharing Performance of Paralleled High-Power SiC MOSFET Modules," IEEE Transactions on Power Electronics, vol. 36, no. 2, pp. 1491-1505, Feb. 2021.

[11] Y. Mao, Z. Miao, C. Wang and K. D. T. Ngo, "Passive Balancing of Peak Currents Between Paralleled MOSFETs With Unequal Threshold Voltages," *IEEE Trans. on Power Electron.*, vol. 32, no. 5, pp. 3273-3277, May 2017.

[12] H. Li, S. Beczkowski, S. M. Nielsen, R. Maheshwari, and T. Franke, "Circuit mismatch and current coupling effect influence on paralleling SiC MOSFETs in multichip power modules," in *Proc. IEEE PCIM Europe*, 2015, pp. 1–8.

[13] G. Wang, J. Mookken, J. Rice and M. Schupbach, "Dynamic and static behavior of packaged silicon carbide MOSFETs in paralleled applications," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, 2014, pp. 1478-1483.

[14] V. Talesara et al., "Dynamic Switching of SiC Power MOSFETs Based on Analytical Subcircuit Model," *IEEE Trans. on Power Electron.*, vol. 35, no. 9, pp. 9680-9689, Sept. 2020.