Multi-level Active Gate Driver for SiC MOSFETs with Paralleling Operation

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***Abstract*—Wide band gap (WBG) devices, like silicon carbide (SiC) MOSFET has gradually replaced the traditional silicon counterpart due to their advantages of high operating temperature and fast switching speed. Paralleling operations of SiC MOSFETs are unavoidable in high power applications in order to meet the system current requirement. However, parasitics mismatches among different paralleling devices would cause current unbalance issues, which would reduce the system reliability and maximum current capability. Thus, to achieve current balancing operation, this paper proposes a solution of using multi-level active gate driver, where the dynamic current sharing during turn-on and turn-off processes are achieved by adjusting the delays, intermediate turn-on and turn-off voltages. The static current sharing is maintained by regulating the static turn-on gate voltage, where the on-state resistance mismatch between different devices can be compensated. A double pulse test setup with two different SiC MOSFETs is built to emulate the scenario of worst case application with large differences of threshold voltage and on-state resistance. The experimental results demonstrate that the proposed active gate driver can achieve both dynamic and static current sharing operations for SiC MOSFETs with paralleling operation. Moreover, the system control diagram is discussed. Simulation studies are conducted to achieve closed-loop control of the paralleled SiC MOSFETs with the aid of the active gate driver approach.**

Keywords*—SiC MOSFET, active gate driver, paralleling operation

I. Introduction

Wide band gap (WBG) devices with outstanding performances have been widely used to replace the traditional technologies [1]-[3]. Both the system efficiency and power density can be improved by using silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) when compared with their silicon counterparts.

In medium and high power applications, due to the limitation of chip size, paralleling operations of power devices/modules are unavoidable to meet the system current requirement [4, 5].

However, due to the manufacture and operation conditions, the device parameters can vary for those paralleled devices [6]. Threshold voltage and on-state resistance are two of the most important parameters that affect the current sharing performances [6, 7]. Specifically, the threshold voltage will affect the dynamic current sharing performance, while the on-state resistance will affect the static current sharing performance. Different methodologies have been proposed to achieve current sharing operations. These methods can be mainly categorized into the following three groups: 1) novel package technology; 2) inserting passive components; 4) active gate driver.

A novel direct bond copper (DBC) layout technology is proposed in [8] to mitigate the current unbalance in the SiC power modules with multiple dies in paralleling operation. The cost and reliability issues make this solution not attractive. The passive methods are simple to be implemented, while the size of the components and power loss are not unneglectable when considering the high power applications. The drive-source resistors and coupled power-source inductors are inserted to achieve dynamic current sharing [9]. However, the static current sharing cannot be achieved. A differential mode choke is inserted into the paralleling branches to achieve dynamic current sharing [10]. However, the large size of the core and the associated power loss make this solution unattractive.

The gate resistance and delay time can be adjusted to achieve dynamic current sharing for power devices with paralleling operation [11]. However, the static current sharing performance cannot be improved. To compensate the threshold voltage mismatch, the variable turn-on gate voltage method is proposed, where different gate voltages are applied for different devices [12]. In [13], the turn-on/turn-off edges are aligned by adjusting the delays, while the turn-on/turn-off slopes are controlled by the duration of an intermediate gate voltages. Although the dynamic current sharing can be achieved, all the existing solutions fail to achieve good static current sharing operation.

Thus, the main objective of this paper is to propose an active gate driver to achieve both static and dynamic current sharing operations. For the proposed active gate driver, there existing four voltage levels, which provides enough control freedoms. The static current sharing operation is ensured by adjusting the turn-on gate voltages for the paralleling devices, while the dynamic current sharing operation is achieved by adjusting the intermediate turn-on/turn-off gate voltages and delays. Another benefit of the proposed active gate driver is that it can achieve both current sharing operation and slew rate control. Two different SiC MOSFETs with different on-state resistances and threshold voltages are paralleled to validate the effectiveness of the proposed method.

The rest of this paper is organized as follows. Section II discusses the origins of the current unbalance for SiC MOSFETs with paralleling operations. The operational principles and circuit design of the proposed method are discussed in Section III and Section IV, respectively. Section V presents the experiment results. Section VI discusses the

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system structure for the paralleled medium voltage SiC devices and the closed-loop simulation results. Finally, conclusions are drawn in Section VII.

II. Problem Statement for SiC MOSFETs with Paralleling Operation

Due to the manufacture process, certain variations of the parameters exist for the device with the same part number. Among these parameters, the most important two parameters for the device with paralleling operation are on-state resistance and threshold voltage. When the gate voltage reaches the threshold voltage, the device is turned on and during the turn-on process, the current flows through the device can be expressed as Eq. (1) [14]. It can be observed that for the device with a small threshold voltage will turn-on first and the current flows through this device is larger than other devices during the turn-on process. Please note that the transferconductance can be regarded as a constant.

$$i_{ds} = g_{fs}(v_{gs} - v_{th})^2 \tag{1}$$

Fig. 1 shows the static equivalent circuit for two SiC MOSFETs in paralleling operation. The current distribution among the paralleling devices is determined by the ratio of device on-state resistances. Thus, the static current unbalance is mainly caused by the mismatch of device on-state resistance. Although the device on-state resistance has positive temperature characteristic, which is beneficial for the static current sharing operation, the on-state resistance is less sensitive to the temperature when compared with its Si counterpart [10].

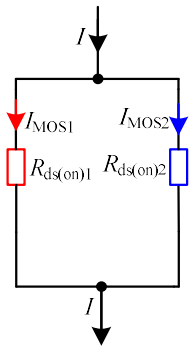
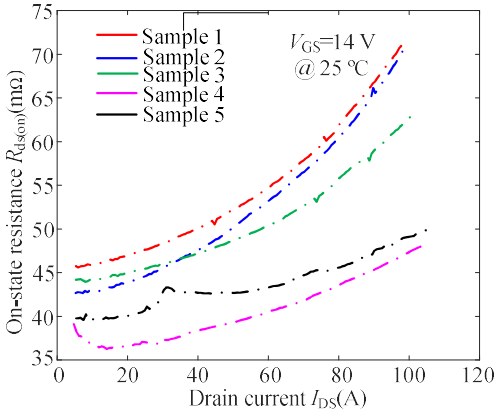
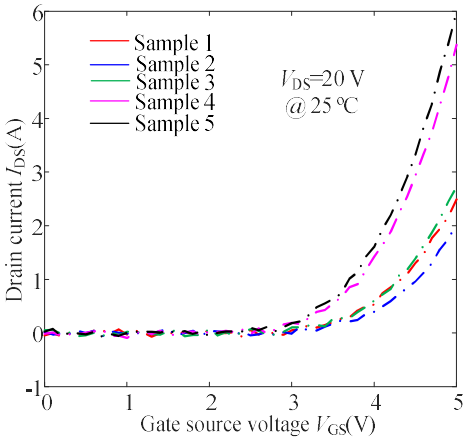


Fig. 1. Equivalent circuit during the steady state.

Five SiC MOSFETs with the same part number have been characterized with curve tracer. The device on-state resistance and threshold voltage variation are demonstrated in Fig. 2. Due to the large variation of the on-state resistance, it would be insufficient to rely on the positive temperature characteristic to achieve static current sharing. Threshold voltage variation is also observed for these samples as shown in Fig. 2(b).



(a) On-state resistance



(b) Threshold voltage

Fig. 2. Static characterization results for the samples.

III. Feasibility Analysis of the Proposed Active Gate Driving Method for SiC MOSFETs with Paralleling Operation

Based on the problem statement, to tackle the current unbalance issue, a variable multi-level gate voltage profile as shown in Fig. 3 is desired. The turn-on gate voltage V_{on2} can be used to compensate the threshold voltage mismatch and achieve dynamic current sharing during turn-on process. The feasibility is proved in Eq. (1). In addition to the threshold voltage mismatch, the dynamic current unbalance caused by the parasitic mismatch can also be compensated by the turn-on gate voltage V_{on2}. Similarly, the turn-off gate voltage V_{off} is selected to achieve current sharing during the turn-off stage.

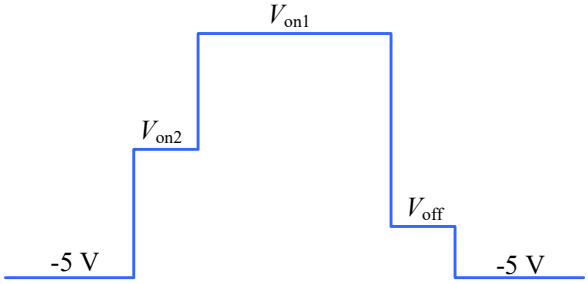


Fig. 3. Desired gate voltage profile for current sharing operation.

The turn-on gate voltage V_{on1} is selected to achieve static current sharing. Fig. 4 shows the relationship between the gate voltage and on-state resistance for one commercial SiC MOSFET. With a higher gate voltage, the on-state resistance is reduced. Thus, by adjusting the static gate voltage, the current distribution among paralleling devices can be regulated.

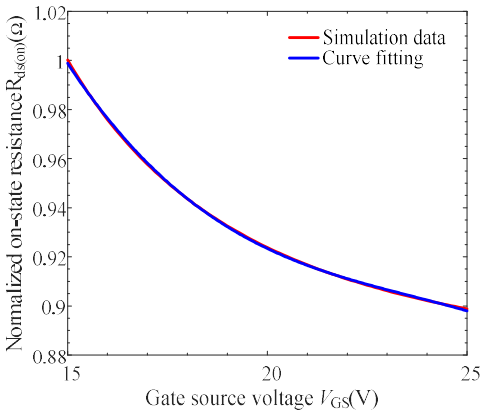


Fig. 4. Relationship between the gate voltage and on-state resistance for a SiC MOSFET.

IV. Active Gate Driver Circuit Design

To achieve the desired multi-level gate profile in Fig. 3, the following circuit topology as shown in Fig. 5 is used. The isolated auxiliary power supply is achieved by using the simple primary side series compensated and secondary side series compensated inductive power transfer topology. The static on-state voltage V_{on1} is generated by the inductive power transfer and the voltage level is adjustable through the switching frequency. The main advantage of using inductive power transfer is to enable high voltage isolation capability, which makes it able to drive medium voltage SiC MOSFETs. All the control signals on the secondary side of the inductive power transfer are transmitted through optical fiber, which has very high voltage isolation capability and *dv/dt* immunity, which would be the best solution for the medium voltage applications. The constant -5 V voltage for turn-off is generated through a non-isolated commercial power module. Two high frequency buck converters are built to achieve the intermediate turn-on and turn-off voltages, where the duty cycles are adjusted to modify the intermediate voltage level. Two voltage selectors are used to select different voltage levels during turn-on and turn-off. The desaturation function of the gate driver is achieved by the current transformer, which is used to monitor the device current. The key components used in Fig. 5 are summarized in Table I. The current buffer IXDN614 from IXYS with 14 A driving capability is selected, which makes it sufficient to drive SiC power modules with paralleling dies in one switching position.

Table I. Key components and part numbers

Parts		Part number
Active gate driver	Primary inverter	LMG5200 GaN based half-bridge power stage
	Buck converters	IXYS IXDN614SI
	Voltage selectors	IXYS IXDN614SI
	Buffer	IXYS IXDN614SI
	Controller	TMS320F28335

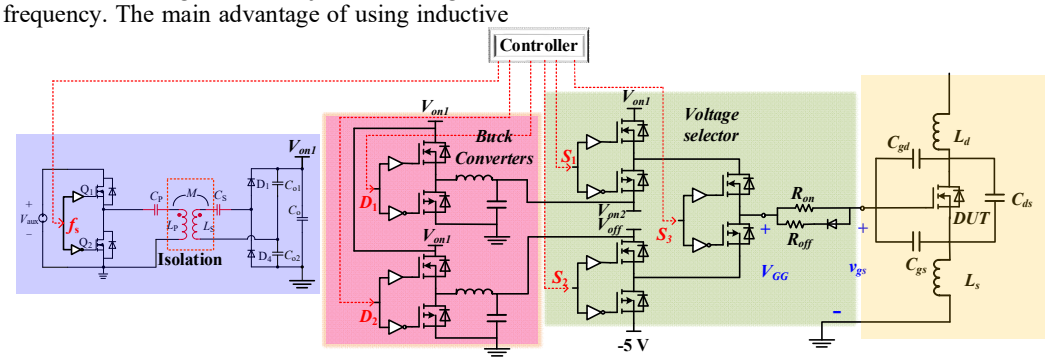


Fig. 5. Implementation circuit for the proposed multi-level active gate driver.

Fig. 6 shows the control strategy to generate the multi-level gate profile. The two buck converters are operating in continuous conduction mode so that their output voltages are determined by their duty ratios. Based on the operational principles of the current buffer (IXDN614), the power supply voltage should be greater than its PWM signal voltage. In the design, the PWM signals are transmitted through the optical fiber, and the optical receiver is powered with 5 V so that the PWM signal voltage is 5 V when it is high. The following restrictions are applied for the multiple voltage levels for the designed active gate driver. The lower boundary value for the static turn-on gate voltage is selected as 10 V to avoid insufficient turn-on, and the upper boundary value is selected as 25 V to ensure safe operation of the device. Please note that a relatively large variation range is selected in this work to prove the effectiveness of the proposed method, while in reality, a small variation range is sufficient to achieve the static current sharing since the on-state resistance mismatch for the paralleling devices with the same part number is not very large.

$$\begin{cases} V_{on1} - V_{on2} \geq 5\text{V} \\ V_{off} - (-5) \geq 5\text{V} \\ V_{on2} - V_{off} \geq 5\text{V} \\ V_{on2} \geq 0\text{V} \\ V_{off} \geq 0\text{V} \\ 10\text{V} \leq V_{on1} \leq 25\text{V} \end{cases} \quad (2)$$

Another consideration is that the intermediate voltage during turn-on process V_{on2} should be greater than the miller plateau voltage to ensure turn-on. Similarly, the intermediate turn-off gate voltage V_{off} should be lower than the miller plateau voltage to ensure safe turn-off. The miller plateau voltage under a given operating condition can be calculated as

$$V_{miller} = V_{th} + I_O / g_{fs} \quad (3)$$

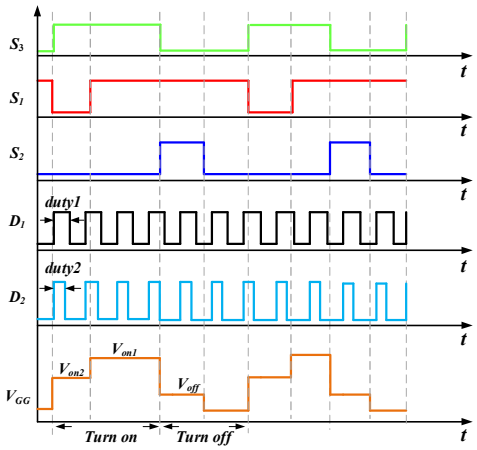
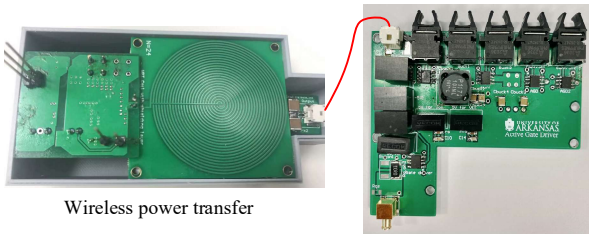


Fig. 6. Control strategy for the proposed active gate driver.

V. Experient Results

To validate the effectiveness of the proposed active gate driver, a double pulse setup with two paralleled SiC MOSFES is built. Fig. 7 shows the prototype of the developed multi-level active gate driver. Due to the high isolation capability of wireless power transfer, the proposed method can be used for medium voltage SiC MOSFET.



Wireless power transfer

Active gate driver

Fig. 7. Prototype of the proposed active gate driver.

In the experiment, two different SiC MOSFETs are selected on purpose to emulate the worst scenario to validate the effectiveness of the proposed strategy, where two devices have large differences in terms of threshold voltage and on-state resistance. One SiC MOSFET is SCT2450KE, its on-state resistance is 450 mΩ and the threshold voltage is in the range of [1.6 V, 4.6 V]. Another SiC MOSFET is SCT3160KL, its on-state resistance is 160 mΩ and the threshold voltage is in the range of [2.7 V, 5.6 V]. The device currents are monitored with two current shunt resistors.

Fig. 8 shows the current sharing performance with traditional gate drivers. Clearly, the current flows through SCT2450KE is much lower due to its large on-state resistance. On the other hand, during the turn-on and turn-off processes, since SCT2450KE has a lower threshold voltage than SCT3160KL, initially, SCT2450KE will handle most of the current, which leads to the unbalance transient currents.

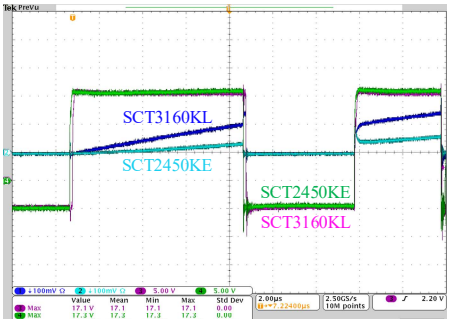


Fig. 8. Current sharing performance with traditional gate driver.

The first step is to achieve static current sharing by adjusting the static gate voltage V_{on1}. The reason is that this voltage will also affect the dynamic current sharing performance. The idea is to increase the on-state resistance of SCT3160KL and reduce the on-state resistance of SCT2450KE. Correspondingly, the static gate voltage for SCT3160KL should be reduced and the static gate voltage for SCT2450KE should be increased. As shown in Fig. 9, by adjusting the static turn-on gate voltage, the static current balancing operation is achieved.

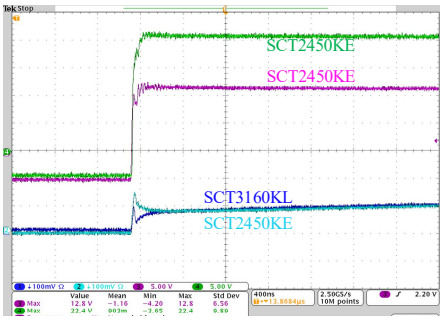


Fig. 9. Static current sharing by adjusting the static gate voltage.

The second step is to achieve dynamic current sharing during the turn-on process by adjusting the intermediate voltage level. To compensate the threshold voltage mismatch, the intermediate voltage of SCT2450KE is adjusted as shown in Fig. 10. With an intermediate voltage, the dynamic current sharing during the turn-on process can be achieved.

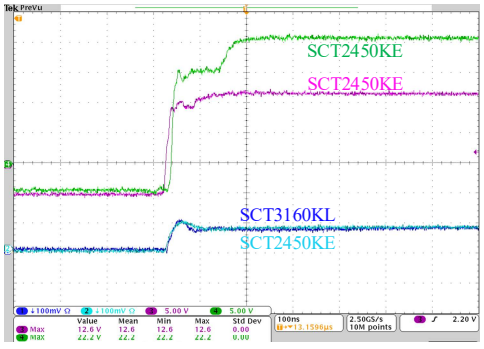


Fig. 10. Dynamic current sharing during turn-on process.

The third step is to achieve current sharing during the turn-off process. Similarly, an intermediate turn-off gate voltage is inserted during the turn-off to achieve current sharing as shown in Fig. 11. The overall current sharing

performance is shown in Fig. 12. Clearly, with the proposed method, the current sharing operation in both static and dynamic can be achieved.

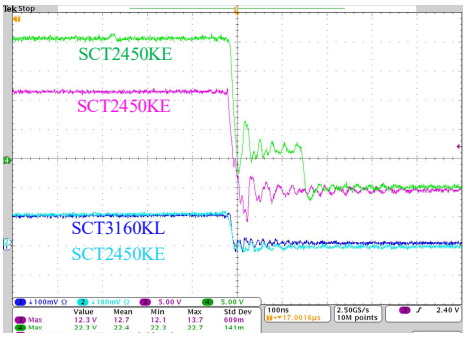


Fig. 11. Dynamic current sharing during turn-off process.

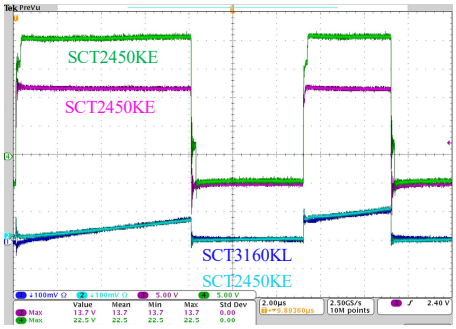
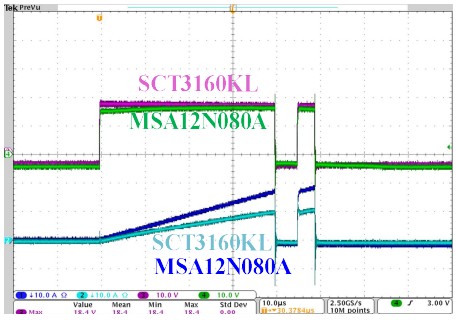
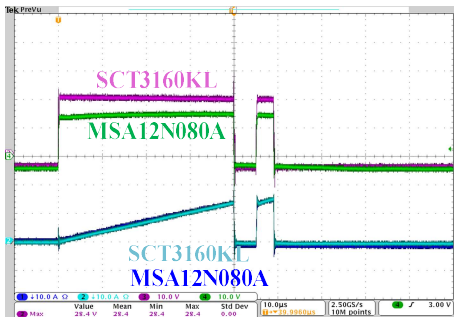


Fig. 12. Overall current sharing performance.

Another two different SiC MOSFETs (SCT3160KL and MSA12N080A) are paralleled to test the feasibility of the proposed strategy. In this combination, the on-state resistance variation is smaller than before, thus, the difference between the static turn-on gate voltages for two devices is smaller than before. Fig. 13 shows the experiment waveforms without and with the proposed active gate driver. With the proposed active gate drive, both the dynamic and static current sharing operation can be achieved.



(a) Without active gate driver



(b) With active gate driver

Fig. 13. Experiment waveforms without and with the proposed active gate driver.

VI. System Structure and Closed-loop Simulation

To achieve the closed-loop control of the system with paralleled devices, the system structure as shown in Fig. 14 is proposed. In the proposed structure, one active gate driver board can be used to drive all the power modules in parallel. To further simplify the circuit, the simple active gate driver with variable static turn-on gate voltage (static current sharing) and delays (dynamic current sharing) is demonstrated. Please note that with the above-mentioned active gate driver, not only the current sharing operation can be achieved, but also the slew rate control for the medium voltage power modules can also be adjusted. From the system control perspective, a local controller together with a central controller structure is proposed. The central controller is responsible for the system control, like modulation and system control. The PWM signal is send to the local controller on each active gate driver board through optical fiber to provide enough signal isolation. Then, the required delay and duty ratio for the active gate driver are generated by the local controller. The device currents in each paralleled power modules are detected by using current transformers and the information is sent back to the local controller.

Fig. 15 shows experiment waveforms comparisons between the designed current transformer and commercial Rogowski coil. Clearly, the measured current from the designed current transformer matches very well with the commercial Rogowski coil. The isolation for the current transformer can be achieved by using high voltage primary cable and selecting the core geometry.

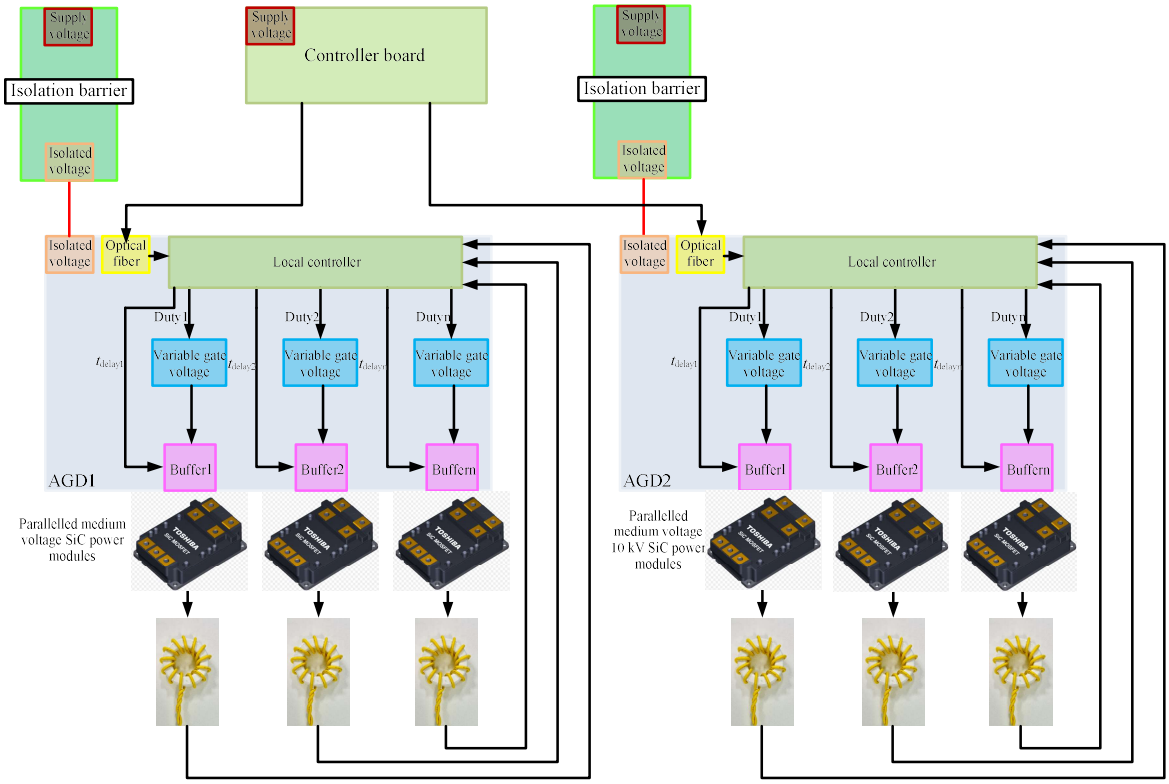


Fig. 14. System structure for medium voltage SiC power modules with paralleling operation.

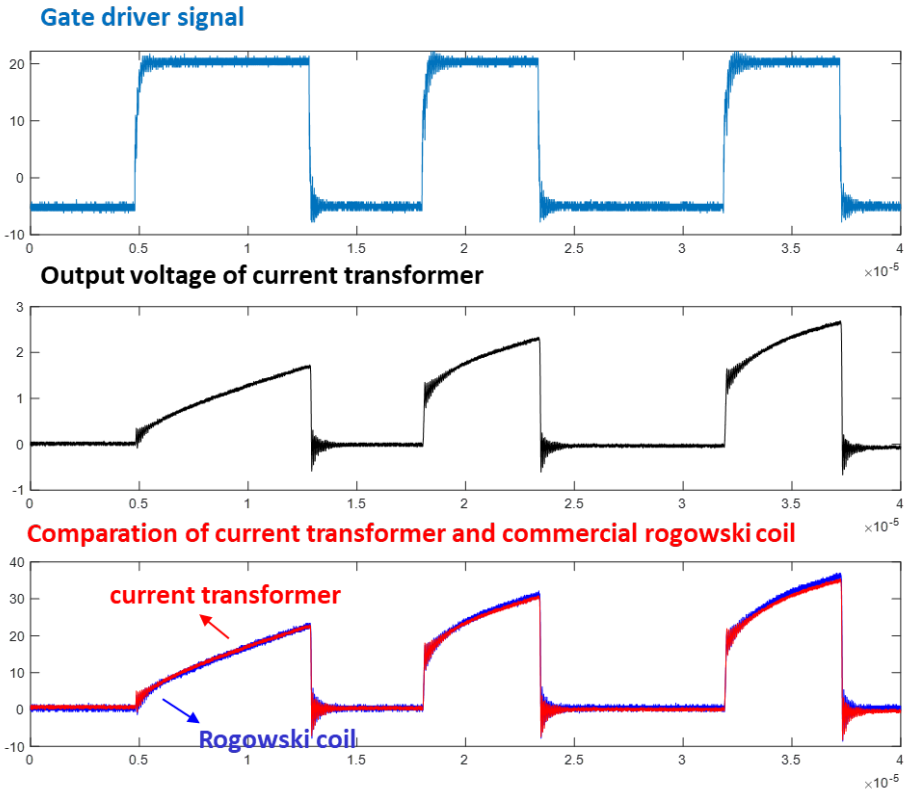


Fig. 15. Experiment waveforms comparisons between the designed current transformer and commercial Rogowski coil.

Closed-loop simulation model is built with MATLAB/SIMULINK. The SiC MOSFET is modelled by using the Shichman-Hodges equation [14]. The threshold voltage and on-state resistance are set different for the paralleled devices. Fig. 16 shows the simulation results. It can be seen that the current sharing operation can be achieved automatically with the proposed active gate driver after several cycles.

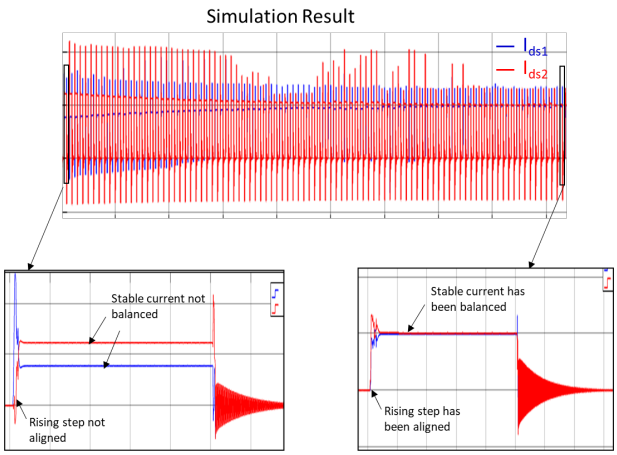


Fig. 16. Closed-loop simulation results with MATLAB/SIMULINK.

VII. Conclusions

In this work, a four-level active gate driver is proposed for the medium voltage SiC MOSFETs with paralleling operation. The static current sharing is achieved by adjusting the static turn-on gate voltage, while the dynamic current sharing is achieved by adjusting the delays and intermediate gate voltages. Another benefit of the proposed active gate driver is that it can achieve both current sharing and slew rate control. Moreover, the system structure is discussed for the medium voltage SiC MOSFETs with paralleling operation. The closed-loop simulation results are also presented.

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