Subcircuit Based Modelling of SiC MOSFET in MATLAB/SIMULINK

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***Abstract*— Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) has been widely used in numerous industrial applications owning to their characteristics of low on-state resistance, high thermal conductivity, and high operating temperature. To fully utilize the potential of SiC MOSFET, an accurate device model is desired to evaluate the device performance before fabrication. In this article, an accurate subcircuit based model is used to describe the SiC MOSFET dynamic performance. In the model, the non-linearity of device parasitic capacitance is considered by extracting capacitance values under multiple drain-source voltage values from datasheet. All the possible circuit parasitic inductances are extracted by using ANSYS Q3D. To reduce the model complexity, the threshold voltage based model for MOSFET is adopted. Finally, the subcircuit based model is implemented in MATLAB/SIMULINK. The developed model has the advantages of high accuracy, convenient, fast execution time. The model would be a convenient tool to evaluate the device performance and help understanding the experiment phenomena. To validate the accuracy of the developed model, double pulse test (DPT) results of a 1.2 kV SiC MOSFET (ROHM) from both simulation and experiment are compared, the results shown that the developed model is an effective evaluation tool for the SiC MOSFET performance.**

Keywords—Subcircuit model, MATLAB/SIMULINK, SiC MOSFET

I. INTRODUCTION

Owning to their characteristics of fast switching speed, low switching loss, and high operating temperature, SiC MOSFETs have gained popularity in numerous industrial applications, like transportation electrification and renewable energy systems [1]-[7]. Lots of research efforts have been made on the power converter design to achieve high efficiency and high power density [8]. To fully utilize the potential of SiC MOSFET, and accurate model is required to predict the device performance before fabrication. According to [9], the SiC MOSFET model can be categorized into five groups: 1) behavioral model; 2) semi-physics based model; 3) physic based model; 4) semi numerical based model; and 5) numerical model. The most commonly used models are behavioral model and physic based model. Compared with behavioral models, physics based models require users to be familiar with the device whole fabrication process and structure information, which makes these models less convenient and more complicate [10]. On the other hand, behavioral models use simple I-V and C-V curves provided by manufacture datasheet or curve tracer to extract the parameters required for the model. In [11], the SiC MOSFET is modelled as one drain-to-source resistance and two constant parasitic capacitances. But the non-linearity of parasitic capacitances with device drain-to-source voltage is not considered and the drain-to-source capacitance is omitted in the model. To improve the model accuracy, in [12], all the parasitics and their non-linearity are considered to construct an accurate model to estimate the SiC MOSFET switching loss. To reduce the model complexity and get closed-form solution, some assumptions and simplifications are made to achieve a trade-off between the model accuracy and complexity. Massive computations are required, which is not convenient. In [10], the SiC MOSFET model is built by extracting the parameters from static characterization results and the model is implemented in Saber. The model shows that the simulation results match the experimental results and can provide high accuracy to evaluate the device performance.

In this article, a subcircuit based model is implemented in MATLAB/SIMULINK. The model accuracy is ensured by taking all the circuit parasitics and their non-linearity's into considerations. Meanwhile, only datasheet is required to build the model, which makes the application of the developed model convenient and attractive. Moreover, with the aid of the developed model, the device and power converter performances can be effectively evaluated in the MATLAB/SIMULINK environment. Fast execution time is achieved by using variable step solver (ode23t). To validate the correctness and effectiveness of the developed model, clamped inductive load test for a 1.2 kV SiC MOSFET from ROHM is performed and the results are compared with the proposed model results. In this article, we reported a convenient and accurate subcircuit model for SiC MOSFET to evaluate device performance, including overshoot and switching losses and help understanding how circuit parasitics influences on the voltage and current waveforms.

II. Model Description

Fig. 1 shows the subcircuit model of the SiC MOSFET, where C_{GS} is the gate source parasitic capacitance, C_{GD} is the gate drain parasitic capacitance, C_{DS} is the drain source parasitic capacitance, L_G is the gate terminal parasitic inductance, L_D is the drain terminal parasitic inductance, L_S is the source terminal parasitic inductance, and $R_{G,int}$ is the internal gate resistance. The relationship between C_{GS}, C_{GS}, C_{GS} and C_{iss}, C_{rss}, C_{oss} can be expressed as follows

$$\begin{aligned} C_{GD} &= C_{rss} \\ C_{GS} &= C_{iss} - C_{rss} \\ C_{DS} &= C_{oss} - C_{rss} \end{aligned} \quad (1)$$

where C_{iss} is the input capacitance, C_{rss} is the reverse transfer capacitance, and C_{oss} is the output capacitance. These capacitance values with different drain-to-source voltage can be obtained from manufacture datasheet or curve tracer static characterization results. Normally, the datasheet results can already provide a good understanding of device performance. For more accuracy analysis, the static characterizations can be done with curve tracer. The parasitic inductances and internal gate resistance can be measured with a LCR meter [10].

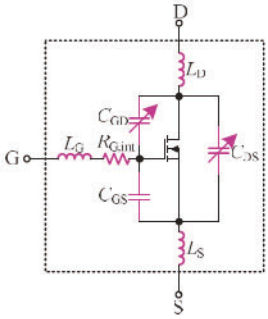


Fig. 1. Subcircuit model for SiC MOSFET.

The MOSFET is modelled by using the Shichman-Hodges equation. The operation of MOSFET is divided into three regions: 1) off region; 2) linear region; and 3) saturated region. The expressions for drain-to-source current I_{DS} for each region can be expressed as follows.

$$\begin{aligned} &I_{DS} = 0, V_{GS} < V_{th}, \text{ off region} \\ &I_{DS} = K((V_{GS} - V_{th})V_{DS} - V_{DS}^2 / 2)(1 + \lambda |V_{DS}|), \\ &\quad 0 < V_{DS} < V_{GS} - V_{th}, \text{linear region} \\ &I_{DS} = \frac{K}{2}(V_{GS} - V_{th})^2 (1 + \lambda |V_{DS}|), 0 < V_{GS} - V_{th} < V_{DS}, \\ &\quad \text{saturated region} \end{aligned} \quad (2)$$

where K is the transistor gain, V_{th} is the threshold voltage, and λ is the channel modulation.

Next, the circuit model for the clamped inductive load (CIL) or DPT setup is discussed. Fig. 2 shows the DPT circuit model with the circuit parasitics. The definitions of circuit parasitics are summarized in Table 1.

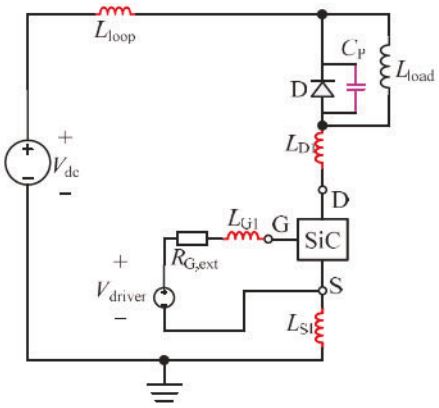


Fig. 2. Circuit model for DPT.

TABLE I. CIRCUIT PARASITICS AND THEIR VALUES

Variable	Definition	Values
$R_{G,ext}$	Gate driver resistor, different resistance may apply for turn-on and turn-off	20 Ω/5 Ω
L_{G1}	Gate loop parasitic inductance introduced by gate driver	9.8 nH
L_{S1}	Parasitic inductance from source terminal to ground	2.5 nH
L_{D1}	Parasitic inductance from drain terminal to freewheeling diode	2.2 nH
L_{load}	Load inductor	30 μH
C_P	Junction capacitance of freewheeling diode	
L_{loop}	Power loop inductance caused by PCB traces	30 nH
V_{dc}	Dc bus voltage	300 V
V_{driver}	Gate driver voltage	25 V/-5 V

Next, the parameter extraction is discussed for the model. Firstly, the parameters K, V_{th}, and λ are extracted by using curve fitting of the device transfer characteristics provided in the manufacture datasheet. Based on equation (2), the threshold voltage can be found when the device entering from off-region to linear region. The transistor gain K and channel modulation λ can be found by using the curve fitting tool 'cftool' in MATLAB. Fig. 3 shows the curve fitting results with K=1.7 A/V^2, V_{th}=5.5 V, and λ= 0.03963 V^{-1}.

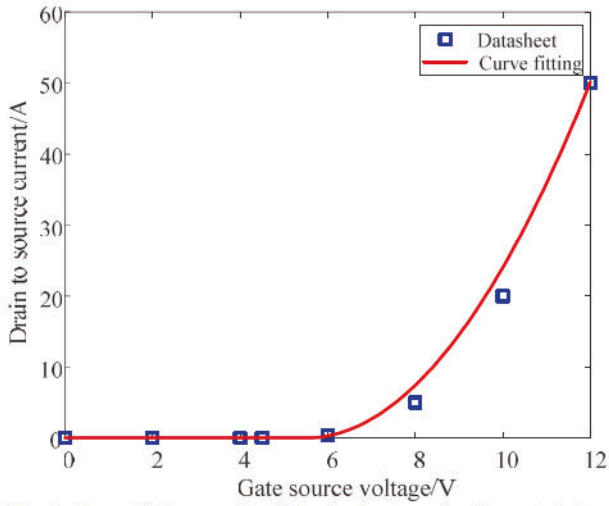


Fig. 3. Curve fitting result of the device transfer characteristic.

The non-linearity of the device parasitic capacitance is considered. The non-linearity of input capacitance C_{iss} is also considered. C_{iss}, C_{rss} and C_{oss} are considered as variables with respect to drain-to-source voltage. Piecewise linear method is used to characterize the non-linearity of device parasitic capacitance by selecting multiple points on the datasheet C-V curves. Based on the selected device, five operating points from the C-V curve are selected as shown in Fig. 4, and the parasitic capacitance is linearized based on these points.

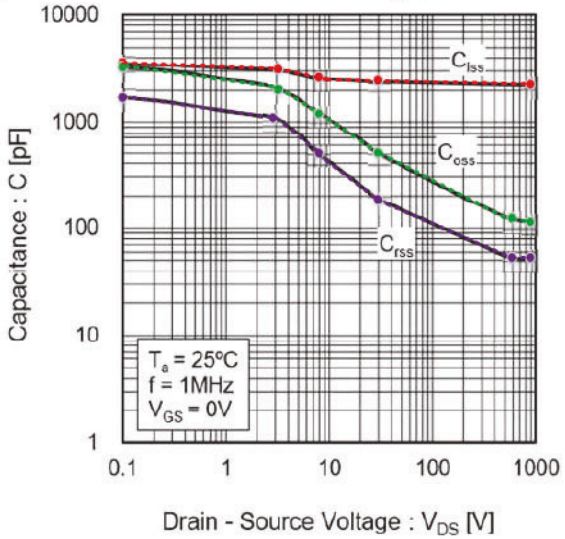


Fig. 4. Selected points on C-V curve of SiC MOSFET.

The terminal parasitic inductance is caused by the device packaging. For SiC MOSFET with TO-247 package, the typical parasitic inductance for three terminals are: L_G=9.2 nH, L_D=6.1 nH, L_S=7.5 nH.

The parasitic values for the DPT circuit are summarized in Table 1. The parasitic capacitance of freewheeling diode is also modelled by choosing multiple points on the C-V curve to represent its relationship between the volatge and capacitance as shown in Fig. 5.

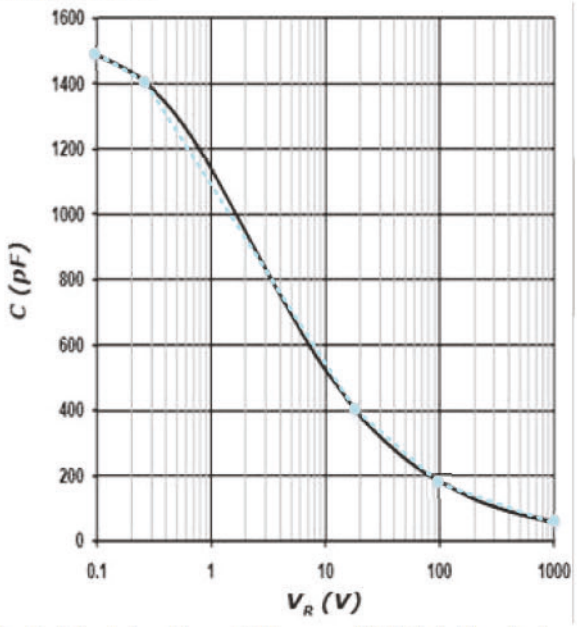


Fig. 5. Selected points on C-V curve of SiC Schottky diode.

Fig. 6 shows the picture of gate driver board, where the gate driver chip Si8271 from Silicon lab is used. The optic fiber is used for the pulse signal transmission with reduced parasitic. Fig. 7 shows the ANSYS Q3D extraction results. It can be seen that the gate loop inductance is around 9.8 nH. Similarly, the power loop inductance can also be extracted by using the ANSYS Q3D, and the power loop parasitic inductance is around 30 nH.

Fig. 6. Picture of the gate driver board.

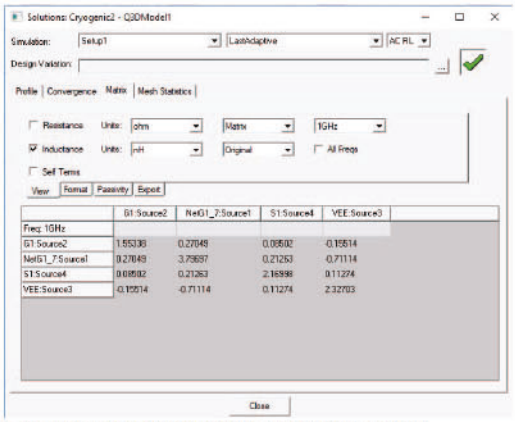


Fig. 7. Picture of ANSYS Q3D extraction results.

Fig. 8 shows the DPT circuit model implemented in the MATLAB/SIMULINK. The advantage of the subcircuit model is that it can be simply implemented based on the manufacture datasheet. By using the SIMULINK environment, massive computations are not required so that the users can easily use it to evaluate the device performance and help understanding different parasitics influence on device performance.

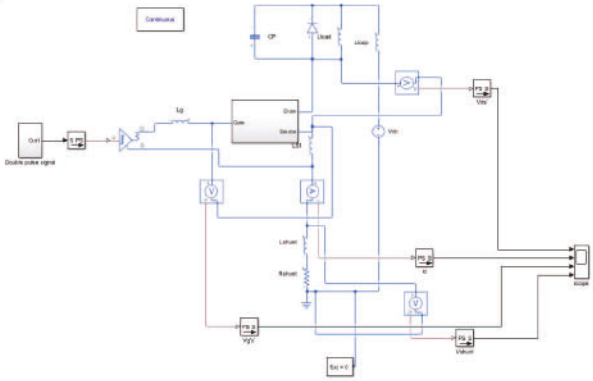


Fig. 8. Implemented circuit model in MATLAB/SIMULINK.

III. Results and Discussions

In this Section, the simulation results from the developed model and experiment results are compared to demonstrate the effectiveness and correctness of the developed model. The 1.2 kV SiC MOSFET with part number of SCT3030KL from ROHM is selected as device under test and the C4D40120D SiC diode from CREE is selected as the freewheeling diode. Fig. 9 shows the test setup, where the passive voltage probes from Tektronix with 200 MHz bandwidth are used to measure the V_{DS} and V_{GS}. I_{DS} is measured with 1200 MHz coaxial shunt from T&M. The load inductor current is measured by using current probe with 30 MHz bandwidth. Fig. 10 shows the experiment waveforms from oscilloscope when input voltage equals 300 V, load current equals 20 A, and with two different turn-on gate resistance.

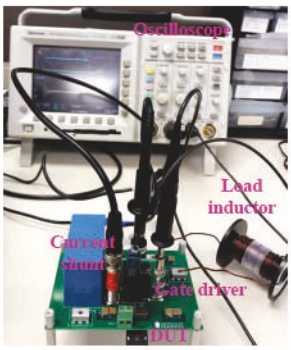
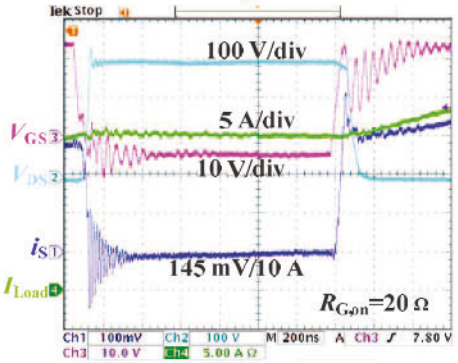
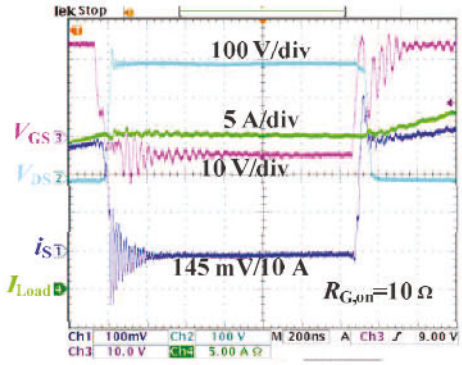


Fig. 9. Picture of the DPT setup.



(a) V_{dc}=300 V, I_{Load}=20 A, $R_{G,on}$=20 Ω

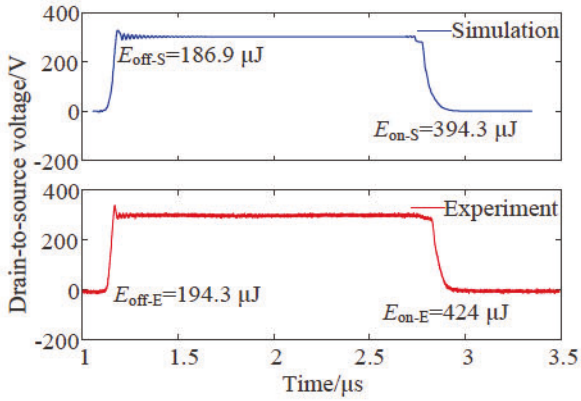


(b) V_{dc}=300 V, I_{Load}=20 A, $R_{G,on}$=10 Ω

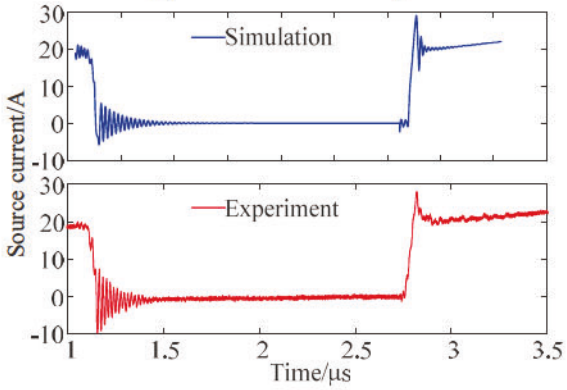
Fig. 10. Experiment setup and experiment waveforms.

Fig. 11 shows the simulation and experiment results comparison when input voltage equals 300 V and load current equals 20 A with $R_{G,on}$=20 Ω and $R_{G,off}$=5 Ω. Fig. 12 shows the comparison results when $R_{G,on}$=10 Ω and $R_{G,off}$=5 Ω. Clearly, the developed model can well predict the device turn-on and turn-off transient performances, which can be used in the pre-design stage of power converter to evaluate the switch performance

and design heatsink. The switching loss obtained by using the developed model agrees with the experiment results. Please note that with a variable step solver (ode23t), simulation time less than one second is achieved for the developed model.

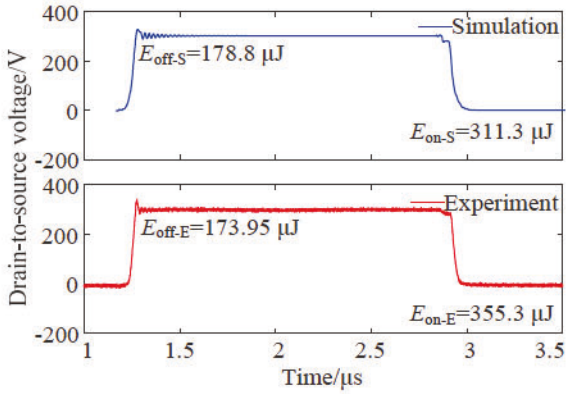


(a) Drain-to-source voltage

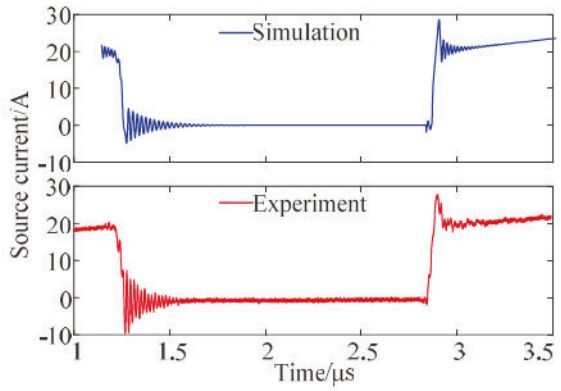


(b) Source current

Fig. 11. Experiment and simulation waveforms comparison when V_{dc}=300 V, I_{Load}=20 A, $R_{G,on}$=20 Ω



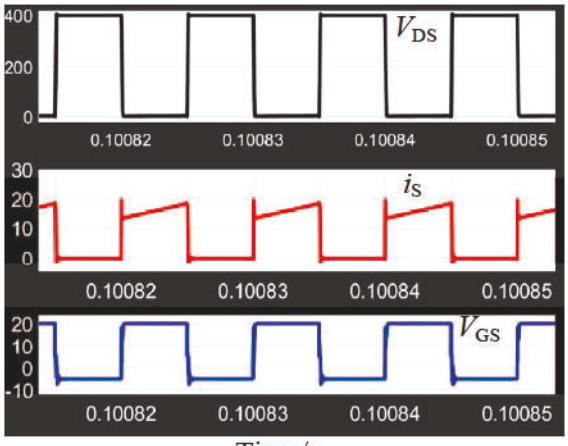
(a) Drain-to-source voltage



(b) Source current

Fig. 12. Experiment and simulation waveforms comparison when V_{dc}=300 V, I_{Load}=20 A, $R_{G,on}$=10 Ω

Application of the developed subcircuit model in power converter is also examined. The boost converter is used as an example. The converter efficiency can be easily evaluated. The duty cycle is 0.5, the switching frequency is 100 kHz, and the load resistance is 50 Ω. When input voltage is 200 V, the converter output power is around 3.2 W. Fig. 13 shows the simulation waveforms, including the switch current, switch voltage, inductor current, and output voltage. With input voltage of 200 V, the converter efficiency is 95.2%. When the input voltage decreases to 100 V, the output power is 800 W and the system efficiency is 96.1%.



(a)

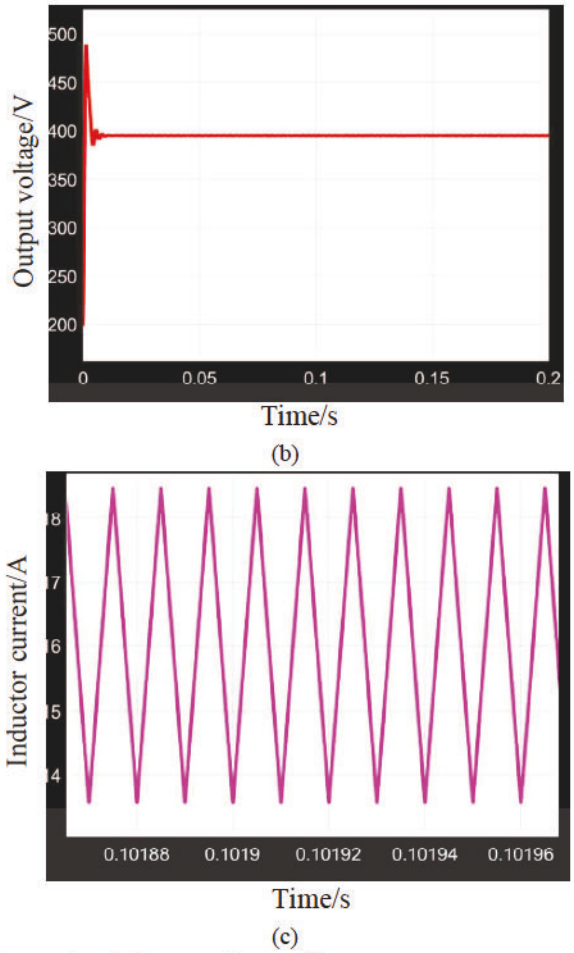


Fig. 13. Simulation waveforms of boost converter.

IV. Conclusions and Future Work

In this article, a subcircuit based SiC MOSFET model is developed in MATLAB/SIMULINK. The non-linearity of the device parasitic capacitances and all possible parasitic inductances are considered to improve the model accuracy. The required data can be obtained from the manufacture datasheet, which is applicable for other SiC MOSFET. In addition, with the MATLAB/SIMULINK environment, the developed model can be easily applied in the power converter to obtain a system level performance. Moreover, fast simulation time (less than one second) with variable step solver (ode23t) is achieved. Thus, it would be convenient to use this model to predict the device performance in the design stage. In the future, the temperature influence on the device model should be taken into consideration. In addition, the developed model can also be applied to investigate the circuit parasitics influence on current sharing of paralleling operation.

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