ARTICLE

Two-Dimensional Cold Electron Transport for Steep-Slope Transistors

Maomao Liu, Hemendra Nath Jaiswal, Simran Shahi, Sichen Wei, Yu Fu, Chaoran Chang, Anindita Chakravarty, Xiaochi Liu, Cheng Yang, Yanpeng Liu, Young Hee Lee, Vasili Perebeinos, Fei Yao,* and Huamin Li*

Read Online

ACCESS | 📊 Metrics & More | 📄 Article Recommendations | 🆂🅸 Supporting Information

ABSTRACT: Room-temperature Fermi–Dirac electron thermal excitation in conventional three-dimensional (3D) or two-dimensional (2D) semiconductors generates hot electrons with a relatively long thermal tail in energy distribution. These hot electrons set a fundamental obstacle known as the "Boltzmann tyranny" that limits the subthreshold swing (SS) and therefore the minimum power consumption of 3D and 2D field-effect transistors (FETs). Here, we investigated a graphene (Gr)-enabled cold electron injection where the Gr acts as the Dirac source to provide the cold electrons with a localized electron density distribution and a short thermal tail at room temperature. These cold electrons correspond to an electronic refrigeration effect with an effective electron temperature of ~145 K in the monolayer MoS_2, which enables the transport factor lowering and thus the steep-slope switching (across for three decades with a minimum SS of 29 mV/decade at room temperature) for a monolayer MoS_2 FET. Especially, a record-high sub-60-mV/decade current density (over 1 $\mu A/\mu m$) can be achieved compared to conventional steep-slope technologies such as tunneling FETs or negative capacitance FETs using 2D or 3D channel materials. Our work demonstrates the potential of a 2D Dirac-source cold electron transistor as a steep-slope transistor concept for future energy-efficient nanoelectronics.

KEYWORDS: graphene, MoS_2, Dirac-source, cold electrons, steep-slope transistors, electronic refrigeration
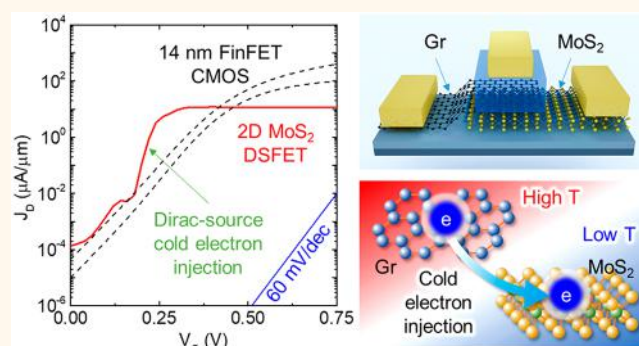
F ermi–Dirac electron thermal excitation is an intrinsic physical phenomenon that grants a tunable electrical conductivity of semiconductors at room temperature, but on the contrary, it also causes excessive power dissipation in various electron systems.[1−3] Especially in field-effect transistors (FETs), the "Boltzmann tyranny" induced by the thermal excitation of hot electrons sets a fundamental limit in the steepness of the transition slope between off and on states, known as the subthreshold swing (SS). To change the current by one order of magnitude at room temperature, the minimum gate voltage is required to be $\partial V_G/\partial(\log_{10} I_D) = (\partial V_G/\partial\Psi_s)[\partial\Psi_s/\partial(\log_{10} I_D)] \sim (k_B T/q) \ln 10 \sim 60$ mV, where V_G is the gate voltage, I_D is the drain current, Ψ_s is the channel surface potential, and k_B, T, and q are the Boltzmann constant, temperature, and electronic charge, respectively. Therefore, various types of steep-slope FETs have been proposed to increase the turn-on steepness and overcome the bottleneck to continue minimizing the power consumption, including tunneling FETs (TFETs)[1−3] and negative capacitance FETs (NCFETs).[4−6] These solutions in principle can achieve a sub-60-mV/decade SS, for example, by lowering the transport factor $(\partial\Psi_s/\partial(\log_{10} I_D))$, via a band-to-band Zener tunneling effect in TFETs[7−10] or by reducing the body factor $(\partial V_G/\partial\Psi_s)$ via a ferroelectric gate layer with the negative differential capacitance in NCFETs.[11−13] However, there are also critical challenges for these technologies to overcome, such as the low current density and source/drain asymmetry in TFETs[14−16] as well as the lack of fundamental understanding in NCFETs.[17−20]

With the rise of graphene (Gr), two-dimensional (2D) van der Waals (vdW) layered materials have been explored as promising material candidates for future energy-efficient nanoelectronics due to the natural quantum confinement in an atomically thin body.[21,22] MoS_2 as one of the most
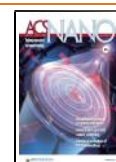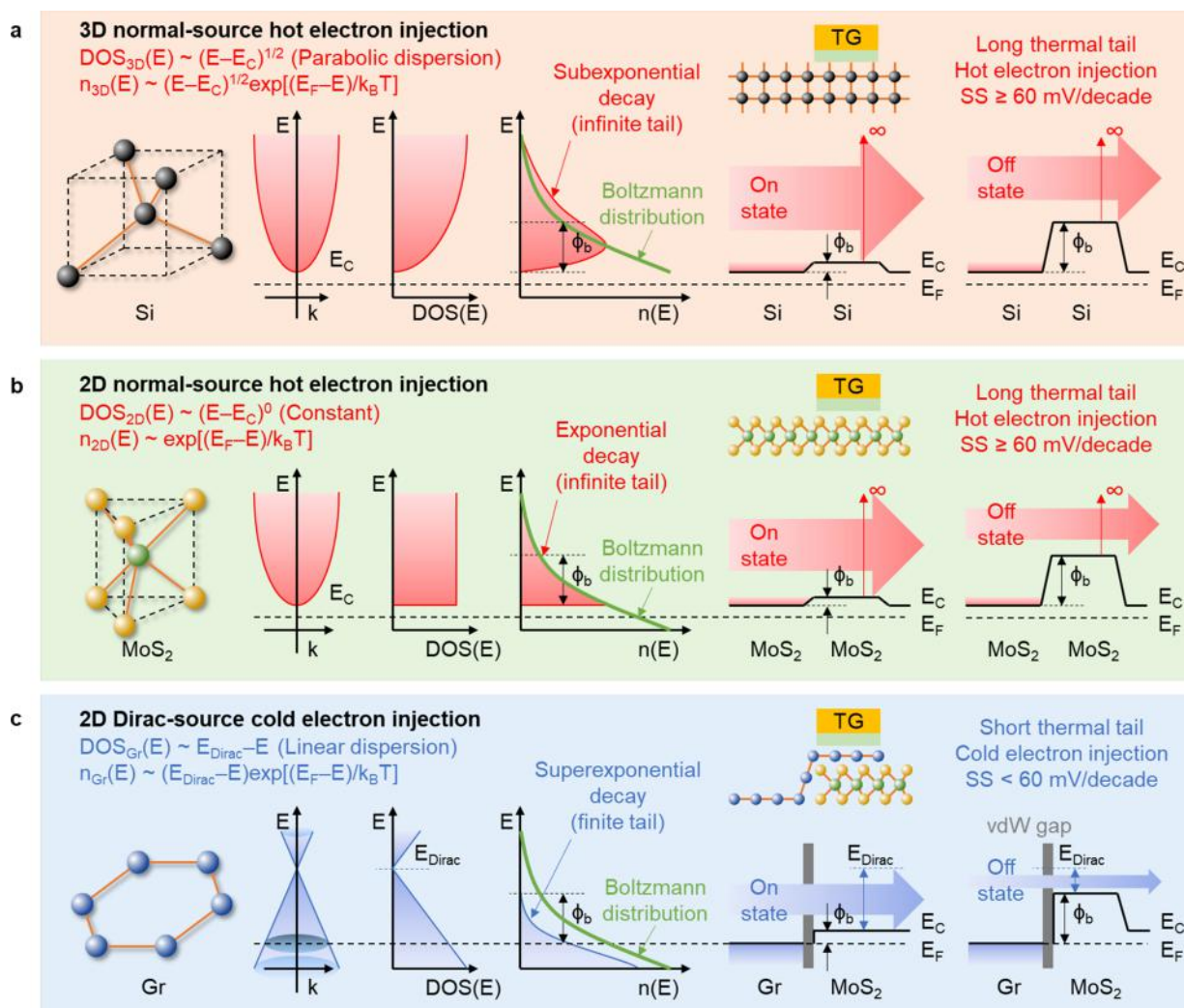
Figure 1. Qualitative comparison of normal-source hot electron injection and Dirac-source cold electron injection. The atomic crystal structure and energy band diagrams including $E-k$, $E-DOS$, and $E-n$ diagrams are illustrated for (a) 3D semiconductors (*e.g.*, Si), (b) 2D semiconductors (*e.g.*, monolayer MoS_2), and (c) 2D monolayer Gr, where k is the wave vector. The corresponding energy band diagrams at the on- and off-states for transistor operation are also included. In the conventional Si or MoS_2 FETs, the 3D or 2D normal-source hot electron injection occurs along the in-plane direction and possesses an infinitely long thermal tail over a potential barrier. In the MoS_2 DSFET, the 2D Dirac-source cold electron injection has a short thermal tail terminated at E_{Dirac}, and it can be cut off more efficiently by a gate-controlled ϕ_b along the out-of-plane direction.

representative semiconducting transition metal dichalcogenides (TMDs) acts as an excellent channel material for nanoscale transistors by offering ideal electrostatic tunability, an appropriate direct bandgap, and moderate carrier mobility, *etc.*[23−25] The MoS_2-based TFETs[7−10] and NCFETs[11−13] have been demonstrated with the sub-60-mV/decade SS. However, neither of them can provide a sub-60-mV/decade current density higher than 1 $\mu A/\mu m$, which is one key metric for a logic transistor to benefit from the steep slopes.[15,16,26]

In this work, we demonstrated a Gr-enabled Dirac-source "cold" electron injection that possesses a more localized electron density distribution and a shorter thermal tail, compared to the conventional normal-source hot electron injection in 3D or 2D semiconductors. The cold electron injection has been implemented in a monolayer MoS_2 FET to introduce an electronic refrigeration effect, which can lower the transport factor and thus enable an outstanding steep-slope switching (across for three decades with a minimum SS of 29 mV/decade at room temperature), an excellent on/off ratio

($\sim10^7$), a strong on-current saturation (~10 $\mu A/\mu m$), and especially a record-high sub-60-mV/decade current density (over 1 $\mu A/\mu m$) compared to any TFETs or NCFETs using 2D or 3D channel materials. The effective electron temperature was extracted to be ~145 K, on the basis of the energy distribution of the cold electrons at room temperature. Our work presents the 2D Dirac-source cold electron FET as a steep-slope transistor concept with the sub-60-mV/decade switching capability, which can benefit future energy-efficient nanoelectronics based on 2D materials.

RESULTS AND DISCUSSION

Graphene-Enabled 2D "Cold" Electron Transport. To illustrate the underlying mechanism and the fundamental advantages of the Gr-enabled Dirac-source cold electron transport, we compare it with the conventional normal-source hot electron transport in 3D and 2D semiconductors such as Si and monolayer MoS_2. The electron density (n) depends on the energy (E) and is defined as a product of the Fermi−Dirac
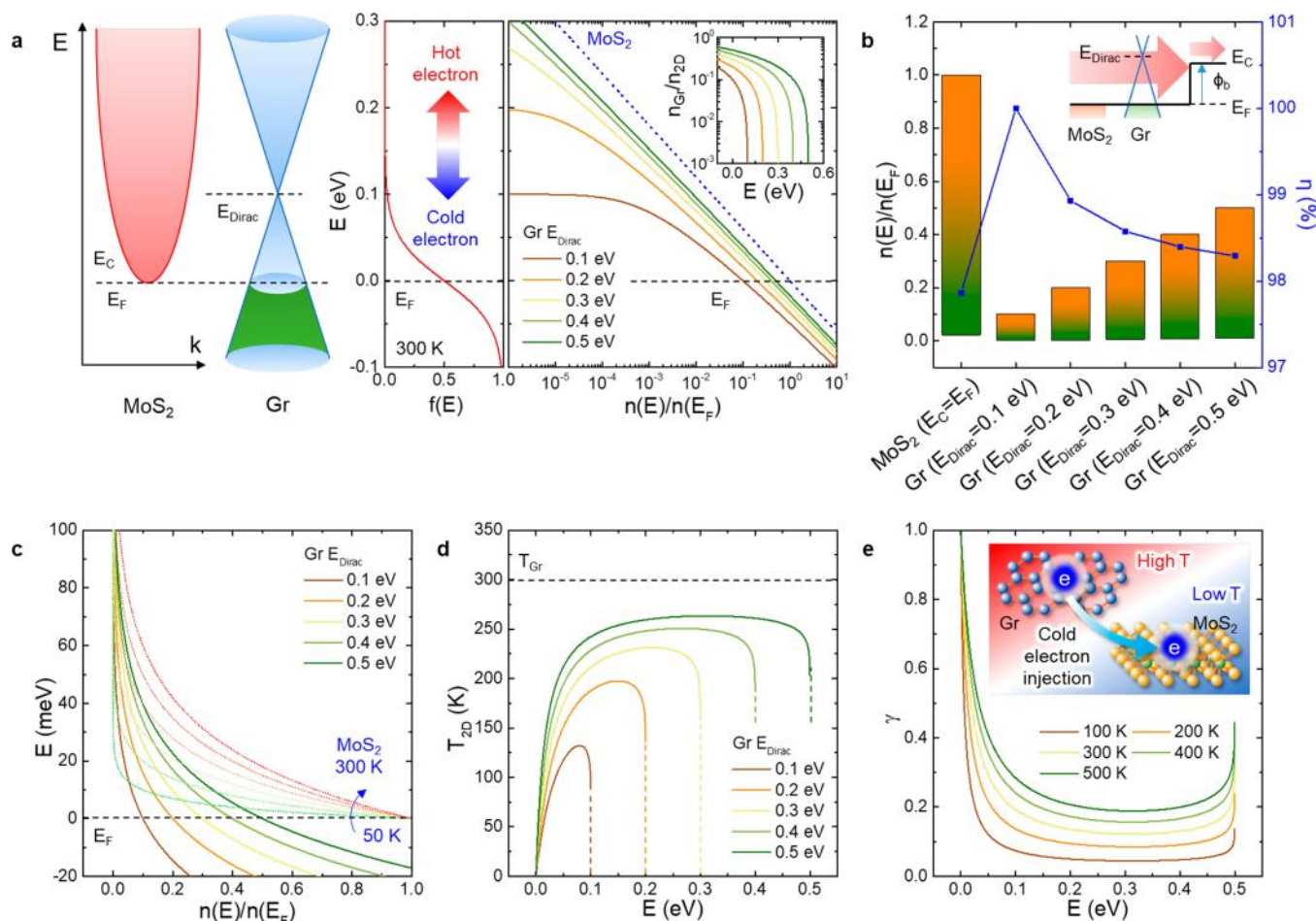
Figure 2. Quantitative comparison of 2D normal-source hot electron injection in monolayer MoS_2 and 2D Dirac-source cold electron injection in monolayer Gr. (a) Left: Energy band structures of MoS_2 and Gr in a $E-k$ diagram. Right: Calculated E as a function of $f(E)$ and $n(E)/n(E_F)$. Here, $E_F = 0$ eV for both MoS_2 and Gr. Inset: $n_{Gr}(E)/n_{2D}(E)$ as a function of E for different doping levels in Gr. (b) Reduction of $n(E)/n(E_F)$ and the corresponding η for both MoS_2 and Gr when ϕ_b increases from 0 to 0.1 eV. Here, $E_F = E_C = 0$ eV for MoS_2 and $E_F = 0$ eV for Gr. Inset: Energy band structure illustrates the electron flow over ϕ_b for MoS_2 or Gr. (c) Comparison of the electron excitation of Gr at room temperature (solid lines) and that of MoS_2 at a low temperature (dot lines, from 50 to 300 K with a step of 50 K). (d) T_{2D} as a function of E when the cold electron injection occurs at $T_{Gr} = 300$ K. Dash lines are guides for the eye. (e) γ as a function of E when the cold electron injection occurs at T_{Gr} ranging from 100 to 500 K. Inset: Illustration of an electronic refrigeration effect when the cold electrons are injected from Gr to MoS_2.

distribution function $f(E) = 1/\{1 + \exp[(E - E_F)/k_B T]\}$ and the density of states (DOS), where E_F is the Fermi energy. Here, we use the subscripts of 3D, 2D, and Gr to distinguish the properties for 3D semiconductors, 2D semiconductors, and monolayer Gr, respectively. Because the DOS is a parabolic function of E in 3D semiconductors as $DOS_{3D}(E) \sim (E - E_C)^{1/2}$, the corresponding $n(E)$ can be expressed as $n_{3D}(E) \sim (E - E_C)^{1/2} \exp[(E_F - E)/k_B T]$, which follows a subexponential decay, as shown in Figure 1a, where E_C is the minimum conduction band edge. Similarly, since the DOS in 2D semiconductors is constant ($DOS_{2D}(E) \sim (E - E_C)^0$), the corresponding $n(E)$ possesses an exponential decay described as $n_{2D}(E) \sim \exp[(E_F - E)/k_B T]$, as shown in Figure 1b. Assuming $E_F = 0$ eV, the exponential decay of $n_{2D}(E)$ also follows the Maxwell–Boltzmann distribution function known as $n(E) \sim \exp(-E/k_B T)$. Both $n_{3D}(E)$ and $n_{2D}(E)$ present a relatively long Boltzmann thermal tail at room temperature, and these tails extend to infinity at the nonzero temperature in principle, due to the Fermi–Dirac electron thermal excitation. Considering a conventional FET structure where a gate-controlled potential barrier (ϕ_b) is established within the

channel, the drain current is attributed to the thermionic injection of the electrons with an E higher than ϕ_b. Due to the long Boltzmann thermal tail as E increases, the minimum SS for 3D and 2D semiconductor channels suffers from the "hot" electron injection and has a limit of 60 mV/decade at room temperature.

As a comparison, the monolayer Gr has a linear energy dispersion near the Dirac point, and its DOS is a linear function of E as $DOS_{Gr}(E) \sim E_{Dirac} - E$ where E_{Dirac} is the energy at the Dirac point. The corresponding $n(E)$ of the monolayer Gr can be expressed as $n_{Gr}(E) \sim (E_{Dirac} - E)/\{1 + \exp[(E - E_F)/k_B T]\} \sim (E_{Dirac} - E) \exp[(E_F - E)/k_B T] \sim (E_{Dirac} - E)n_{2D}(E)$. Thus, when $E_{Dirac} - E < 1$, $n_{Gr}(E)$ always shows a superexponential decay compared to $n_{2D}(E)$. The Boltzmann thermal tail in Gr is relatively short, because it is no longer infinite but terminated right at E_{Dirac} even at room temperature, as shown in Figure 1c. By exploiting the monolayer Gr as the cold electron source in a heterojunction structure, for example, a Gr/MoS_2 heterobilayer, ϕ_b can be created at the interface and tuned by the gate electrostatically.[27] Compared to the hot electron injection in 3D and 2D
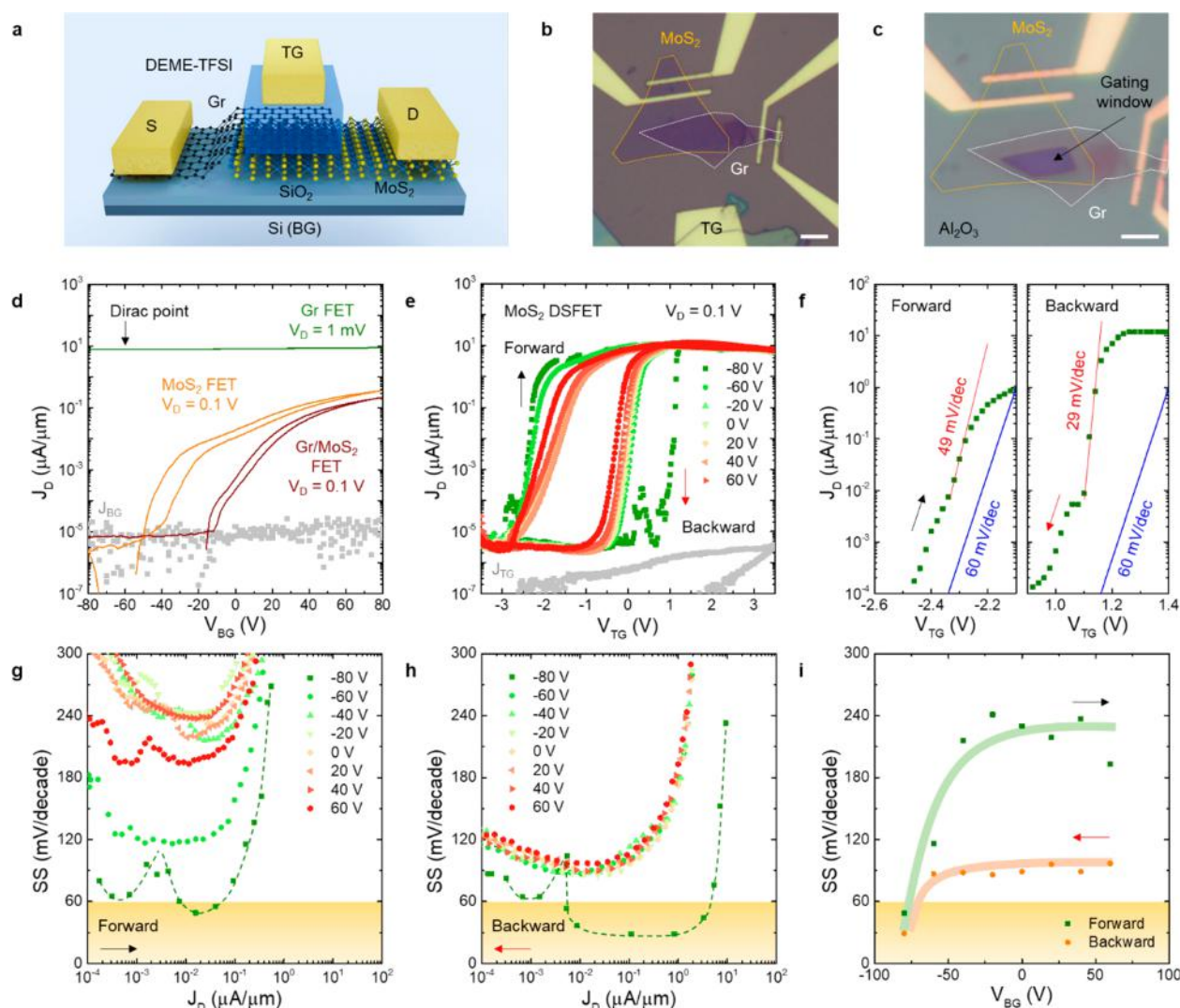
Figure 3. Sub-60-mV/decade switching of 2D MoS$_2$ DSFET at room temperature. (a) Schematic illustration of the ideal device structure. Here, S, D, TG, and BG denote the source, drain, top gate, and back gate, respectively. (b and c) Optical microscopy images of the device before and after Al$_2$O$_3$ deposition. A gating window is opened within the Gr/MoS$_2$ overlapping area for a localized top gating through an ionic liquid. Scale bar: 5 μm. (d) J_D−V_{BG} transfer characteristics of Gr FET, MoS$_2$ FET, and Gr/MoS$_2$ FET. (e) J_D−V_{TG} transfer characteristics of MoS$_2$ DSFET under various V_{BG} values. J_{BG} and J_{TG} are the leakage current densities measured from the back gate and the top gate, respectively. Back and red arrows indicate the forward and backward sweeps, respectively. (f) Sub-60-mV/decade switching of MoS$_2$ DSFET in the forward and backward sweeps. Blue line is the 60 mV/decade thermionic limit. (g and h) SS as a function of J_D in the forward and backward sweeps under various V_{BG} values. Dash lines as guides for the eye indicate the double minima of SS at V_{BG} = −80 V. (i) Minimum SS as a function of V_{BG} in the forward and backward sweeps with lines as guides for the eye.

semiconductors, the cold electron injection from Gr possesses a more localized distribution near E_F and a shorter thermal tail, which can be cut off more effectively by ϕ_b, giving rise to a faster switching to break the SS limit in principle.[28,29] It needs to be emphasized that a p-type doping in Gr is needed to enable the cold electron injection to the n-type channel, so ϕ_b varies within the energy range of E_{Dirac}−E_F. In this case, the possible hot electrons in the upper part of the Dirac cone ($E > E_{Dirac}$) can be negligible, because the cold electrons with an energy close to E_F will be the dominating and major carriers in this condition, according to the Fermi−Dirac distribution function. Similarly, one can imagine that a n-type doping in Gr is required for a p-type DSFET where ϕ_b varies within the energy range of E_F−E_{Dirac}.

To provide a quantitative comparison, we assume that $n(E_F)$ is the electron density at $E = E_F$ and calculate the normalized

carrier density, $i.e.$, $n(E)/n(E_F)$ for the monolayer Gr and 2D semiconductors, as shown in Figure 2a. Here, Gr is p-type doped and E_{Dirac}−E_F ranges from 0.1 to 0.5 eV. Assuming that a gate-controlled ϕ_b increases from 0 to 0.1 eV, $n(E)/n(E_F)$ in 2D semiconductors is reduced from 1 to 0.021. A modulation efficiency, defined as $\eta = 1 − n(E)/n(E_F)$, suggests that 97.9% electrons above E_F are cut off by ϕ_b, as shown in Figure 2b. In contrast, for the p-type doped Gr where E_{Dirac} = 0.1 eV, all the electrons above E_F are completely halted by ϕ_b, giving rise to η = 1. As the doping level increases in Gr, η slightly decreases but is still higher than that of 2D semiconductors even at E_{Dirac} = 0.5 eV. It is worth mentioning that 2D semiconductors in this comparison are considered as an extreme case in which E_F aligns with E_C as $E_F = E_C$ = 0 eV. For a more practical situation, E_C is usually higher than E_F in 2D semiconductors, and the corresponding η would be significantly lowered compared to
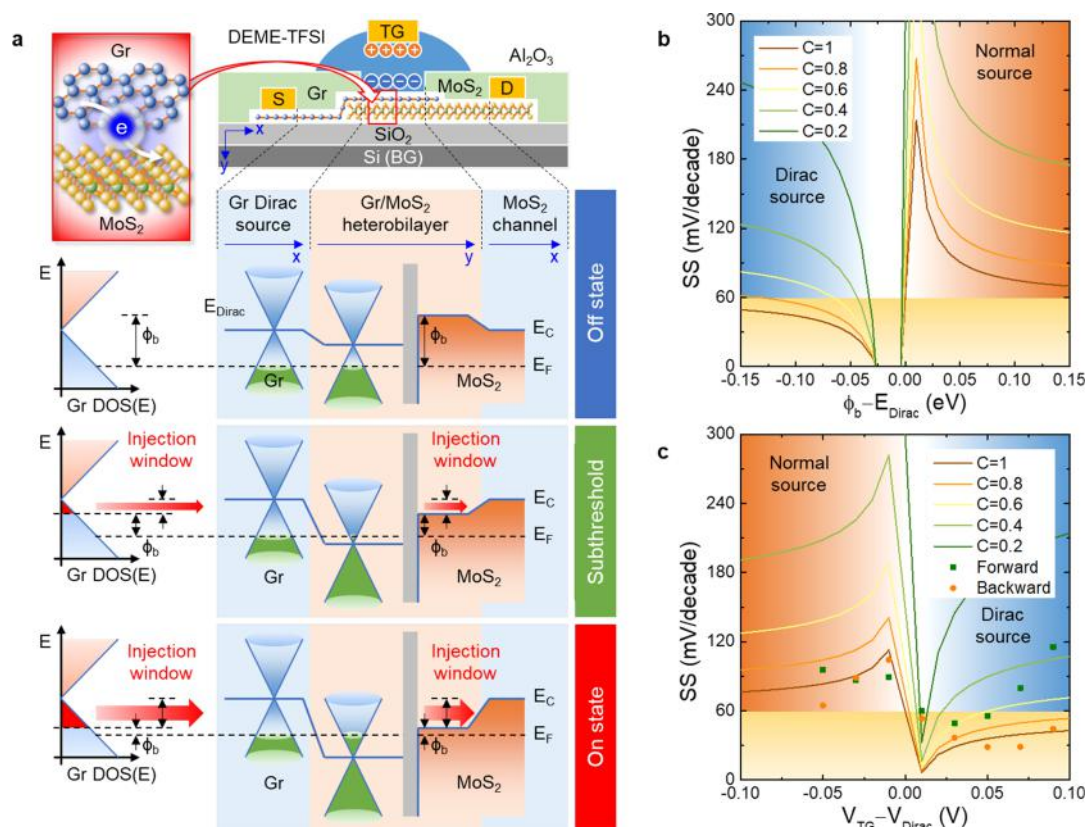
Figure 4. Operation principle of 2D MoS₂ DSFET. (a) Cross-section view of a practical device structure and the energy band diagrams along the carrier transport path for different conditions including the off state, subthreshold (dominated by the Dirac-source cold electron injection), and on state. (b) Calculated SS as a function of $\phi_b - E_{Dirac}$ at different C levels. (c) Calculated SS as a function of $V_{TG} - V_{Dirac}$ compared with the experimental results. The orange and blue backgrounds indicate the dominance of the normal-source hot electron injection and Dirac-source cold electron injection, respectively.

that in Gr. For example, assuming $E_F = 0$ eV, $E_C = 0.1$ eV, and ϕ_b increases from 0.1 to 0.2 eV, η is anticipated to be only 2.1% for 2D semiconductors.

Furthermore, when we compare the energy distribution of $n(E)/n(E_F)$ in Gr at room temperature with that in 2D semiconductors at a low temperature, it is intriguing to see that they are comparable in certain regimes, as shown in Figure 2c. To extract the effective temperature of these cold electrons in 2D semiconductors, we start with the ratio of electron density between Gr and 2D semiconductors, i.e., $n_{Gr}(E)/n_{2D}(E) \sim E_{Dirac} - E$, which strongly depends on the doping level in Gr (see Figure 2a). Considering $n_{Gr}(E) \sim (E_{Dirac} - E) \exp[(E_F - E)/k_B T_{Gr}]$ and $n_{2D}(E) \sim \exp[(E_F - E)/k_B T_{2D}]$ where T_{Gr} and T_{2D} are the electron temperatures in Gr and 2D semiconductors, respectively, the relationship between T_{Gr} and T_{2D} can be extracted as $T_{2D} = [1/T_{Gr} + k_B \ln(E_{Dirac} - E)/(E_F - E)]^{-1}$ when $n_{Gr}(E)$ equals to $n_{2D}(E)$. At $E_F = 0$ eV, T_{2D} can be further simplified as $T_{2D} = [1/T_{Gr} - k_B \ln(E_{Dirac} - E)/E]^{-1}$. Therefore, when $E_{Dirac} > E > E_F$, the electrons in Gr at room temperature ($T_{Gr} = 300$ K) can serve as the cold electrons in 2D semiconductors at a lower temperature, as shown in Figure 2d. The cooling efficiency, defined as $\gamma = 1 - T_{2D}/T_{Gr}$, can be calculated as well, as shown in Figure 2e. As the T_{Gr} rises, the γ increases accordingly, suggesting an enhanced capability of suppressing the electron thermal excitation in 2D semiconductors. One can imagine that, by implementing this Gr-enabled cold electron injection in 2D FET devices such as the monolayer MoS₂ FET, an electronic refrigeration effect can be

introduced in the electron transport. These cold electrons can equivalently lower the transport factor ($(k_B T/q) \ln 10$) and thus create an effective approach to achieve the energy-efficient steep-slope transistors, in addition to the conventional energy-filtering technique using the band-to-band Zener tunneling.

Sub-60-mV/Decade Switching of 2D MoS₂ Dirac-Source Cold Electron FET. Here, we design a 2D steep-slope Dirac-source FET (DSFET) using the monolayer Gr and MoS₂ as the cold-electron source and semiconductor channel, respectively, and experimentally demonstrate the electronic refrigeration effect and thus the outstanding sub-60-mV/decade switching performance at room temperature. A schematic of an ideal 2D MoS₂ DSFET and microscopic images of the device are illustrated in Figure 3a−c. The details of material characterization and device fabrication are provided in the Method section as well as in Figures S1 and S2. In brief, a Gr/MoS₂ heterobilayer structure is formed, followed by electrode patterning and deposition. Their electronic properties are investigated through various back-gate transistor configurations including Gr FET, MoS₂ FET, and Gr/MoS₂ FET. The entire device is passivated by a thin Al₂O₃ layer, except for the gating windows which are opened within the overlapping area and the top-gate electrode. Room-temperature ionic liquid (diethylmethyl(2-methoxyethyl) ammonium bis(trifluoromethylsulfonyl)imide, or DEME-TFSI) is drop-casted on the device to connect the top-gate electrode to the exposed Gr/MoS₂ heterobilayer area and provide a localized

high-efficiency ionic gating through an electric double layer (EDL) effect.[9,30,31]

For device characterization, the drain current density (J_D) as a function of drain voltage (V_D), back-gate voltage (V_{BG}), and top-gate voltage (V_{TG}) are measured at room temperature. First, we use the Si back gate to modulate the carrier transport. Ohmic contacts are confirmed through the J_D−V_D output characteristics in the back-gate Gr FET, MoS$_2$ FET, and Gr/MoS$_2$ FET, as shown in Figure S3. A comparison of the J_D−V_{BG} transfer characteristics is summarized in Figure 3d and Figure S4, where the maximum field-effect electron mobilitis are extracted as 4957, 24, and 66 cm^2/(V s) for the back-gate Gr FET, MoS$_2$ FET, and Gr/MoS$_2$ FET, respectively. The Gr FET shows a Dirac point at about −60 V with a weak gate modulation (an on/off ratio less than 2) due to its zero bandgap. The MoS$_2$ FET possesses a typical electron transport branch with an on/off ratio near 10^6. Similarly, the Gr/MoS$_2$ FET is dominated by the electron transport, and an intermediate on/off ratio about 10^4 was obtained. Because the hot carrier injection dominates in all three devices under the back gating, their SSs are still constrained by the thermionic limit. Then, we exploit the top gate through the localized EDL effect to precisely control the carrier transport only at the Gr/MoS$_2$ interface, and measure the J_D−V_{TG} transfer characteristics for the top-gate MoS$_2$ DSFET at different V_{BG} levels, as shown in Figure 3e. Key metrics of the transistor performance, including the SS, transconductance, electron mobility, and threshold voltage are extracted, as shown in Figures S5−S8. It is intriguing to see that a sub-60-mV/decade switching at room temperature can be obtained at V_{BG} = −80 V, and the minimum SS value can be obtained as 49 mV/decade in a forward sweep and 29 mV/decade in a backward sweep, as shown in Figure 3f. By extracting the SS as a function of J_D, the sub-60-mV/decade switching sustains for about one decade in the forward sweep and about three decades in the backward sweep, as shown in Figure 3g,h. As V_{BG} continues increasing, the minimum SS rises and stabilizes at about 210 mV/decade in the forward sweep and about 90 mV/decade in the backward sweep, as shown in Figure 3i. Besides, a strong current saturation occurs in both the forward and backward sweeps when the MoS$_2$ DSFET is operated at on state (see Figure 3e), where the on-current density is nearly constant (~10 μA/μm at V_D = 0.1 V) across a wide sweeping range (~5 V in the forward sweep and ~3 V in the backward sweep). Such independence of the gate voltage is not obtained in either the back-gate Gr FET, MoS$_2$ FET, or Gr/MoS$_2$ FET (see Figure 3d). In addition, we also note the small current peaks that locate before the subthreshold regime (−2.75 V in the forward sweep and 0.25 V in the backward sweep) and only occur at V_{BG} of −80 V. This is possibly due to the formation of the p−n junction in the monolayer Gr, which brings a double-minima (or double-dip) feature[32−34] of the drain current in the 2D MoS$_2$ DSFET.

To better understand the steep-slope switching mechanism of the 2D MoS$_2$ DSFET and its dependence on the top-gate and back-gate electric fields, an energy band diagram along the channel is illustrated in Figure 4a. The electron transport path from the source to the drain can be divided into three regions: (i) V_{BG}-controlled Gr Dirac-source region along the in-plane direction (x-axis), (ii) V_{TG}-controlled Gr/MoS$_2$ heterobilayer region along the out-of-plane direction (y-axis), and (iii) V_{BG}-controlled MoS$_2$ channel region along the in-plane direction (x-axis). To enable the cold electron injection into the n-type

MoS$_2$ channel, the Gr-source region is doped into p-type by applying a constant V_{BG} (V_{BG} < V_{Dirac}, where V_{Dirac} is the gate voltage at the Dirac point). When the MoS$_2$ DSFET is at the off state, the applied V_{TG} turns the Gr into p-type in the heterobilayer region. E_F in the p-type Gr and E_C in the n-type MoS$_2$ create a large ϕ_b at the Gr/MoS$_2$ interface to prevent the electron injection. As V_{TG} increases, both E_{Dirac} in Gr and E_C in MoS$_2$ are lowered in the heterobilayer region, resulting in a transition of Gr from p-type to n-type as well as a reduced ϕ_b. Thus, the MoS$_2$ DSFET is operated in the subthreshold regime, and the current increases due to the thermionic injection of the hot electrons that have a higher E over ϕ_b. As V_{TG} continues increasing, the E_C in MoS$_2$ becomes lower than E_F in Gr. Thus, an energy window defined as E_{Dirac}−ϕ_b is opened for the cold electron injection from the Gr source to the MoS$_2$ channel. With the expansion of the injection window, J_D increases accordingly and eventually reaches the maximum at the on state. Although the carrier transport in the subthreshold regime is still dominated by the thermionic emission over ϕ_b, the sub-60-mV/decade switching becomes possible due to the localized electron density distribution and the short Boltzmann thermal tail of the cold electrons from Gr. At the on state, because of a degenerate doping from the EDL effect,[35,36] the injection window is maximized and stabilized with the minimum ϕ_b, giving rise to a strong and steady on-current saturation even when V_{TG} continues increasing.

In addition to the sub-60-mV/decade steep slope and the strong on-current saturation, another feature of the 2D MoS$_2$ DSFET is the "double minima" in the SS during the operation (see Figure 3g,h). In the normal FET operation, the SS−J_D characteristics usually show a single valley and the minimum SS is attributed to the most efficient thermionic emission of the hot electrons over ϕ_b in the subthreshold regime. Whereas in the 2D MoS$_2$ DSFET operation, in addition to the minimum SS induced by the normal-source hot electron injection, the second valley with a sub-60-mV/decade SS occurs, owing to the Dirac-source cold electron injection. On the basis of an experimental temperature-dependent measurement, we can confirm that the cold electron injections are dominated by the thermionic emission (see Figure S9). Therefore, both the hot and cold electron injection currents can be described by the Landauer−Büttiker formula at the ballistic transport limit,[28,29,37] and the SS can be plotted as a function of ϕ_b−E_{Dirac} for a variety of C, as shown in Figure 4b. Here, $C = \partial\phi_b/\partial(qV_{TG})$ is the reciprocal body factor describing the variation of ϕ_b as a function of V_{TG} for 2D heterojunctions, and it ranges from 0 to 1. When ϕ_b > E_{Dirac}, the Gr serves as the normal source to provide the hot electrons and the SS is always larger than 60 mV/decade at room temperature. As V_{TG} increases, ϕ_b is close to E_{Dirac} and the SS approaches to infinity in principle. When ϕ_b < E_{Dirac}, the Gr acts as the Dirac source that enables the cold electron injection and allows a faster switching by breaking the SS limit. It is noted that, as C decreases, the steep-slope energy window for the cold electron injection is also reduced, but the sub-60-mV/decade switching is still feasible even at C = 0.2. Assuming that the EDL capacitance in the ionic liquid is 1 μF/cm^2,[38] the Fermi level shift (E_F−E_{Dirac}) of Gr under the top gating can be estimated[39] and the SS as a function of V_{TG}−V_{Dirac} is obtained, as shown in Figure 4c. As V_{TG} increases, both the hot electron injection and cold electron injection are predicted in succession, which are qualitatively consistent with the experimental data obtained from both the forward and backward sweeps.

To confirm the reproducibility, we also fabricate additional MoS$_2$ DSFETs with a similar device structure as shown in Figure 3. Optical microscopy images of one example device are shown in Figure S10a,b, and a summary of these device performances is shown in Figure S10c,d. We also extract the corresponding minimum SS for both the hot and cold electron injection from each device, as summarized in Table 1. From

Table 1. Summary of the Minimum SS under Hot and Cold Electron Injection in MoS$_2$ DSFETs

MoS$_2$ DSFET devices	#1	#2	#3	#4	#5
on-current saturation	yes	yes	yes	yes	yes
double-minima SS	yes	yes	yes	yes	yes
minimum SS under hot electron injection (mV/decade)	81	105	156	235	65
minimum SS under cold electron injection (mV/decade)	49	100	96	152	29

the room-temperature J_D−V_{TG} characteristics, all the devices clearly show a strong on-current saturation across a wide V_{TG} range (∼5 V). Some of the devices do not possess a sub-60-mV/decade SS, probably due to the contamination-induced degradation of the body factor in these devices. Nevertheless, a clear "double-minima" feature is obtained for all the devices. The double-minima feature is considered as the signature of the cold electron injection from the Gr Dirac source, so we can confirm that all the devices in deed follow the DSFET operation. Specifically, the first SS minima locates at a lower J_D

and corresponds to the normal-source hot carrier injection; the second SS minima locates at a higher J_D and corresponds to the Dirac-source cold electron carrier injection. The SS under the cold electron injection is always lower than that under the hot electron injection, suggesting an improved carrier transport under the same electrostatic gating condition. The repeatability of a single MoS$_2$ DSFET is also tested, as shown in Figure S11.

Owing to the ultrahigh capacitance of EDL, the body factor is assumed to be in unity in the 2D MoS$_2$ DSFETs with sub-60-mV/decade SS. This is also evidenced by the near-60-mV/decade SS achieved under the hot carrier injection. Therefore, the SS is predominated by the transport factor, as shown in Figure 5a. Because of the electronic refrigeration effect from the cold electron injection, the transport factor can be lower than 60 mV/decade at room temperature and the effective temperature (T_{eff}) of the cold electrons can be estimated from the SS. On the basis of the minimum SS of 29 mV/decade at room temperature, the lowest T_{eff} can be calculated as $T_{eff} = SSq/(k_B \ln 10) = $ ∼145 K, which corresponds to a γ of ∼52%. Furthermore, the technical core of the DSFET lies in the source-to-channel interface, whereas the core of the NCFET locates at the gate stack. Therefore, these two technologies have no conflicts in principle to be adopted on the same device. With an innovative design in the device architecture and fabrication process, it is possible to integrate both the Dirac source and ferroelectric layer in a single transistor structure, reduce the transport factor (<60 mV/decade) and body factor (<1) simultaneously, and produce a Dirac source-
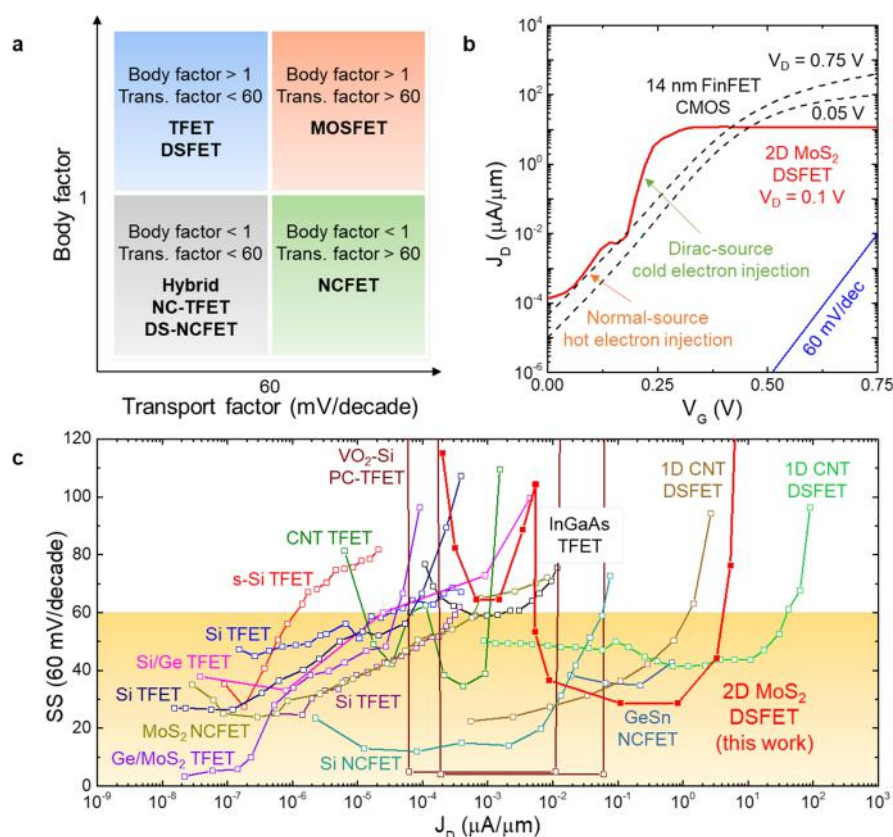

Figure 5. Benchmarking of 2D MoS$_2$ DSFET with other state-of-the-art steep-slope transistor technologies. (a) Body factor *versus* transport factor for comparing the beyond-CMOS technologies including TFET, DSFET, NCFET, hybrid NC−TFET and hybrid DS−NCFET. (a) Transfer characteristics of 2D MoS$_2$ DSFET in a comparison with 14 nm FinFET CMOS technology. (b) SS as a function of J_D in a comparison with TFETs, NCFETs, and 1D DSFETs based on a variety of channel materials.

negative capacitance (DS−NC) hybrid steep-slope FET with a superior energy-efficient performance.

Finally, we benchmark our 2D MoS$_2$ DSFET with other state-of-the-art beyond-CMOS technologies. Compared to the 14 nm Si FinFET CMOS technology,[40] the 2D MoS$_2$ DSFET shows a near-60-mV/decade SS at the beginning of the subthreshold regime owing to the hot electron injection. Then, it switches sequentially to the cold electron injection with the sub-60-mV/decade SS until the end of the subthreshold regime, as shown in Figure 5b. Although the strongly saturated on-current density is lower than that of the Si technology, it can be further improved in principle by increasing the doping level of the Gr source and thus enlarging the energy window for the cold electron injection. The sub-60-mV/decade SS of 2D MoS$_2$ DSFET is also plotted as a function of J_D in comparison with other steep-slope technologies, including the TFETs,[7,41−48] NCFETs,[12,49,50] and one-dimensional (1D) DSFETs[28] based on a variety of channel materials, as shown in Figure 5c. The 2D MoS$_2$ DSFET possesses an ultimately thin channel (∼0.65 nm for monolayer MoS$_2$) compared to the conventional bulk channel materials such as Si, Ge, InGaAs, *etc.* Furthermore, the 2D MoS$_2$ DSFET shows a superior steep-slope current density (∼4 μA/μm), which is the highest compared to any TFET and NCFET technologies based on 2D or 3D channel materials so far. Such a high sub-60-mV/decade current density in the 2D MoS$_2$ DSFET is attributed to the operation mechanism. The cold electron injection dominates until the end of the subthreshold regime where the relevant subthreshold current is high and close to the saturated on-current density, whereas the other steep-slope technologies such as the TFETs dominate only at the beginning of the subthreshold regime where the subthreshold current is relatively low. It is also worth mentioning that the sub-60-mV/decade current density of 2D MoS$_2$ DSFET only remains inferior to that of 1D carbon nanotube (CNT) DSFETs, which can be attributed to the employment of high-density CNT arrays as the channel in their case. Here, we choose the monolayer MoS$_2$ as the ultimately thin channel simply because it is the most representative 2D semiconducting material. One can easily expect that the richness of the 2D material family will further enable the performance-boosting of the 2D DSFETs, for example, by exploiting other high-mobility 2D semiconductors such as black phosphorus.

CONCLUSIONS

In this work, we investigated the Gr-enabled cold electron injection and thus the electronic refrigeration effect in monolayer MoS$_2$ and demonstrated the steep-slope 2D MoS$_2$ DSFET with an outstanding sub-60-mV/decade SS (across for three decades with the minimum SS of 29 mV/decade at room temperature), an excellent on/off ratio (∼10^7), a strong on-current saturation (∼10 μA/μm across 5 V sweeping range at V_D = 0.1 V), and more importantly, a record-high steep-slope current density (over 1 μA/μm) compared to those of any 2D- or 3D-channel-based TFETs or NCFETs. The double-minima SS in the subthreshold regime of the 2D MoS$_2$ DSFET was interpreted, which was attributed to the conventional hot electron injection with a near-60-mV/decade SS and the cold electron injection (T_{eff} of ∼145 K at room temperature) with a sub-60-mV/decade SS. Our work demonstrated the 2D DSFET as a steep-slope transistor concept for energy-efficient beyond-CMOS technology.

METHOD

Material Characterization. The Raman spectroscopy was performed by a Renishaw inVia Raman microscope. The atomic force microscopy (AFM) was performed by Bruker Dimension Icon with ScanAsyst. Both the Raman and AFM characterization confirmed the monolayer structure of MoS$_2$ and Gr (see Figure S1). Specifically, the Raman spectrum of the monolayer MoS$_2$ showed an E^1_{2g} peak at 385 cm^{-1} and an A_{1g} peak at 402 cm^{-1}. The AFM characterization of the monolayer MoS$_2$ suggests a thickness of ∼0.7 nm. For the monolayer Gr, a 2D peak at 2687 cm^{-1} and a G peak at 1587 cm^{-1} were obtained in the Raman spectrum, and the 2D/G peak intensity ratio was about 2, serving as the signature of the monolayer Gr. The AFM characterization of the monolayer Gr suggests a thickness of ∼0.6 nm. Compared to the ideal thickness value (0.34 nm for the monolayer Gr and 0.65 nm for the monolayer MoS$_2$), the difference in this work is mainly due to the polymer residues, which are induced on the sample surface during the transfer and lithography process. By combining both the Raman and AFM characterizations, we can conclude the monolayer structure of MoS$_2$ and Gr.

Device Fabrication and Measurement. The monolayer MoS$_2$ was synthesized using a customized two-zone chemical vapor deposition (CVD) system.[51] Specifically, ammonium heptamolybdate was used as a water-soluble Mo precursor and NaOH was used as a water-soluble promoter. Their mixed solution was spin-coated on a SiO$_2$/Si growth substrate. The reaction between Mo and Na produced Na$_2$MoO$_4$ compounds and then became MoS$_2$ after S vapor injection. The annealing time was optimized to control the size of the isolated monolayer triangular domains. After synthesis, the monolayer MoS$_2$ flakes were wet-transferred onto an n-type Si substrate (0.001−0.005 Ω cm) with a 285 nm SiO$_2$ layer on the surface. Then, the monolayer Gr was mechanically exfoliated from a graphite crystal (SPI Supplies Brand grade SPI-1) and transferred on top of the monolayer MoS$_2$ to form a partially overlapped heterobilayer structure. Next, multiple Ti/Au electrodes (10/90 nm) were patterned and deposited using electron-beam lithography and evaporation, serving as the source, drain, and top gate for different transistor configurations including the Gr FET, MoS$_2$ FET, Gr/MoS$_2$ FET, and MoS$_2$ DSFET (see Figure S2). Before applying the ionic liquid, a 30 nm Al$_2$O$_3$ thin film was deposited by atomic layer deposition (ALD), followed by electron-beam lithography and wet etching to create two well-confined gating windows: one on the heterobilayer and another one on the top-gate electrode. After drop-casting DEME-TFSI (727679 Sigma-Aldrich), the gating windows were connected through the ionic liquid, and a localized top-gate voltage can be applied to the exposed Gr/MoS$_2$ heterobilayer through the EDL effect.

The electrical measurements were performed in a vacuum-chamber probe station (MSTECH M5VC) with a semiconductor parameter analyzer (Keysight B1500A). The I_D was measured as a function of V_{BG}, V_{TG}, and V_D for the output and transfer characteristics. Due to the triangle shape of the monolayer MoS$_2$ domain and thus the irregular channel structure, J_D was defined as I_D divided by the length of the drain contact electrode on the MoS$_2$ layer. The back-gate sweep rate was set as ∼10 V/s, and the top-gate sweep rate was set as 1 mV/s to ensure the EDL establishment as the V_{TG} varies.[9,30,31] For both the back-gate and top-gate transfer characteristics, the measurement started from the forward

sweep, immediately followed by the backward sweep to complete a dual-sweep loop.

It is also worth mentioning that the leakage currents including both J_{BG} and J_{TG} were well-maintained at around or even less than 10^{-5} $\mu A/\mu m$ (see Figure 3d,e). The measured J_D values in the subthreshold regime were orders of magnitude higher than J_{BG} and J_{TG}. Therefore, the possible gate leakage or dielectric breakdown can be excluded from the 2D MoS_2 DSFET operation.

ASSOCIATED CONTENT

Ⓢ Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.1c01503.

> Discussions of AFM and Raman characterizations, device configurations, $J_D−V_D$ output characteristics, $J_D−V_{BG}$ transfer characteristics, calculations of subthreshold swings, transconductance characterizations, carrier mobilities in MoS_2 DSFETs, threshold voltages and hysteresis in MoS_2 DSFETs, temperature-dependent measurement, reproducibility, repeatability, theoretical calculations, doping of the Gr Dirac source, and body factor. Figures of microscopy image, Raman spectrum, AFM surface scan, height profile, schematic illustration of transistor configurations, comparison of $J_D−V_D$ output characteristics and $J_D−V_{BG}$ transfer characteristics, calculated SS in the backward sweep of the MoS_2 DSFET by using a variety of the sweep steps, comparison of transconductance characteristics, estimation of field-effect mobilities for electrons in MoS_2 DSFET, room-temperature and tempeature-dependent $J_D−V_{TG}$ transfer characteristics. (PDF)

AUTHOR INFORMATION

Corresponding Authors

Fei Yao − Department of Materials Design and Innovation, University at Buffalo, The State University of New York, Buffalo, New York 14260, United States; Email: feiyao@buffalo.edu

Huamin Li − Department of Electrical Engineering, University at Buffalo, The State University of New York, Buffalo, New York 14260, United States; ⓞ orcid.org/0000-0001-7093-4835; Email: huaminli@buffalo.edu

Authors

Maomao Liu − Department of Electrical Engineering, University at Buffalo, The State University of New York, Buffalo, New York 14260, United States

Hemendra Nath Jaiswal − Department of Electrical Engineering, University at Buffalo, The State University of New York, Buffalo, New York 14260, United States

Simran Shahi − Department of Electrical Engineering, University at Buffalo, The State University of New York, Buffalo, New York 14260, United States

Sichen Wei − Department of Materials Design and Innovation, University at Buffalo, The State University of New York, Buffalo, New York 14260, United States

Yu Fu − Department of Materials Design and Innovation, University at Buffalo, The State University of New York, Buffalo, New York 14260, United States

Chaoran Chang − Department of Materials Design and Innovation, University at Buffalo, The State University of New York, Buffalo, New York 14260, United States

Anindita Chakravarty − Department of Electrical Engineering, University at Buffalo, The State University of New York, Buffalo, New York 14260, United States

Xiaochi Liu − School of Physics and Electronics, Central South University, Changsha 410083, China

Cheng Yang − School of Physics and Electronics, Shandong Normal University, Jinan 250014, China; ⓞ orcid.org/0000-0001-7428-1819

Yanpeng Liu − Institute of Nanoscience, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China; ⓞ orcid.org/0000-0002-5265-2735

Young Hee Lee − Center for Integrated Nanostructure Physics, Institute for Basic Science, Suwon 16419, Korea; ⓞ orcid.org/0000-0001-7403-8157

Vasili Perebeinos − Department of Electrical Engineering, University at Buffalo, The State University of New York, Buffalo, New York 14260, United States; ⓞ orcid.org/0000-0002-0234-8188

Complete contact information is available at:
https://pubs.acs.org/10.1021/acsnano.1c01503

Author Contributions

F.Y. and H.L. conceived and supervised the project. M.L. and H.N.J. performed the device fabrication and measurement. M.L., S.S., A.C., and H.L. participated in the sample preparation. S.W., Y.F., and C.C. synthesized the monolayer MoS_2 and performed the material characterization. X.L., C.Y., Y.L., Y.H.L., and V.P. participated in the data analysis.

Notes

The authors declare no competing financial interest.

REFERENCES

(1) Ionescu, A. M.; Riel, H. Tunnel Field-Effect Transistors as Energy-Efficient Electronic Switches. *Nature* **2011**, *479*, 329−337.

(2) Seabaugh, A. C.; Zhang, Q. Low-Voltage Tunnel Transistors for beyond CMOS Logic. *Proc. IEEE* **2010**, *98*, 2095−2110.

(3) Jena, D. Tunneling Transistors Based on Graphene and 2-D Crystals. *Proc. IEEE* **2013**, *101*, 1585−1602.

(4) Khan, A. I.; Chatterjee, K.; Wang, B.; Drapcho, S.; You, L.; Serrao, C.; Bakaul, S. R.; Ramesh, R.; Salahuddin, S. Negative Capacitance in a Ferroelectric Capacitor. *Nat. Mater.* **2015**, *14*, 182−186.

(5) Wong, J. C.; Salahuddin, S. Negative Capacitance Transistors. *Proc. IEEE* **2019**, *107*, 49−62.

(6) Wang, X.; Yu, P.; Lei, Z.; Zhu, C.; Cao, X.; Liu, F.; You, L.; Zeng, Q.; Deng, Y.; Zhu, C.; Zhou, J.; Fu, Q.; Wang, J.; Huang, Y.; Liu, Z. van der Waals Negative Capacitance Transistors. *Nat. Commun.* **2019**, *10*, 3037.

(7) Sarkar, D.; Xie, X.; Liu, W.; Cao, W.; Kang, J.; Gong, Y.; Kraemer, S.; Ajayan, P. M.; Banerjee, K. A Subthermionic Tunnel Field-Effect Transistor with an Atomically Thin Channel. *Nature* **2015**, *526*, 91−95.

(8) Balaji, Y.; Smets, Q.; de la Rosa, C. J. L.; Lu, A. K. A.; Chiappe, D.; Agarwal, T.; Lin, D.; Huyghebaert, C.; Radu, I.; Mocuta, D.; Groeseneken, G. Tunneling Transistors Based on MoS$_2$/MoTe$_2$ van der Waals Heterostructures. *IEEE J. Electron Devices Soc.* **2018**, *6*, 1048−1055.

(9) Liu, X.; Qu, D.; Li, H.-M.; Moon, I.; Ahmed, F.; Kim, C.; Lee, M.; Choi, Y.; Cho, J. H.; Hone, J. C.; Yoo, W. J. Modulation of Quantum Tunneling *via* a Vertical Two-Dimensional Black Phosphorus and Molybdenum Disulfide *p*−*n* Junction. *ACS Nano* **2017**, *11*, 9143−9150.

(10) Roy, T.; Tosun, M.; Cao, X.; Fang, H.; Lien, D.-H.; Zhao, P.; Chen, Y.-Z.; Chueh, Y.-L.; Guo, J.; Javey, A. Dual-Gated MoS2/WSe$_2$ van der Waals Tunnel Diodes and Transistors. *ACS Nano* **2015**, *9*, 2071−2079.

(11) Si, M.; Su, C.-J.; Jiang, C.; Conrad, N. J.; Zhou, H.; Maize, K. D.; Qiu, G.; Wu, C.-T.; Shakouri, A.; Alam, M. A.; Ye, P. D. Steep Slope Hysteresis-Free Negative Capacitance MoS$_2$ Transistors. *Nat. Nanotechnol.* **2018**, *13*, 24−29.

(12) Yu, Z.; Wang, H.; Li, W.; Xu, S.; Song, X.; Wang, S.; Wang, P.; Zhou, P.; Shi, Y.; Chai, Y.; Wang, X. Negative Capacitance 2D MoS$_2$ Transistors with Sub-60mV/dec Subthreshold Swing over 6 Orders, 250 μA/μm Current Density, and Nearly-Hysteresis-Free. *63rd IEEE International Electron Devices Meeting, IEDM 2017*, San Francisco, CA, December 2−6, 2017.

(13) McGuire, F. A.; Lin, Y.-C.; Price, K.; Rayner, G. B.; Khandelwal, S.; Salahuddin, S.; Franklin, A. D. Sustained Sub-60 mV/Decade Switching *via* the Negative Capacitance Effect in MoS$_2$ Transistors. *Nano Lett.* **2017**, *17*, 4801−4806.

(14) Avci, U. E.; Morris, D. H.; Young, I. A. Tunnel Field-Effect Transistors: Prospects and Challenges. *IEEE J. Electron Devices Soc.* **2015**, *3*, 88−95.

(15) Seabaugh, A.; Alessandri, C.; Heidarlou, M. A.; Li, H.-M.; Liu, L.; Lu, H.; Fathipour, S.; Paletti, P.; Pandey, P.; Ytterdal, T. Steep Slope Transistors: Tunnel FETs and Beyond. *2016 46th European Solid-State Device Research Conference (ESSDERC)*, Lausanne, Switzerland, September 12−15, 2016.

(16) Vandenberghe, W. G.; Verhulst, A. S.; Sorée, B.; Magnus, W.; Groeseneken, G.; Smets, Q.; Heyns, M.; Fischetti, M. V. Figure of Merit for and Identification of Sub-60 mV/Decade Devices. *Appl. Phys. Lett.* **2013**, *102*, 013510.

(17) Hoffmann, M.; Slesazeck, S.; Schroeder, U.; Mikolajick, T. What's Next for Negative Capacitance Electronics? *Nat. Electron.* **2020**, *3*, 504−506.

(18) Cao, W.; Banerjee, K. Is Negative Capacitance FET a Steep-Slope Logic Switch? *Nat. Commun.* **2020**, *11*, 196.

(19) Alam, M. A.; Si, M.; Ye, P. D. A Critical Review of Recent Progress on Negative Capacitance Field-Effect Transistors. *Appl. Phys. Lett.* **2019**, *114*, 090401.

(20) Chang, S.-C.; Avci, U. E.; Nikonov, D. E.; Young, I. A. A Thermodynamic Perspective of Negative-Capacitance Field-Effect Transistors. *IEEE J. Explor. Solid-State Computat. Dev. Circuits* **2017**, *3*, 56−64.

(21) Novoselov, K. S.; Mishchenko, A.; Carvalho, A.; Castro Neto, A. H. 2D Materials and van der Waals Heterostructures. *Science* **2016**, *353*, aac9439.

(22) Wang, Q. H.; Kalantar-Zadeh, K.; Kis, A.; Coleman, J. N.; Strano, M. S. Electronics and Optoelectronics of Two-Dimensional Transition Metal Dichalcogenides. *Nat. Nanotechnol.* **2012**, *7*, 699−712.

(23) Yoon, Y.; Ganapathi, K.; Salahuddin, S. How Good Can Monolayer MoS$_2$ Transistors Be? *Nano Lett.* **2011**, *11*, 3768−3773.

(24) Li, X.; Yang, L.; Si, M.; Li, S.; Huang, M.; Ye, P.; Wu, Y. Performance Potential and Limit of MoS$_2$ Transistors. *Adv. Mater.* **2015**, *27*, 1547−1552.

(25) Alam, K.; Lake, R. K. Monolayer MoS$_2$ Transistors beyond the Technology Road Map. *IEEE Trans. Electron Devices* **2012**, *59*, 3250−3254.

(26) Resta, G. V.; Leonhardt, A.; Balaji, Y.; De Gendt, S.; Gaillardon, P.-E.; De Micheli, G. Devices and Circuits Using Novel 2-D Materials: A Perspective for Future VLSI Systems. *IEEE Trans. Very Large Scale Integration (VLSI) Syst.* **2019**, *27*, 1486−1503.

(27) Di Bartolomeo, A. Graphene Schottky Diodes: An Experimental Review of the Rectifying Graphene/Semiconductor Heterojunction. *Phys. Rep.* **2016**, *606*, 1−58.

(28) Qiu, C. G.; Liu, F.; Xu, L.; Deng, B.; Xiao, M. M.; Si, J.; Lin, L.; Zhang, Z. Y.; Wang, J.; Guo, H.; Peng, H. L.; Peng, L. M. Dirac-Source Field-Effect Transistors as Energy-Efficient, High-Performance Electronic Switches. *Science* **2018**, *361*, 387−391.

(29) Liu, F.; Qiu, C.; Zhang, Z.; Peng, L.-M.; Wang, J.; Guo, H. Dirac Electrons at the Source: Breaking the 60-mV/Decade Switching Limit. *IEEE Trans. Electron Devices* **2018**, *65*, 2736−2743.

(30) Li, H.-M.; Xu, K.; Bourdon, B.; Lu, H.; Lin, Y.-C.; Robinson, J. A.; Seabaugh, A. C.; Fullerton-Shirey, S. K. Electric Double Layer Dynamics in Poly(ethylene Oxide) LiClO$_4$ on Graphene Transistors. *J. Phys. Chem. C* **2017**, *121*, 16996−17004.

(31) Alessandri, C.; Fathipour, S.; Li, H.; Kwak, I.; Kummel, A.; Remskar, M.; Seabaugh, A. C. Reconfigurable Electric Double Layer Doping in an MoS$_2$ Nanoribbon Transistor. *IEEE Trans. Electron Devices* **2017**, *64*, 5217−5222.

(32) Bartolomeo, A. D.; Giubileo, F.; Santandrea, S.; Romeo, F.; Citro, R.; Schroeder, T.; Lupina, G. Charge Transfer and Partial Pinning at the Contacts as the Origin of a Double Dip in the Transfer Characteristics of Graphene-Based Field-Effect Transistors. *Nanotechnology* **2011**, *22*, 275702.

(33) Feng, T.; Xie, D.; Xu, J.; Zhao, H.; Li, G.; Ren, T.; Zhu, H. Back-Gate Graphene Field-Effect Transistors with Double Conductance Minima. *Carbon* **2014**, *79*, 363−368.

(34) Liang, J.; Xu, K.; Arora, S.; Laaser, J. E.; Fullerton-Shirey, S. K. Ion-Locking in Solid Polymer Electrolytes for Reconfigurable Gateless Lateral Graphene *p*-*n* Junctions. *Materials* **2020**, *13*, 1089.

(35) Paletti, P.; Yue, R.; Hinkle, C.; Fullerton-Shirey, S. K.; Seabaugh, A. Two-Dimensional Electric-Double-Layer Esaki Diode. *npj 2D Mater. Appl.* **2019**, *3*, 19.

(36) Alessandri, C.; Fathipour, S.; Li, H.; Kwak, I.; Kummel, A.; Remskar, M.; Seabaugh, A. C. Reconfigurable Electric Double Layer Doping in an MoS$_2$ Nanoribbon Transistor. *IEEE Trans. Electron Devices* **2017**, *64*, 5217−5222.

(37) Britnell, L.; Gorbachev, R. V.; Jalil, R.; Belle, B. D.; Schedin, F.; Mishchenko, A.; Georgiou, T.; Katsnelson, M. I.; Eaves, L.; Morozov, S. V.; Peres, N. M. R.; Leist, J.; Geim, A. K.; Novoselov, K. S.; Ponomarenko, L. A. Field-Effect Tunneling Transistor Based on Vertical Graphene Heterostructures. *Science* **2012**, *335*, 947−950.

(38) Zhang, Y.; Ye, J.; Matsuhashi, Y.; Iwasa, Y. Ambipolar MoS$_2$ Thin Flake Transistors. *Nano Lett.* **2012**, *12*, 1136−1140.

(39) Wang, F.; Zhang, Y.; Tian, C.; Girit, C.; Zettl, A.; Crommie, M.; Shen, Y. R. Gate-Variable Optical Transitions in Graphene. *Science* **2008**, *320*, 206−209.

(40) Natarajan, S.; Agostinelli, M.; Akbar, S.; Bost, M.; Bowonder, A.; Chikarmane, V.; Chouksey, S.; Dasgupta, A.; Fischer, K.; Fu, Q.; Ghani, T.; Giles, M.; Govindaraju, S.; Grover, R.; Han, W.; Hanken, D.; Haralson, E.; Haran, M.; Heckscher, M.; Heussner, R. et al. A 14 nm Logic Technology Featuring 2nd-Generation FinFET, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588 μm^2 SRAM Cell Size. *Proc. 2014 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, December 15−17, 2014.

(41) Dewey, G.; Chu-Kung, B.; Boardman, J.; Fastenau, J. M.; Kavalieros, J.; Kotlyar, R.; Liu, W. K.; Lubyshev, D.; Metz, M.; Mukherjee, N.; Oakey, P.; Pillarisetty, R.; Radosavljevic, M.; Then, H. W.; Chau, R. Fabrication, Characterization, and Physics of III−V Heterojunction Tunneling Field Effect Transistors (H-TFET) for Steep Sub-Threshold Swing. *Proc. 2011 IEEE International Electron Devices Meeting (IEDM)*, Washington, DC, December 5−7, 2011.

(42) Gandhi, R.; Chen, Z.; Singh, N.; Banerjee, K.; Lee, S. CMOS-Compatible Vertical-Silicon-Nanowire Gate-All-Around *p*-Type Tunneling FETs with ≤ 50-mV/Decade Subthreshold Swing. *IEEE Electron Device Lett.* **2011**, *32*, 1504−1506.

(43) Jeon, K.; Loh, W.-Y.; Patel, P.; Kang, C. Y.; Oh, J.; Bowonder, A.; Park, C.; Park, C. S.; Smith, C.; Majhi, P.; Tseng, H.; Jammy, R.; Liu, T. K.; Hu, C. Si Tunnel Transistors with a Novel Silicided Source and 46 mV/dec Swing. *2010 Symposium on VLSI Technology*, Honolulu, HI, June 15−17, 2010.

(44) Kim, S. H.; Kam, H.; Hu, C.; Liu, T.-J. K. Germanium-Source Tunnel Field Effect Transistors with Record High I_{ON}/I_{OFF}. *2009 Symposium on VLSI Technology*, Kyoto, Japan, June 15−17, 2009.

(45) Knoll, L.; Zhao, Q.-T.; Nichau, A.; Trellenkamp, S.; Richter, S.; Schafer, A.; Esseni, D.; Selmi, L.; Bourdelle, K. K.; Mantl, S. Inverters with Strained Si Nanowire Complementary Tunnel Field-Effect Transistors. *IEEE Electron Device Lett.* **2013**, *34*, 813−815.

(46) Lu, Y.; Bangsaruntip, S.; Wang, X.; Zhang, L.; Nishi, Y.; Dai, H. DNA Functionalization of Carbon Nanotubes for Ultrathin Atomic Layer Deposition of High-*κ* Dielectrics for Nanotube Transistors with 60 mV/decade Switching. *J. Am. Chem. Soc.* **2006**, *128*, 3518−3519.

(47) Mori, T.; Yasuda, T.; Fukuda, K.; Morita, Y.; Migita, S.; Tanabe, A.; Maeda, T.; Mizubayashi, W.; O'uchi, S.-I.; Liu, Y.; Masahara, M.; Miyata, N.; Ota, H. Unexpected Equivalent-Oxide-Thickness Dependence of the Subthreshold Swing in Tunnel Field-Effect Transistors. *Appl. Phys. Express* **2014**, *7*, 024201.

(48) Casu, E. A.; Vitale, W. A.; Oliva, N.; Rosca, T.; Biswas, A.; Alper, C.; Krammer, A.; Luong, G. V.; Zhao, Q. T.; Mantl, S.; Schuler, A.; Seabaugh, A.; Ionescu, A. M. Hybrid Phase-Change — Tunnel FET (PC-TFET) Switch with Subthreshold Swing < 10mV/Decade and Sub-0.1 Body Factor: Digital and Analog Benchmarking. *2016 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, December 3−7, 2016.

(49) Zhou, J.; Han, G.; Peng, Y.; Liu, Y.; Zhang, J.; Sun, Q.-Q.; Zhang, D. W.; Hao, Y. Ferroelectric Negative Capacitance GeSn PFETs with Sub-20 mV/Decade Subthreshold Swing. *IEEE Electron Device Lett.* **2017**, *38*, 1157−1160.

(50) Liu, C.; Chen, H.-H.; Hsu, C.-C.; Fan, C.-C.; Hsu, H.-H.; Cheng, C.-H. Negative Capacitance CMOS Field-Effect Transistors with Non-Hysteretic Steep Sub-60mV/dec Swing and Defect-Passivated Multidomain Switching. *2019 Symposium on VLSI Technology*, Kyoto, Japan, June 9−14, 2019.

(51) Kim, H.; Han, G. H.; Yun, S. J.; Zhao, J.; Keum, D. H.; Jeong, H. Y.; Ly, T. H.; Jin, Y.; Park, J.-H.; Moon, B. H.; Kim, S.-W.; Lee, Y. H. Role of Alkali Metal Promoter in Enhancing Lateral Growth of Monolayer Transition Metal Dichalcogenides. *Nanotechnology* **2017**, *28*, 36LT01.