ESD Stress Effect on Failure Mechanisms in GaN-on-Si Power Device

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***Abstract*—This paper reports investigation of failure mechanisms of GaN-on-Si power device under electrostatic discharge (ESD) stress using on-wafer transmission-line pulse (TLP) testing. Hot-hole injections under the gate and filament formation in the buffer layer are examined by monitoring the threshold voltage (V_{th}) and on-resistance (R_{on}) subjected to a floating gate or an off-state gate voltage. Distinct and continued degradation has been observed after the ESD stress is removed indicating a slow de-trapping process due to deep-level buffer traps. Finally, 2D device simulation is used to probe the physical insight into failure mechanisms.**

***Index Terms*—Buffer traps, electrostatic discharge, failure mechanisms, GaN-on-Si, transmission-line pulse.**

I. Introduction

GALLIUM nitride-based devices have emerged as the leading candidate for high-voltage electronics. Material characteristics such as large critical fields, high electron mobility, and excellent thermal conductivity enable low on-resistance R_{on} and high breakdown voltages in GaN high-electron-mobility transistors (HEMTs) [1]–[3]. Because of its compatibility to CMOS process, the GaN-on-Si integration platform is an excellent choice for high power applications with electrostatic discharge (ESD) protection [4], [5]. Nevertheless, the reliability issues in the monolithic GaN platform still pose a challenge for commercialization of power electronics [6], [7]. Currently, GaN device reliability standards are based on Si laterally diffused metal oxide semiconductor (LDMOS) transistor failure models, which do not often transfer to GaN-on-Si power devices [8]. Therefore, the reliability mechanisms including time-dependent dielectric breakdown (TDDB), negative/positive-bias temperature instability (NBTI/PBTI), and electrostatic discharge (ESD) need more attention.

Recently, there has been some progress in studying TDDB and BTI failure mechanisms in GaN-on-Si devices [9], [10]. With higher integration in GaN power electronics, the potential failure and reliability of GaN ESD devices should be evaluated. The physical mechanism in GaN power devices under ESD events, however, is still debatable. The electromigration between the contact and III/V semiconductor destroys the Schottky barriers with increased leakage current after ESD events [11]. Some literature indicates that the ESD robustness of GaN devices is related to trap distribution in the buffer layer with electric field crowding [12]. The ESD behavior under transmission line pulse (TLP) and very-fast transmission line pulse (VFTLP) has been evaluated by applying different substrate biases [13], [14]. Furthermore, the evolution of mechanical stress in GaN devices is also regarded to as a source of failure after ESD stress [15]. Nevertheless, the understanding of device degradations subjected to ESD is still lacking.

In this paper, the device degradations during the ESD stress before failure are investigated. Although both threshold voltage V_{th} and on-resistance increase with the transmission line pulse number and stress voltage, an un-expected reduction in V_{th} under a floating gate is observed, suggesting two different failure mechanisms exist under different ESD stress conditions. The hot-hole injection is strengthened by applying an off-state gate voltage during TLP stress, resulting in a monotonic decrease in V_{th}. The insight of filament formation and the de-trapping process of deep-level buffer traps under the stress and restore phases have been analyzed by examining the measured leakage current and device simulation results.

II. Device and Stress Characterization

GaN devices examined in this work are normally on HEMTs fabricated on p-type silicon (111) substrate. A cross-section is shown in Fig. 1(a). The epitaxial layers on top of the silicon substrate containing a graded AlGaN buffer with Carbon doping and a GaN layer followed by an $Al_{0.3}Ga_{0.7}N$ barrier layer. An extra GaN cap layer has been deposited above the barrier layer to increase the mobility of the two-dimensional electron gas (2DEG) and decrease the surface leakage current. A SiN passivation layer has been deposited by plasma enhanced chemical vapor deposition (PECVD) to suppress the current collapse. The drain and source contacts were formed using Ti/Al/Ni/Au metallization and the gate contact uses Ni/Au. I_{ds}-V_{gs} and I_{ds}-V_{ds} are shown in Fig. 1(b) and Fig. 1(c), respectively. The threshold voltage V_{th} is extracted as the

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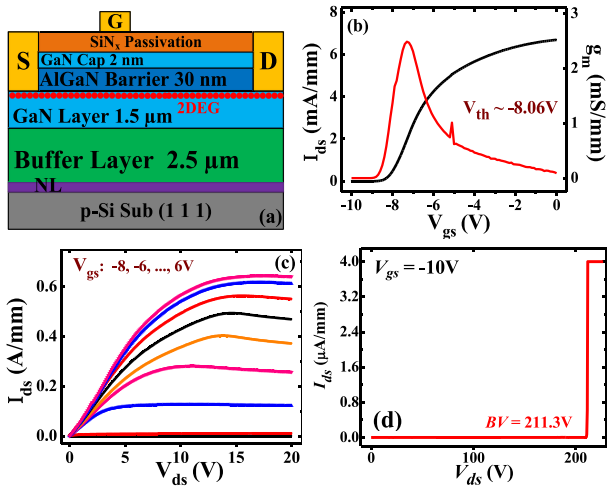

Fig. 1. (a) Cross-section of a GaN power device with $L_{gd}/L_g/L_{gs}$ = 5/2/10 μm and width = 100 μm, (b) I_{ds}-V_{gs}, (c) I_{ds}-V_{ds} curves, and (d) off-state breakdown characteristic.

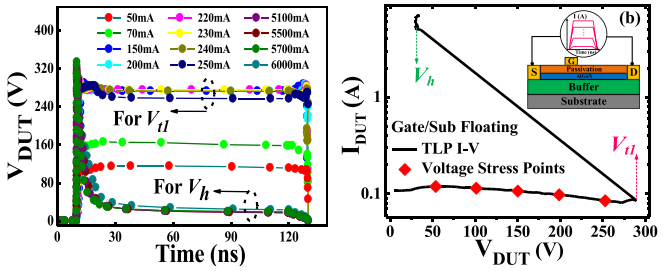

Fig. 2. (a) The corresponding TLP voltage versus time with different current pulses and (b) obtained TLP *I-V* curve. The gate is floating.

voltage where the slope of transconductance (g_m) reaches its maximum point.

The Barth 4002 TLP system was utilized to evaluate the device ESD characteristics. The corresponding TLP voltage versus time with different current pulses and an example snap-back *I-V* curve of the GaN-on-Si power devices under TLP measurement with 120ns pulse-width, 10ns rise time, and 10ns fall time is shown in Fig. 2. The first snap-back point at the TLP *I-V* curve is defined as the trigger voltage V_{t1} which refers to the largest sustainable voltage under ESD pulsed and the second snap-back point is defined as the holding voltage V_h which means that the second current path has been established with a lower voltage and higher current in the measuring device.

In order to monitor the device degradation, different electrical stresses leading to the trigger voltage have been applied using sequential rectangular pulses generated by the Barth TLP system. After each stress cycle, on-the-fly measurement is performed using a Keithley 4200A Semiconductor Characterization System to avoid the recovery effect [16]. In order to investigate different trap mechanisms relating to ESD stress, different gate conditions are selected to examine the surface traps at lower current density [17]. The Keithley 2461A is used to supply the gate bias. To further explore the failure mechanisms under ESD events, the restore behavior has been studied experimentally. The restore phase is defined when the TLP stress is removed while the DC characteristics are monitored at the interval of a specific time for ten minutes. This was followed by an accelerated restore cycle under white light illumination for one minute with immediate dark characterization afterward.

III. TLP Stress Under a Floating Gate

In the normal operating condition of ESD protection devices, the drain and source are connected to protected components while the gate is left floating. In order to mimic this operating condition, the TLP voltage ranging from 50V to 250V has been applied to the measured devices. The V_{th} shift as a function of the number of TLP pulses and voltage is shown in Fig. 3(a). An unexpected reduction in V_{th} is observed at the beginning of the 50V and 100V TLP stress voltage. However, when the total ESD pulses exceed 15 at low TLP voltage or the pulse voltage exceeds 100V, a linear increase in V_{th} is displayed. Although a decrease in V_{th} has been seen under low TLP stress, the monotonic increase in R_{on} is shown in Fig. 3(b) with increased number of TLP pulses and voltage. The experimental data indicate that there are two different failure mechanisms between low and high TLP pulse voltages. Under low TLP pulse stress, the hot-hole injection mechanism with negative charge accumulation underneath the gate region may increase the Schottky gate barrier height and decreases V_{th}. But under high TLP pulse stress, a filament formation in the buffer layer interacts with deep-level buffer traps that could introduce the 2DEG depletion to enhance V_{th} and R_{on} degradations.

It is interesting to note that V_{th} and R_{on} increase significantly during the restore phase after removing the TLP stress. The cumulative degradation is attributed to the deep-level acceptor-like buffer traps with a slow de-trapping process [18]. The accumulated holes induced by the filament formation in the buffer layer cannot be de-trapped immediately by the acceptor-like buffer traps in the restore phase where the hole-trapping results in continued V_{th} and R_{on} degradations. In addition, the V_{th} degradation saturates under the restore phase, indicating an equilibrium between generation and recombination of holes in the buffer layer and hot-hole injection under the gate region. The un-saturated R_{on} degradation during the restore phase suggests that the filament formation is the dominant mechanism contributing to R_{on} degradation under stress.

The white illumination annealing (a common method for the defect annealing) is applied to verify the hot-hole mechanisms after the restore phase [19]. By providing electrons from the photons, an enormous recovery in V_{th} and R_{on} is observed after the device is exposed to white light for 60 seconds. However, Fig. 3(c) shows that white light cannot recover the V_{th} degradation completely due to the damage from hot-hole injection resulting in numerous traps in the passivation layer. R_{on} recovery is more successful for restoring the device by recombining hole filaments with acceptor-like buffer traps.

According to the experimental results, the filament formation is one of the dominant failure mechanisms under ESD stress. But the exact location still needs to be determined by

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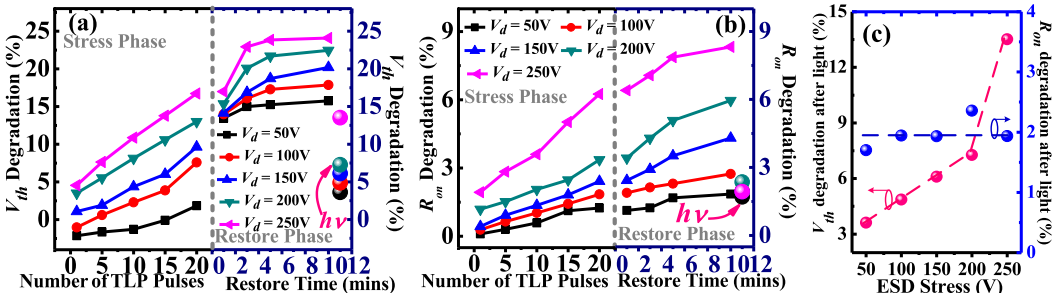

Fig. 3. Measured (a) V_{th}, (b) R_{on} degradations under stress and restore phases for different V_d voltages, and (c) V_{th} and R_{on} after white light illumination under different ESD stress voltages. The gate is floating.

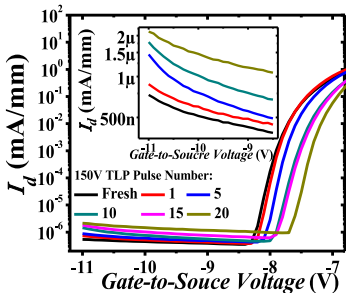

Fig. 4. I_d-V_{gs} curves for different pulse numbers of the GaN power device with a floating gate.

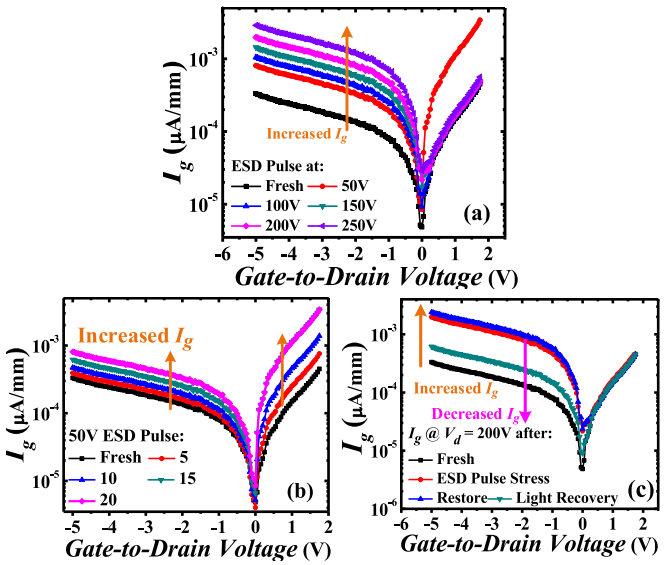

Fig. 5. (a) I_g-V_{gd} curves under different stress voltages at the end of stress phase, (b) I_g-V_{gd} curves under 50V ESD stress for different number of pulses, and (c) I_g-V_{gd} curves under 200V ESD stress for different stress or restore conditions. The gate is left floating.

additional experiments. The transfer characteristics after each TLP stress cycle, which are measured under 150V of TLP stress, are shown in Fig. 4, where off state drain leakage current is inserted. The increased off state drain leakage current with an increase in the number of pulses indicates that there is a leakage current path between the drain and the gate region. A highly conducting hole accumulation path is formed after high TLP stress, introducing an increase in the drain leakage current [20]. The filament formation also enhances the 2DEG depletion process with increased R_{on} degradation.

To verify the two different failure mechanisms discussed above, Fig. 5 shows the I_g shift measured under different TLP conditions. In Fig. 5(a) I_g increases with positive gate-to-drain voltage (V_{gd}) for increasing TLP voltage except when the TLP stress voltage is equal to 50V. I_g increases significantly with negative V_{gd}, attributing to the increased conduction in the buffer layer. It is worth noting that I_g shows a unique increase with positive V_{gd} under the 50V ESD stress as shown in Fig. 5(b). The increased I_g in both positive and negative V_{gd}'s indicates that two mechanisms happen before 20 TLP stress pulses, while the hot-hole injection plays a dominant role in the degradation [22]. The I_g -V_{gd} under different test conditions (fresh, ESD pulse stress, restore, and restore with light) is displayed in Fig. 5(c). The results in Fig. 5(c) imply that the hole filament formation under large TLP voltage and long stress time. Particularly, a small I_g increase in the restore phase reveals that the rate of hole-trapping is larger than that of hole depletion for the deep-level acceptor-like buffer traps. The deep-level acceptor-like traps are neutralized under white light illumination with decreased I_g under negative V_{gd}.

IV. TLP Stress Under an Off-State Gate

In order to further investigate the trap mechanisms relating to TLP stress in GaN power devices, an off state gate voltage at −10V is applied during the TLP stress. The revolution between V_{th} and R_{on} degradations and the TLP pulses is shown in Fig. 6. Compared to that of a floating gate, V_{th} decreases (or negative V_{th} degradation) under the TLP stress. With a lower Schottky gate barrier height between the gate contact and dielectric layer induced by the off-state gate voltage, the hot-hole injection in the gate region is the governing mechanism resulting in a negative V_{th} degradation. However, V_{th} degradation reverses its direction when the stress voltage of TLP increases. This suggests that the filament formation in the buffer region has a large impact on the V_{th} degradation at high EDS stress voltage.

The enhanced hot-hole injection from the off-state bias indicates that the hot-hole injection and filament formation in the buffer layer are responsible for the V_{th} degradations under high EDS stress voltage. A similar R_{on} degradation is shown in Fig. 6(b). Considering that the R_{on} is dependent on the 2DEG density. The negative R_{on} degradation is related to the

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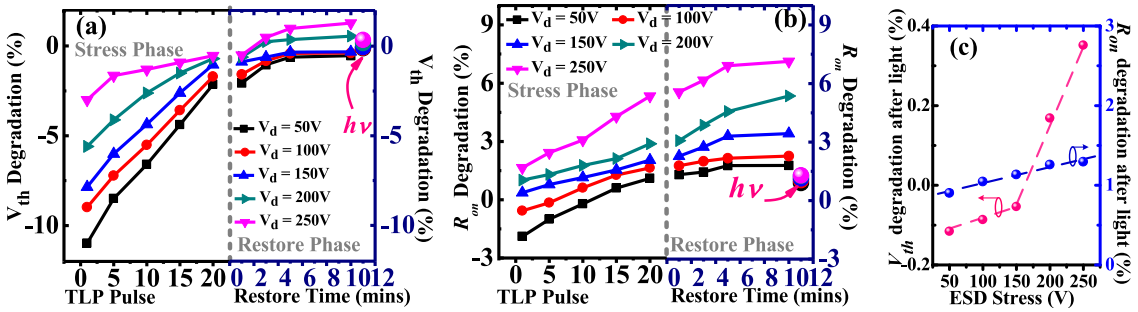

Fig. 6. Measured (a) V_{th}, (b) R_{on} degradations under stress and restore phases with different voltage stresses, and (c) V_{th} and R_{on} after white light illumination subjected to different ESD stress voltages. The gate is at an off state gate voltage.

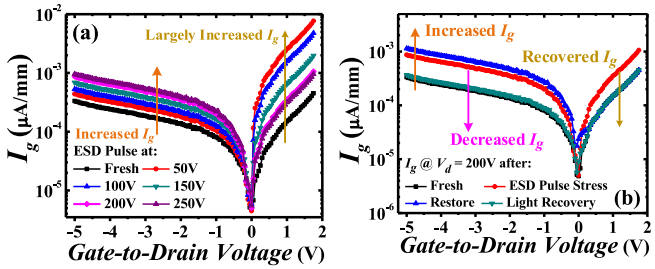

Fig. 7. (a) I_g-V_{gd} curves under different stress voltages at the end of the stress phase and (b) I_g-V_{gd} curves under 200V ESD stress at different conditions. The gate is at an off state gate voltage.

compensated 2DEG under the gate and the depleted 2DEG between the gate and drain. Overall, the R_{on} is affected by both hot-hole injection under the gate and the filament formation between the gate and drain region.

In the restore phase, the V_{th} could reach nearly its original value under low TLP stress voltage. This is due to the hot-hole injection is fast charging process with temporary damage in the dielectric layer. Nonetheless, a slight increase in V_{th} and R_{on} is shown in the restore phase under high TLP stress voltage. This suggests that the deep-level buffer traps cannot be recombined in short time after removing the TLP stress. An enormous recovery in both V_{th} and R_{on} is shown after the device is exposed to one minute of white light. Under low TLP stress voltage, the V_{th} can be fully recovered due to the fast-charging process of hot-hole injection. Under high TLP stress voltage, however, the V_{th} cannot be fully recovered due to the deep-level buffer traps. Similar behavior is also seen in the R_{on} recovery.

The gate leakage current for different TLP stress conditions under an off state gate voltage is illustrated in Fig. 7. Similar to that of a floating gate, I_g increases with V_{gd} when the ESD stress voltage increases (see Fig. 7(a)). However, I_g also increases with positive V_{gd} noticeably. The I_g-V_{gd} subjected to different conditions (fresh, ESD stress, restore, and restore with light) under the 200V TLP stress is shown in Fig. 7(b). The increased I_g at positive V_{gd} is recovered after the TLP stress is removed, while the I_g at negative V_{gd} shows an abnormal increase at the restore phase. This may imply that the hot-hole injection is related to the fast-charging process, and the filament formation is correlated to the deep-level buffer traps, which cannot be recombined in short time. The white light illumination provides more energy for the ionized buffer traps to be neutralized in decreased I_g for negative V_{gd}. And the recovery level of R_{on} degradation after white light illumination is dependent on the TLP stress voltage.

V. TCAD Device Simulation

The Sentaurus device simulation is used to probe the physical insight into the trap mechanism relating to observed dynamic resistance degradation from the experiment. The AlGaN/GaN device structure shown in Fig. 1(a) is used in simulation. The simulation model of ESD behavior in semiconductor devices attracts extensive attention [23], [24]. To analyze the performance of the measured GaN power devices, the TLP multiple-pulse simulation method is adopted [25]–[27]. This method is similar to the actual TLP test: a series of current pulses with increasing amplitude, 10 ns of rising time, 100 ns of a duration time, and 10 ns of fall time are applied to the source and drain sides. Then a series of voltage pulses can be obtained, each current pulse and the average of 70%-90% of the corresponding voltage will constitute a point of the TLP I-V curve. By implementing the mixed-mode stress measurement, the device parameters after a special number of TLP pulses are characterized to mimic the degradation of the simulated devices. The source and drain contacts use heavily doped GaN to form ohmic contacts. High-field mobility saturation model and inverse piezoelectric effect are adjusted to improve the simulation accuracy compared with the experimental results. The polarization scale parameter used in the simulation is 0.29 to be consistent with the experimental data [18]. Shockley-Read-Hall and dynamic nonlocal path Trap-assisted Tunneling Model are enabled to simulate the trapping and de-trapping mechanisms under different TLP stresses. The self-heating effect including the lattice temperature model and electron/hole thermal model is enabled to monitor possible hole/electron emission processes. The buffer layer is set as a low mole-fraction AlGaN to duplicate graded buffer layers in fabrication. In the device simulation, Gaussian distribution with the peak density of 10^{19} cm^{-3} shallow donors in the Carbon-doping buffer layer is implemented. As shown in [18], trapping phenomena in the Carbon-doped buffer layer can be reproduced by adopting deep-level acceptor-like traps with a concentration almost two orders of magnitude lower than that at the nominal Carbon

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TABLE I
KEY PARAMETERS USED IN SIMULATION

Parameter	Value
Gate-source spacing	5 μm
Gate-drain space	10 μm
Gate length	2 μm
Gate width	100 μm
Al mole fraction of barrier layer	0.23
Al mole fraction of buffer layer	0.01
Gate metal work-function	4.25 V
Polarization scale parameter	0.29
Shallow compensating donors in the GaN buffer	1×10^{19} cm^{-3}
Acceptor-like traps doping concentration	1×10^{17} cm^{-3}
Acceptor-like buffer traps energy level	E_C - 0.9 eV
Doping concentration under source/drain contact	1×10^{20} cm^{-3}

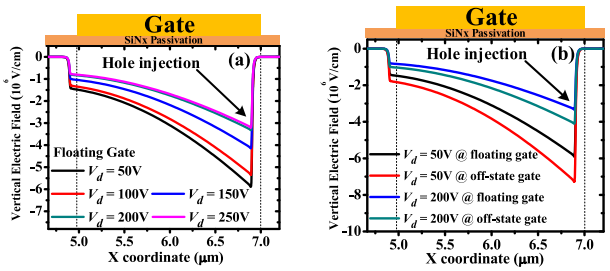

Fig. 8. Simulated vertical electric field along with the SiN/GaN interface at (a) floating gate and (b) comparison of vertical electric field between a floating gate and an off-state gate.

doping level. Therefore, low-density deep-level (E_C−0.9eV) acceptor-like traps (10^{15} cm^{-3}) with a deeper-level capture cross-section area of 10^{-15} cm^2 are applied to the buffer layer. To verify the trap effect on the gate breakdown, the transient voltage stress effect is simulated. The key parameters used in the 2D device simulation are given in Table I.

Using the above-mentioned physical models, the Sentaurus device simulation was performed to verify the hot-hole injection mechanisms as shown in Fig. 8. Under the TLP pulse stress, a high negative electric field peak indicates that the direction of the vertical electric field is pointing upward and favorable for hot-hole injection. Under low TLP stress voltage (50 - 100V), the high negative vertical electrical field will drive the hot-hole injection to the gate with negative charge accumulation underneath the gate region to increase the energy barrier. With the increased TLP drain voltage, the decreased vertical electrical field results in less hot-hole injection to the gate. And the lower energy barrier will result in an increased V_{th} as shown in the experiments. When the TLP stress voltage is up to 200V, the vertical electrical field will reach the saturation for the saturated V_{th}. And under off-state voltage, the negative gate voltage will induce higher vertical electrical field as the comparison shown in Fig. 8(b). The increased energy barrier induced by the high negative electrical field is the reason of the sever V_{th} degradation under off-state TLP stress.

More insight is provided with the hole temperature distribution along the gate region in Fig. 9. The hole temperature is a key indicator of hot-hole injection in semiconductor devices.

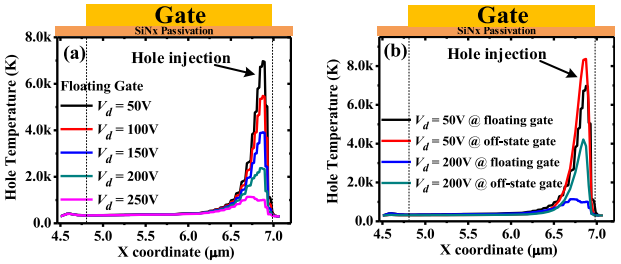

Fig. 9. Simulated hole temperature along with the SiN/GaN interface at (a) floating gate and (b) comparison of hole temperature between a floating gate and an off-state gate.

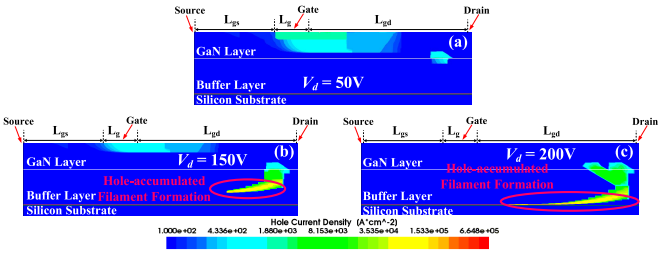

Fig. 10. Simulated hole-accumulated filament formation in the buffer layer for a floating gate.

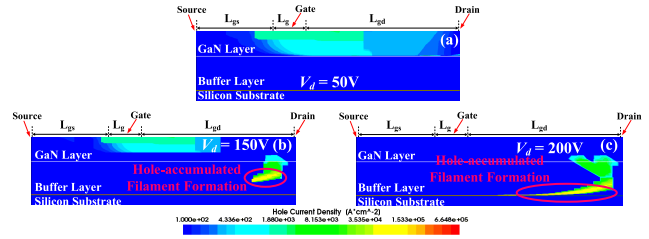

Fig. 11. Simulated hole-accumulated filament formation in the buffer layer for an off-state gate.

And with increasing TLP drain voltage at a floating gate, a decreased hole temperature is obtainable which supports less hot-hole injection at the gate region under high TLP stress. However, an increased hole temperature is displayed under an off-state gate voltage in Fig. 9(b). Higher hole temperature indicates more hole injection under an off-state gate voltage, and the injected hole will induce more mirror electrons to compensate the 2DEG with significant V_{th} degradation.

An exceptionally large hole-accumulation region in the bottom of the buffer layer between the drain and gate as seen in Figs. 10 and 11 supporting the filament formation under high TLP pulse stress for a floating gate or an off-state gate. As shown in Fig. 10(a), the holes are accumulated at the gate region with decreased V_{th} under low TLP stress voltage (50V). However, with the increased TLP voltage, there are more holes accumulated in the buffer layer to form the filament formation. And this mechanism has also been verified with different gate conditions. The off-state gate voltage will offer more hot-hole to be injected to the gate region with a significant Vth degradation as shown in Fig. 6(a). The hole-accumulated filament formation will enhance the local electric field near the

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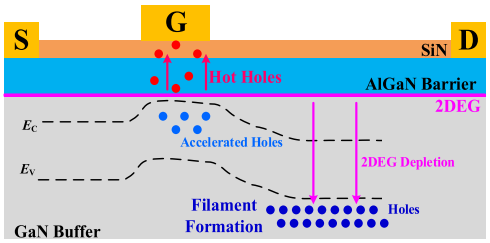

Fig. 12. The insight of failure mechanism under the ESD pulse stress.

drain side to deplete the 2DEG with increased R_{on} degradation. Compared to that under the floating gate, there are more holes accumulated at the gate under low TLP stress voltage, while there are less accumulated holes at the buffer region. However, when the TLP stress voltage reaches to 250V, the hole filament formation region and density are closely to that under a floating gate. Those simulation results successfully verify the experimental results as shown in previous sections.

Overall, the physical mechanisms of TLP stress in GaN power devices is illustrated in Fig. 12. The high electric field from ESD stress strengthens the electron-hole generation at the drain side. The excess electrons are collected at the drain, while the excess holes follow two routes: 1) to the source via the channel under low TLP pulse stress and 2) to the buffer layer under high ESD stress. Accelerated hot holes under the gate may inject into the SiN passivation layer. Excess holes are injected into the buffer layer because of the uneven buffer trap distribution [28]. These accumulated holes in the buffer layer can enhance the local electric field near the drain side. Injected holes could also get trapped in the buffer and trigger an avalanche condition forming a highly conductive narrow hole path or filament.

VI. Conclusion

The failure mechanisms of electrical degradations under the ESD stress are discussed. An un-anticipated decrease in V_{th} is observed at the beginning of stress under low pulse voltage, while V_{th} and R_{on} monotonically increase under high pulse voltage. According to the experimental data and device simulation results, the V_{th} reduction is attributed to hot-hole injection underneath the gate. This effect is increased by adding an off state gate voltage during TLP stress. As the total number of TLP pulses and voltage increase, the filament is formed by accumulated holes interacting with the traps in the buffer layer, leading to an increase in V_{th} and R_{on}. These mechanisms are verified by distinct degradations in the restore phase and leakage current analysis.

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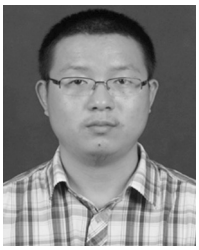

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